

## 30V N-Channel MOS

### Description

The NP45N03 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. Standard Product NP45N03 is Pb-free (meets ROHS & Sony 259 specifications).

### General Features

- ◆  $V_{DS} = 30V$   $I_D = 45A$   
 $R_{DS(ON)}(Typ.) = 6.3m\Omega$  @  $V_{GS} = 10V$   
 High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

### Application

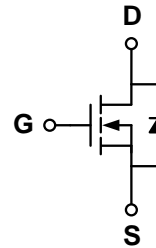
- ◆ High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- ◆ Networking DC-DC Power System
- ◆ Load switch

### Package

- ◆ DFN3×3-8L



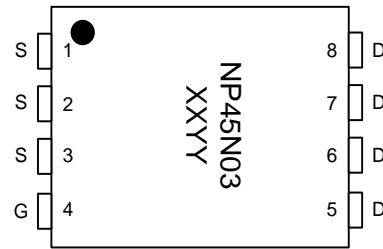
### Schematic diagram



### Marking and pin assignment

#### DFN3×3-8L

(Top View)



### Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP45N03QR-G	-55°C to +150°C	DFN3×3-8L	3000

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		$V_{DS}$	30	V
Gate-source voltage		$V_{GS}$	±20	V
Continuous Drain Current	TC=25°C	$I_D$	45	A
	TC=100°C		28	
Pulsed Drain Current		$I_{DP}$	180	A
Avalanche Current		IAS	32	A
Avalanche energy( L=0.5mH)		EAS	120	mJ
Maximum power dissipation	TC=25°C	$P_D$	28	W
Power Dissipation – Derate above 25°C	TC=25°C		1.67	
Operating junction Temperature range		$T_j$	-55—150	°C

**Electrical Characteristics** (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
BVDSS Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C, $I_D=1mA$		27		mV/°C
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
		$T_J=85^\circ C$	-	-	30	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.5	V
Drain-source on-state resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS}=10V, I_D=45A$	-	6.3	7	mΩ
		$V_{GS}=4.5V, I_D=40A$		9.9	12.9	
On Status Drain Current	$I_{D(ON)}$	$V_{DS}=10V, V_{GS}=10V$	50	-	-	A
<b>Diode Characteristics</b>						
Diode Forward Voltage <sup>1</sup>	$V_{SD}$	$I_{SD}=1A, V_{GS}=0V$	-	0.8	1.1	V
Diode Continuous Forward Current	$I_S$		-	-	46	A
Reverse Recovery Time	$t_{rr}$	$I_F=30A,$	-	9.2	-	ns
Reverse Recovery Charge	$Q_{rr}$	$dI/dt=100A/us$	-	2	-	nC
<b>Dynamic Characteristics<sup>2</sup></b>						
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}=0V, f=1MHz$	-	1.7	-	
Input capacitance	$C_{ISS}$	$V_{GS}=0V, V_{DS}=20V$ $f=1.0MHz$	-	1317	-	pF
Output capacitance	$C_{OSS}$		-	163	-	
Reverse transfer capacitance	$C_{RSS}$		-	131	-	
Turn-on delay time	$t_{D(ON)}$	$V_{GS}=10V, V_{DD}=15V,$ $R_L=20\Omega, I_D=15A, R_G=3.3\Omega$	-	4.6	-	ns
Turn-on Rise time	$t_r$		-	12.2	-	
Turn-off delay time	$t_{D(OFF)}$		-	26.6	-	
Turn-off Fall time	$t_f$		-	8	-	
Total gate charge	$Q_g$	$V_{GS}=4.5V, I_D=15A$ $V_{DS}=15V$	-	12.6		nC
Gate-source charge	$Q_{gs}$		-	4.2		
Gate-drain charge	$Q_{gd}$		-	5.1	-	
<b>Drain-Source Diode Characteristics</b>						
Diode forward voltage	$V_{SD}$	$I_{SD}=50A, V_{GS}=0V$	-	0.8	1.1	V

 Note: 1: Pulse test; pulse width  $\leq 300ns$ , duty cycle  $\leq 2\%$ .

2: Guaranteed by design, not subject to production testing.

**Thermal Characteristics**

Parameter	Symbol	Typical	Unit
Thermal Resistance-Junction to Case	$R_{\theta jc}$	1.7	°C/W
Thermal Resistance junction-to ambient	$R_{\theta ja}$	62.5	

## Typical Performance Characteristics

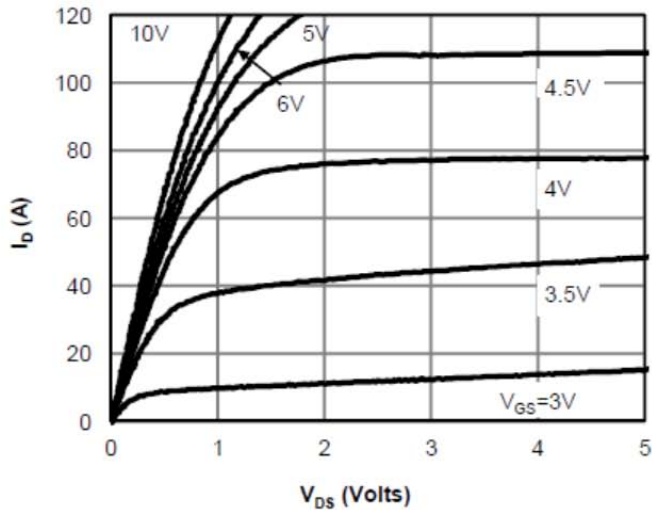


Fig 1: On-Region Characteristics (Note E)

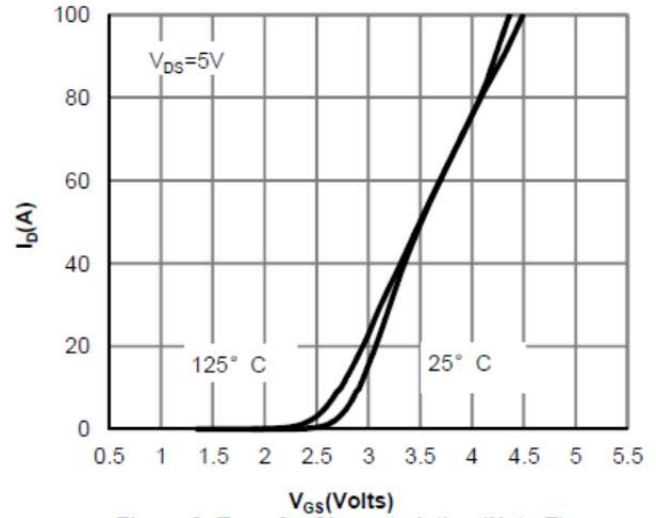


Figure 2: Transfer Characteristics (Note E)

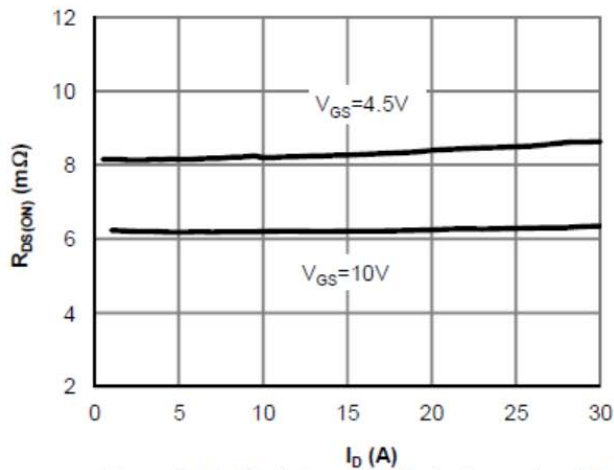


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

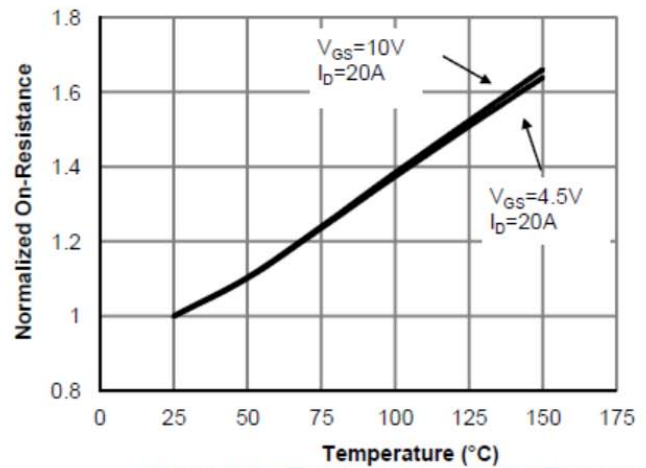


Figure 4: On-Resistance vs. Junction Temperature (Note E)

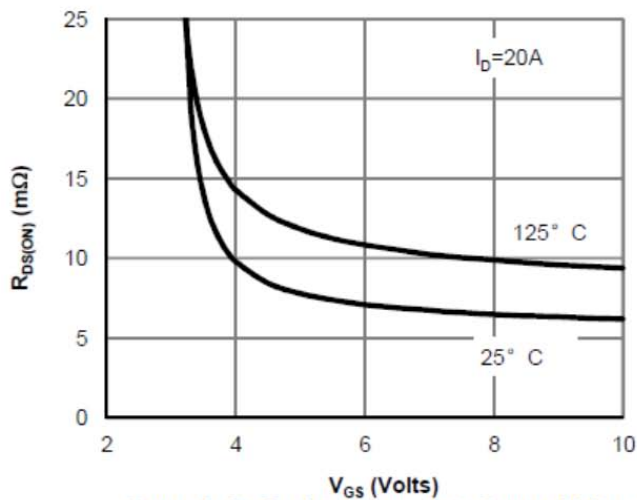


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

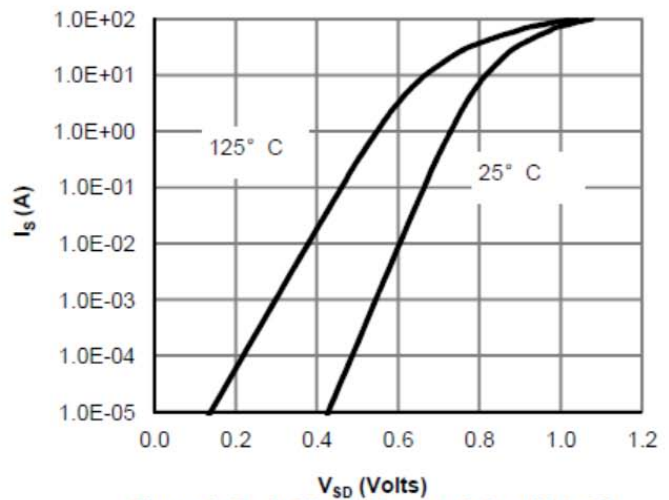


Figure 6: Body-Diode Characteristics (Note E)

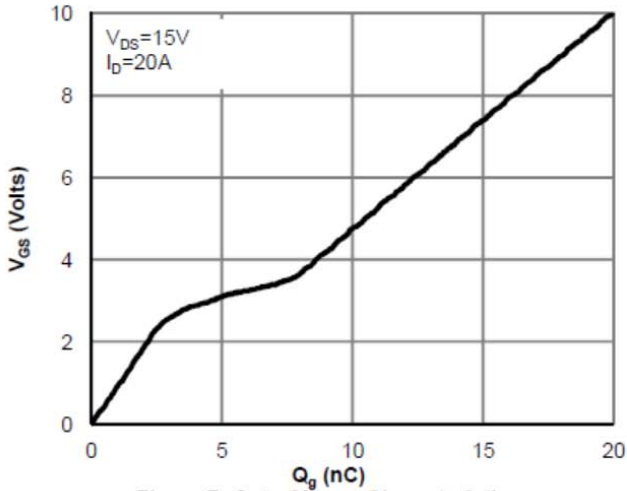


Figure 7: Gate-Charge Characteristics

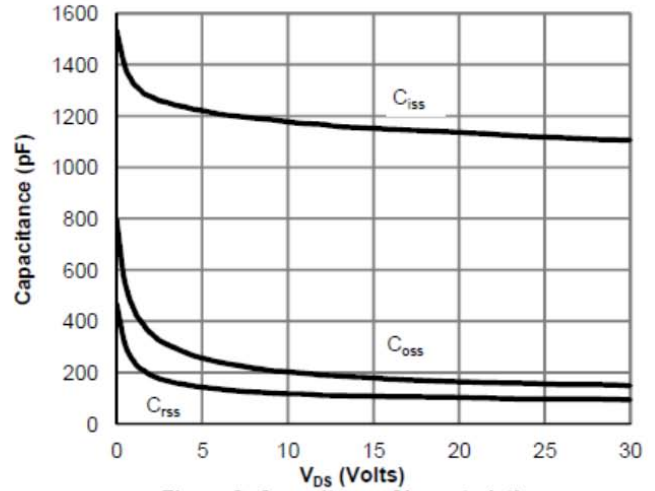


Figure 8: Capacitance Characteristics

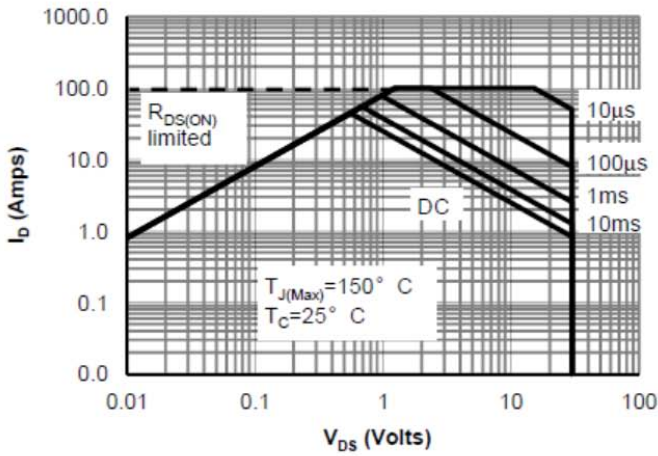


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

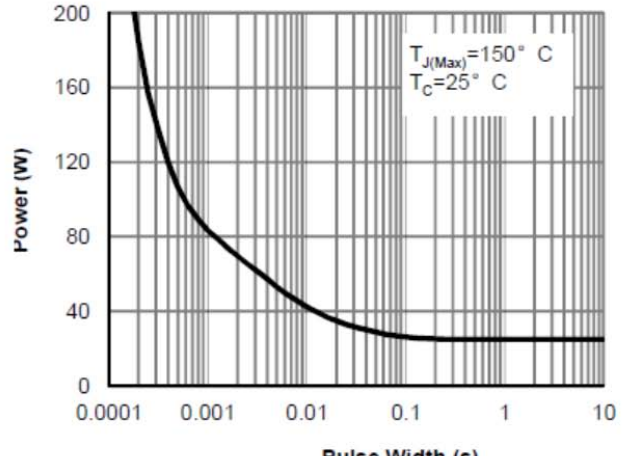


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

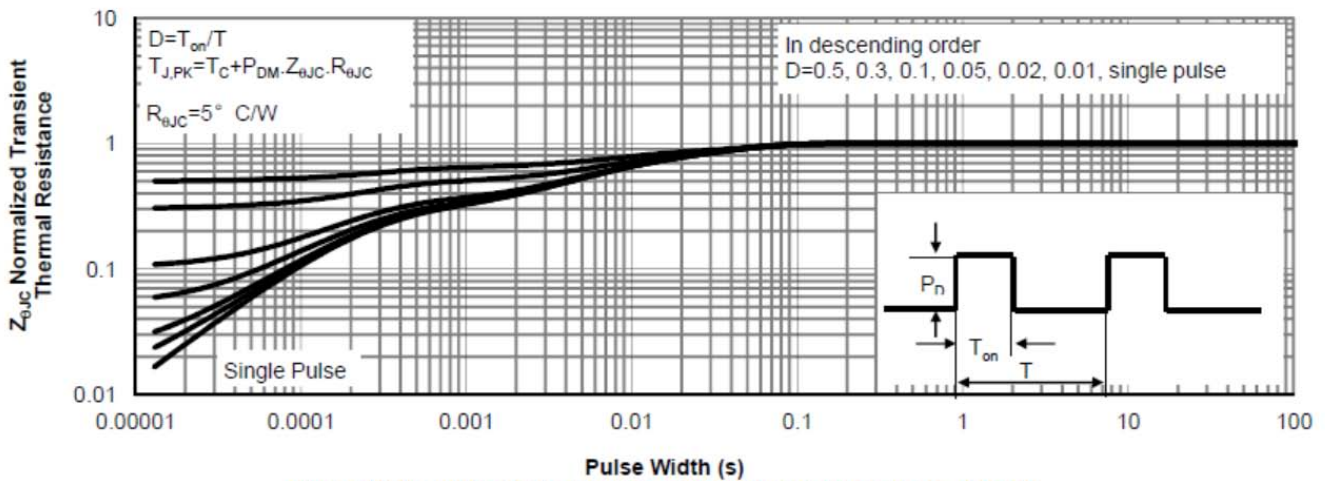


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

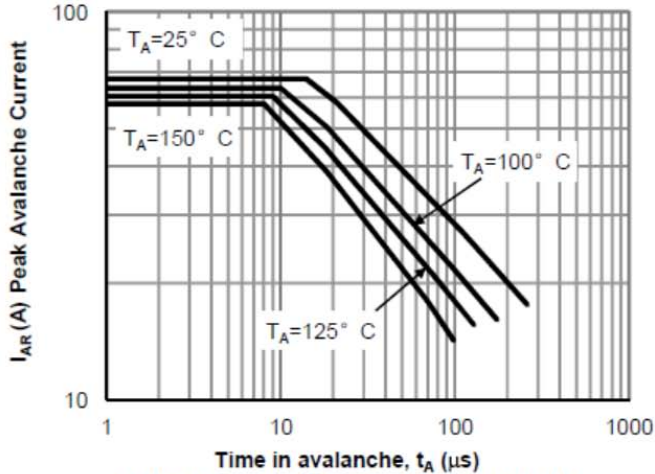


Figure 12: Single Pulse Avalanche capability (Note C)

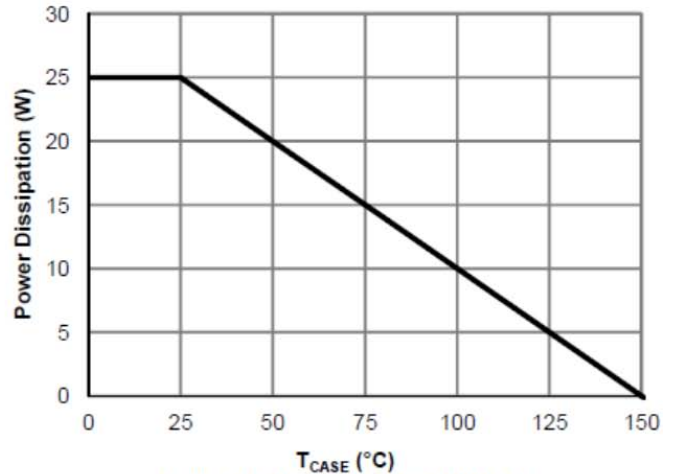


Figure 13: Power De-rating (Note F)

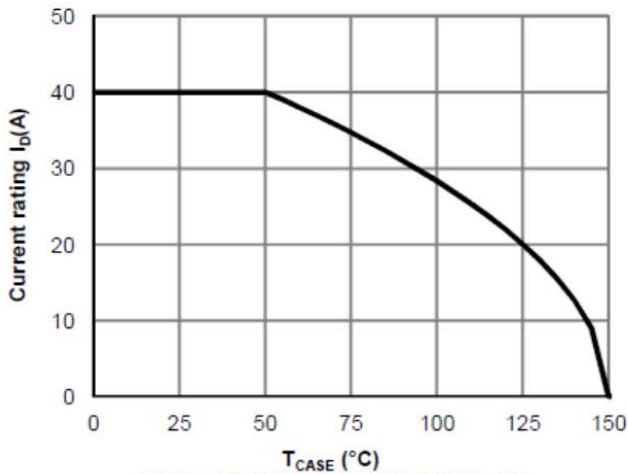


Figure 14: Current De-rating (Note F)

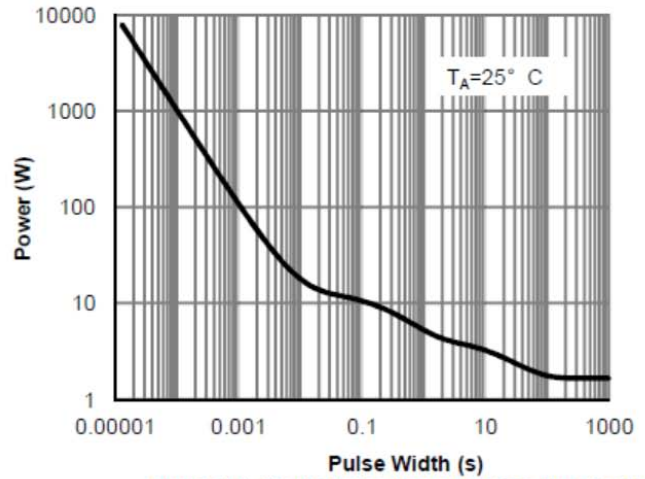


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

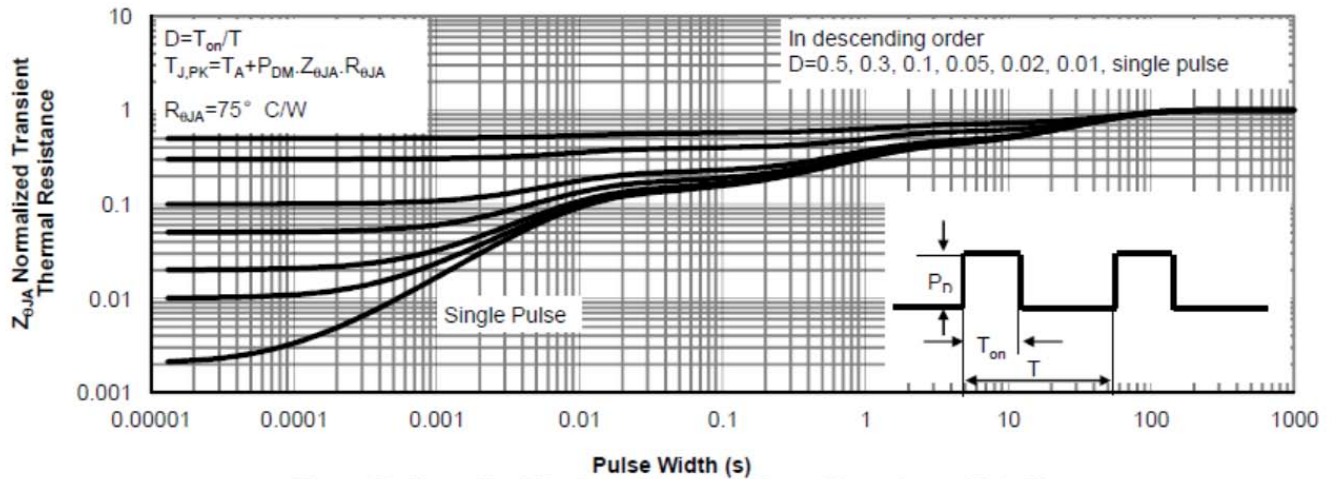
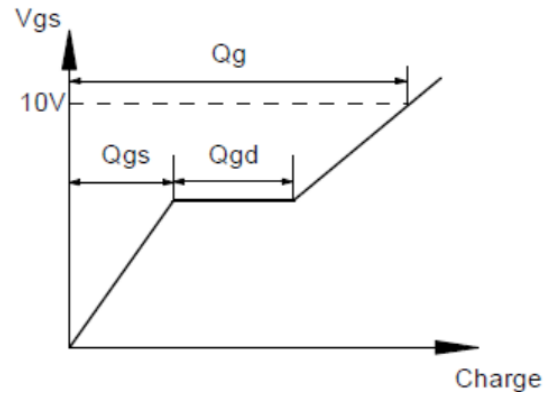
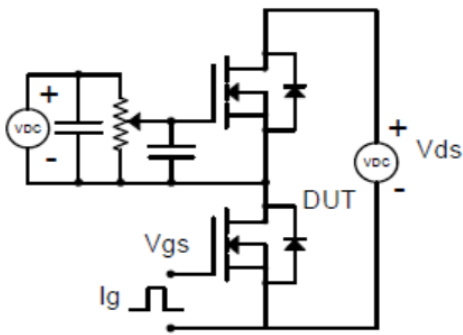
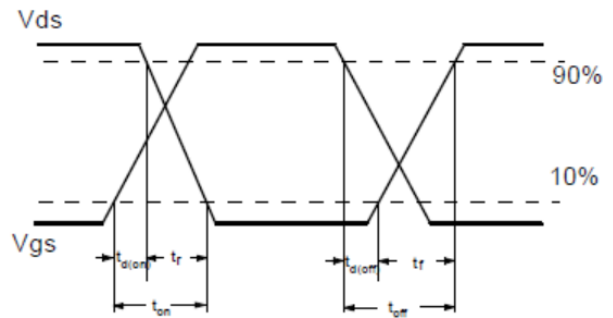
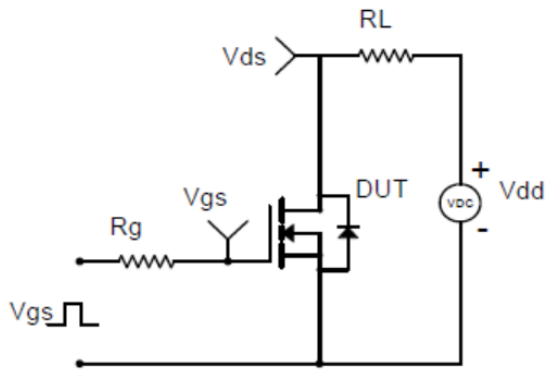


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

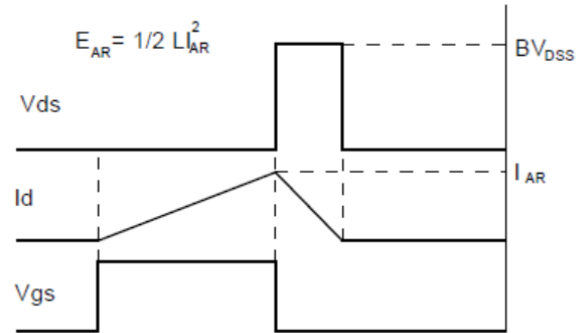
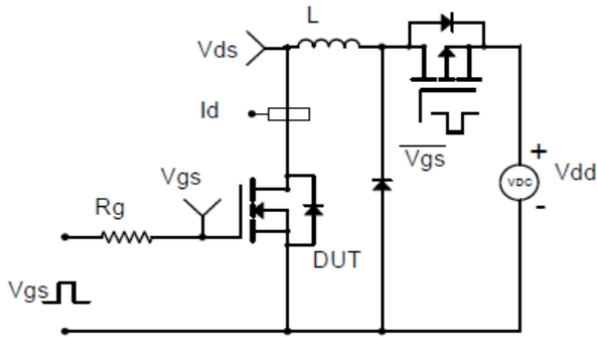
Gate Charge Test Circuit & Waveform



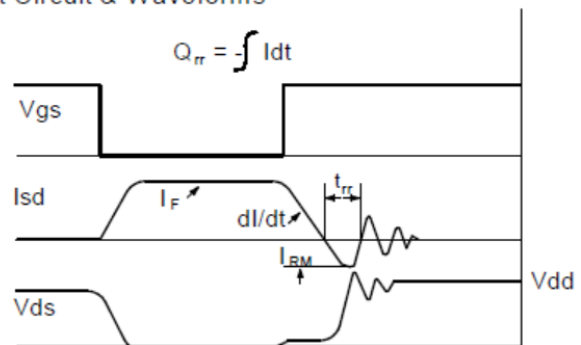
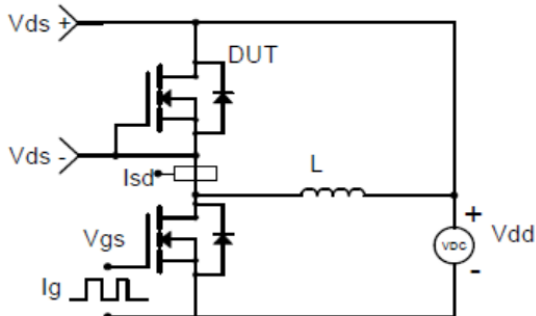
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

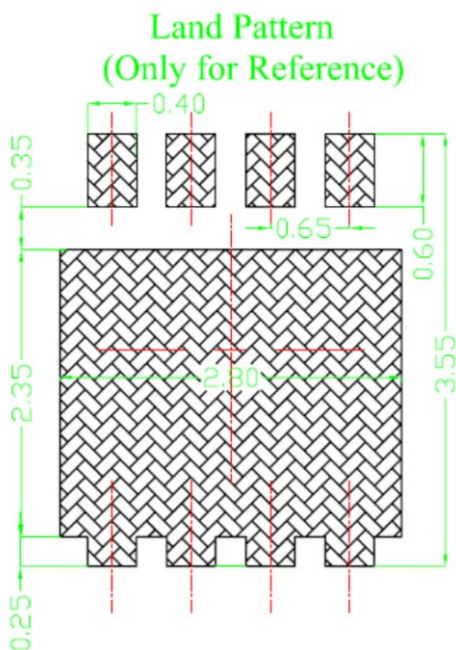
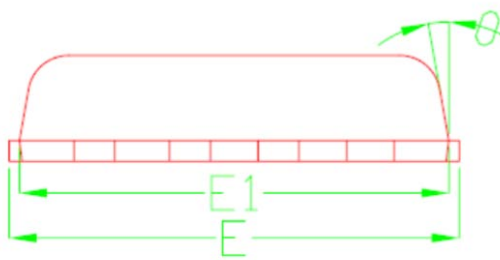
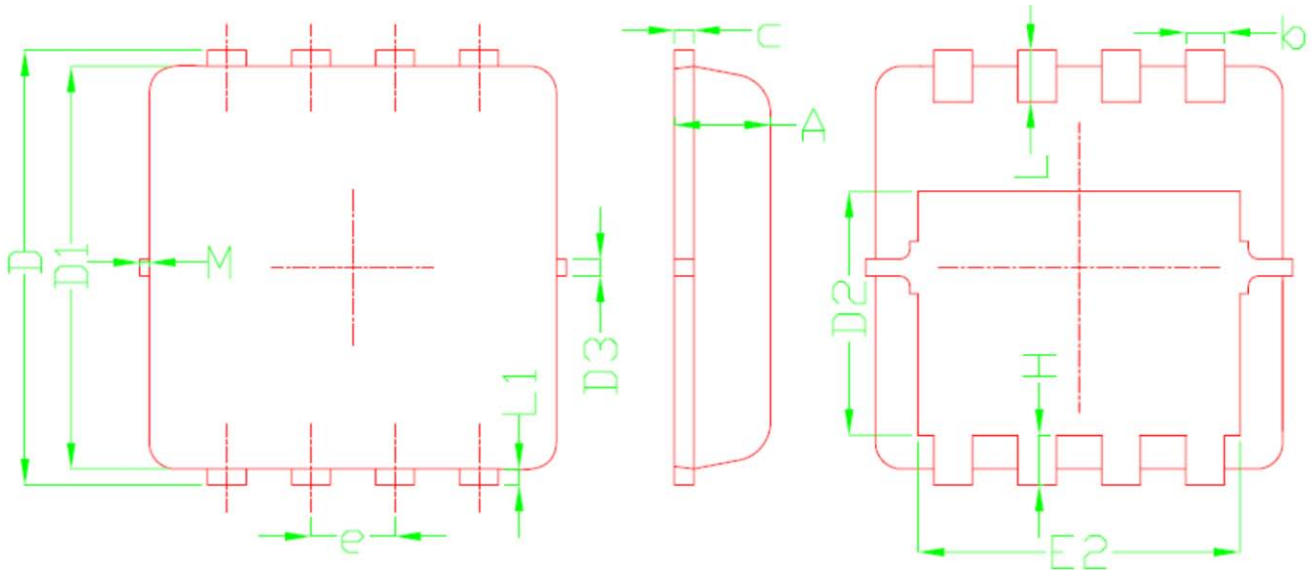


Diode Recovery Test Circuit & Waveforms



## Package Information

- DFN3×3-8L



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
$\theta$	---	10°	12°
M	*	*	0.15
* Not specified			

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