

60V N-Channel Enhancement Mode MOSFET

Description

The NP6050G uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- ◆ $V_{DS} = 60V$ $I_D = 50A$
 $R_{DS(ON)}(Typ.) = 16.5m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(ON)}(Typ.) = 20.5m\Omega$ @ $V_{GS} = 4.5V$
 High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

Application

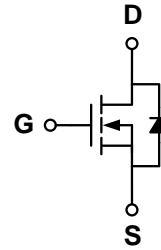
- ◆ Load switch

Package

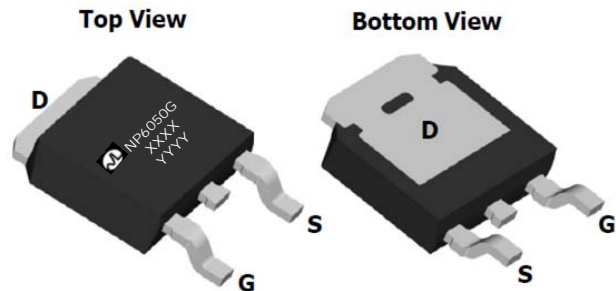
- ◆ TO-252-2L

100% UIS TESTED!
100% ΔV_{ds} TESTED!

Schematic diagram



Marking and pin assignment



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP6050G	-55°C to +150°C	TO-252-2L	2500

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V_{GS}	± 20	V
Continuous Drain Current	TC=25°C	I_D	50	A
	TC=100°C		35	
Pulsed Drain Current		I_{DP}	200	A
Avalanche Current		IAS	24	A
Avalanche energy(L=0.5mH) ^(note1)		EAS	130	mJ
Maximum power dissipation	TC=25°C	P_D	85	W
	TC=100°C		44	
Operating junction Temperature range		T_j	-55—150	°C

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
		$T_J=85^\circ C$	-	-	30	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	2	2.8	V
Drain-source on-state resistance ¹	$R_{DS(on)}$	$V_{GS}=10V, I_D=25A$	-	16.5	20	m Ω
		$V_{GS}=4.5V, I_D=25A$	-	20.5	25	
On Status Drain Current	$I_{D(on)}$	$V_{DS}=10V, V_{GS}=10V$	50	-	-	A
Diode Characteristics						
Diode Forward Voltage ¹	V_{SD}	$I_{SD}=50A, V_{GS}=0V$	-	0.8	1.1	V
Diode Continuous Forward Current	I_S		-	50	-	A
Reverse Recovery Time	t_{rr}	$I_F=20A,$	-	28	-	ns
Reverse Recovery Charge	Q_{rr}	$di/dt=100A/\mu s$	-	40	-	nC
Dynamic Characteristics²						
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}=0V, f=1MHz$	-	0.65	-	Ω
Input capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=20V$ $f=1.0MHz$	-	1920	-	pF
Output capacitance	C_{OSS}		-	155	-	
Reverse transfer capacitance	C_{RSS}		-	115	-	
Turn-on delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=20V,$ $R_L=20\Omega, I_D=1A, R_G=6\Omega$	-	8	-	ns
Turn-on Rise time	t_r		-	5	-	
Turn-off delay time	$t_{D(off)}$		-	30	-	
Turn-off Fall time	t_f		-	5.5	-	
Total gate charge	Q_g	$V_{GS}=10V, I_D=20A$ $V_{DS}=20V$	-	47.5	-	nC
Gate-source charge	Q_{gs}		-	6	-	
Gate-drain charge	Q_{gd}		-	14.5	-	
Drain-Source Diode Characteristics						
Diode forward voltage	V_{SD}	$I_{SD}=50A, V_{GS}=0V$	-	0.8	1.1	V

 Note: 1: Pulse test; pulse width $\leq 300ns$, duty cycle $\leq 2\%$.

2: Guaranteed by design, not subject to production testing.

Thermal Characteristics

Parameter	Symbol	Typical	Unit
Thermal Resistance-Junction to Case	$R_{\theta jc}$	1.7	$^\circ C/W$
Thermal Resistance junction-to ambient	$R_{\theta ja}$	62.5	

Typical Performance Characteristics

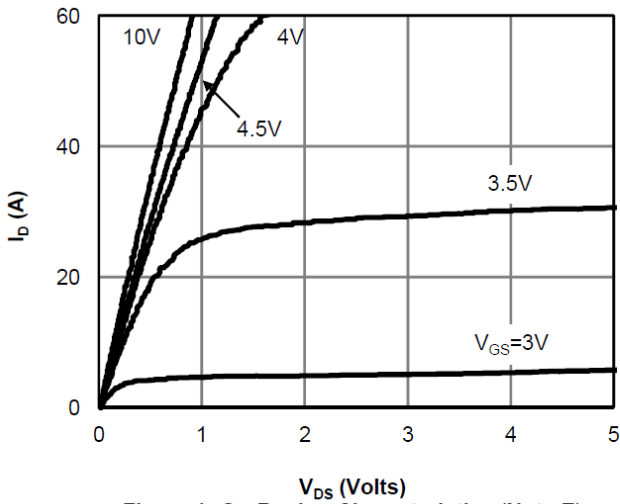


Figure 1: On-Region Characteristics (Note E)

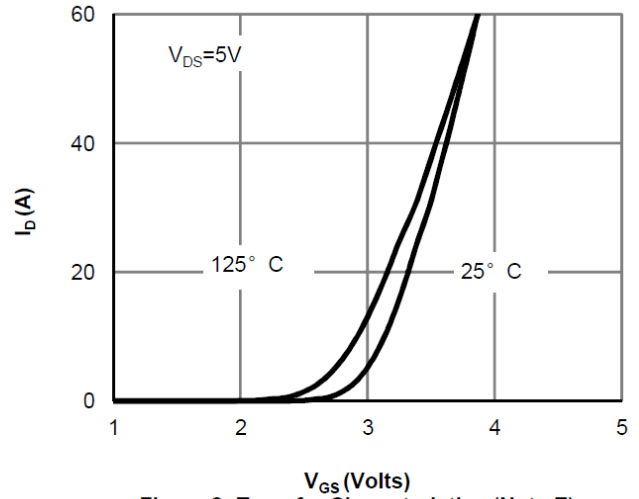


Figure 2: Transfer Characteristics (Note E)

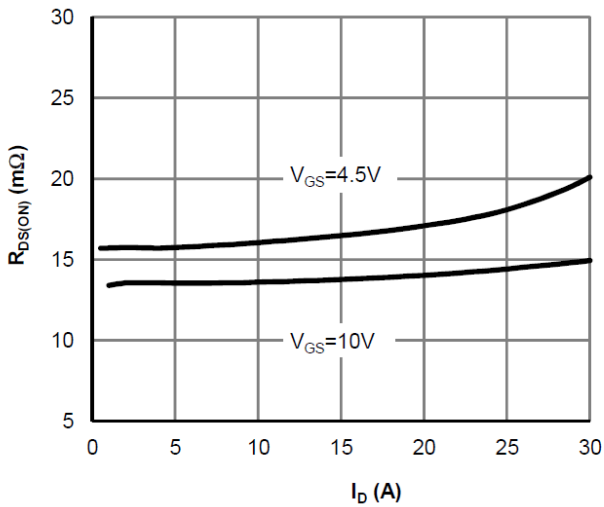


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

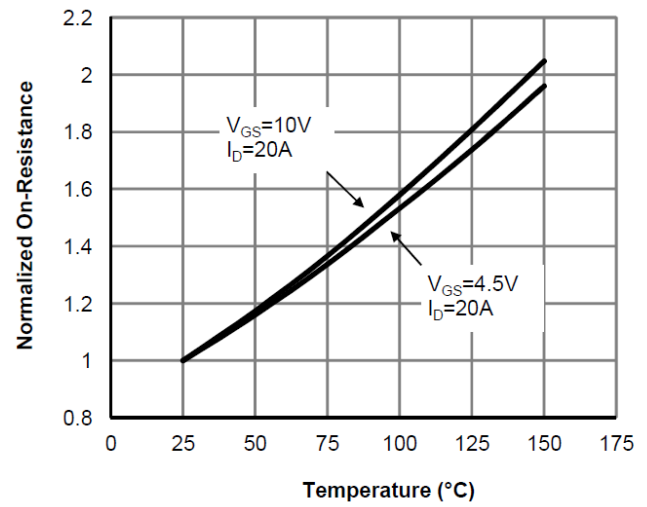


Figure 4: On-Resistance vs. Junction Temperature (Note E)

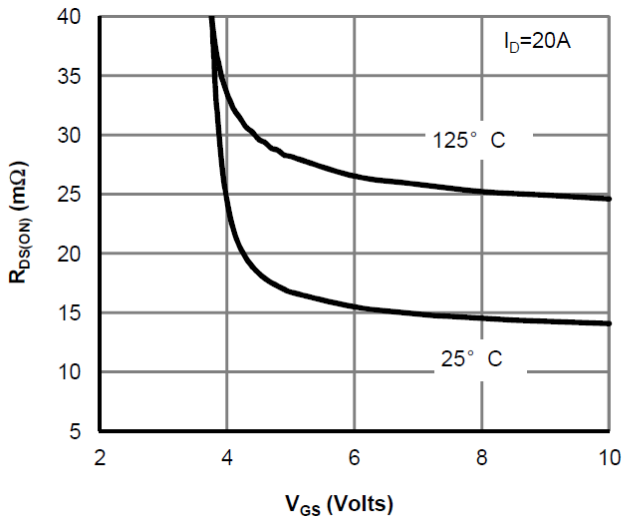


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

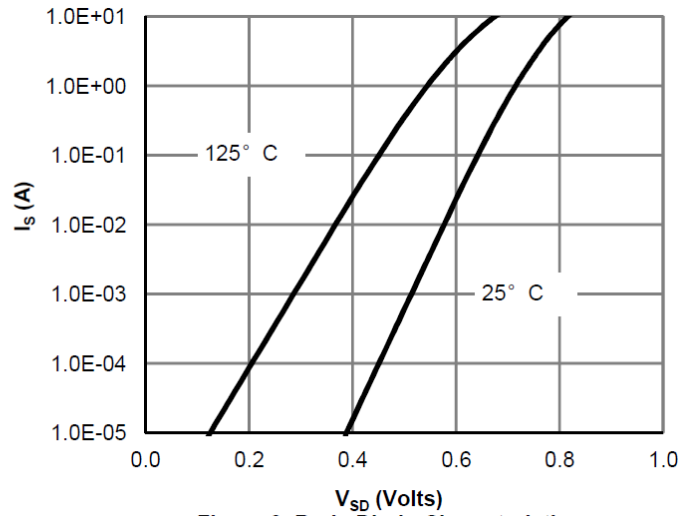


Figure 6: Body-Diode Characteristics (Note E)

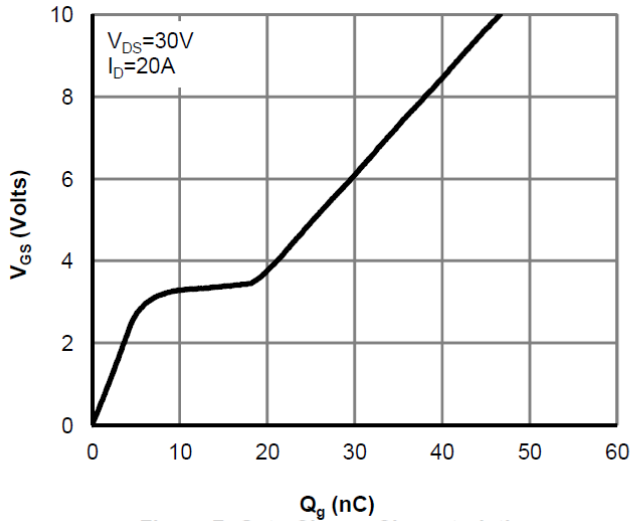


Figure 7: Gate-Charge Characteristics

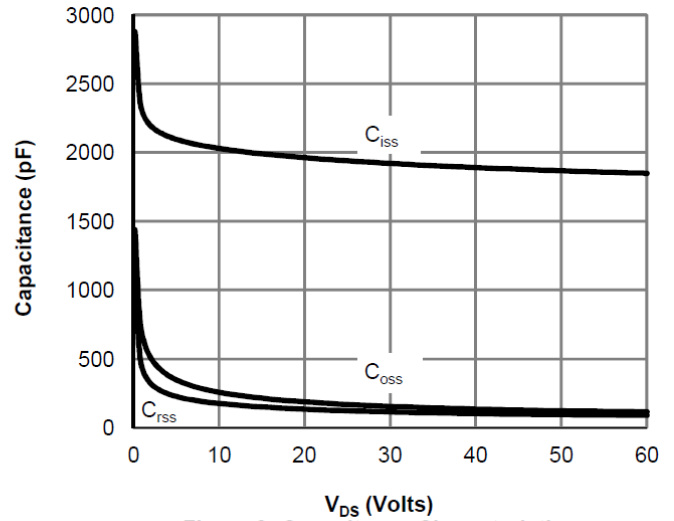


Figure 8: Capacitance Characteristics

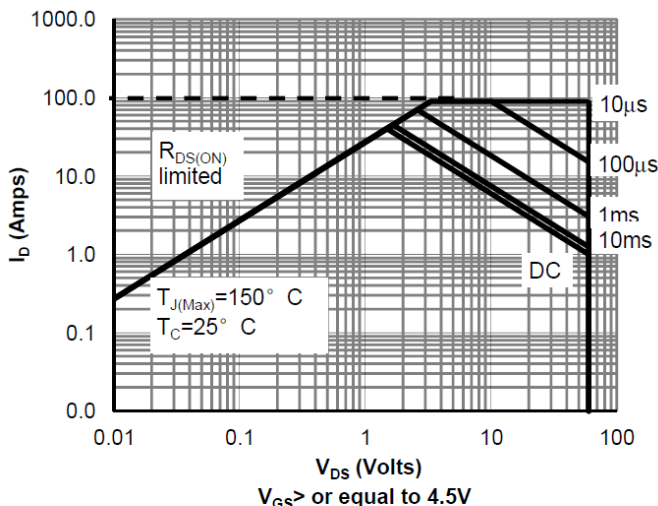


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

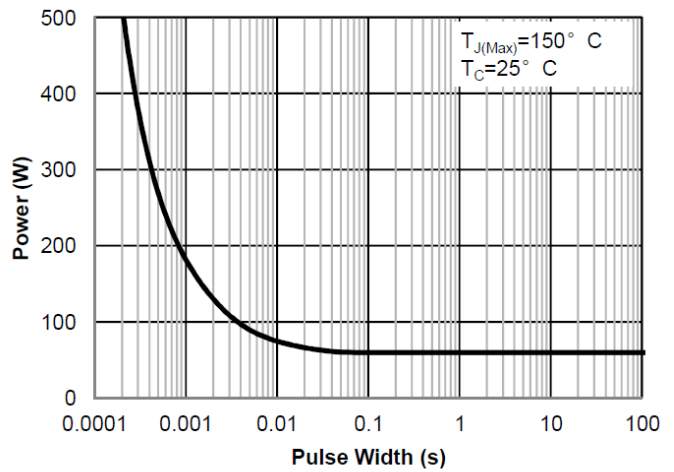


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

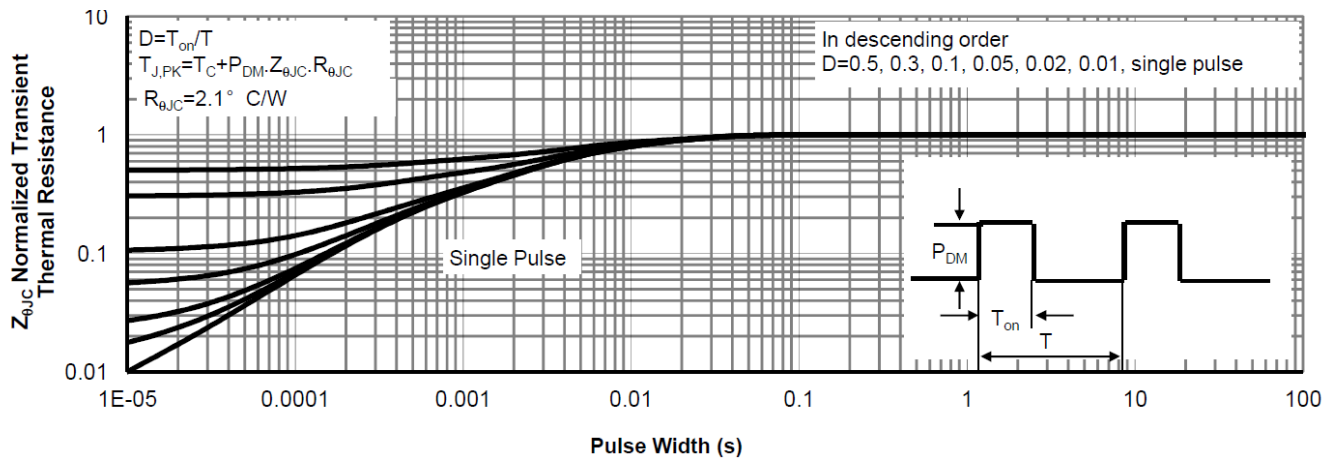


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

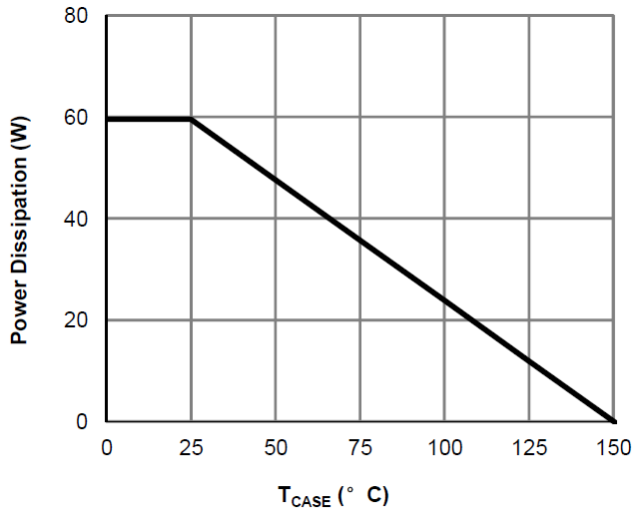


Figure 12: Power De-rating (Note F)

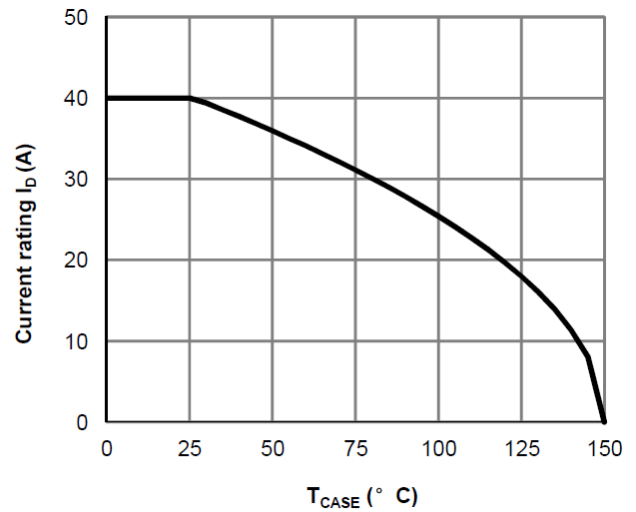


Figure 13: Current De-rating (Note F)

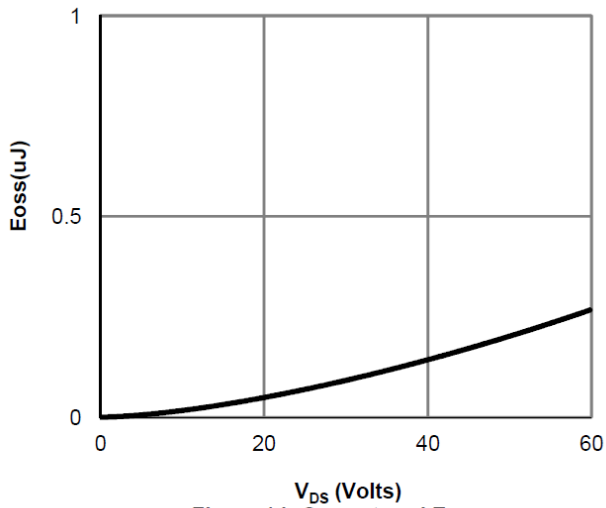


Figure 14: Coss stored Energy

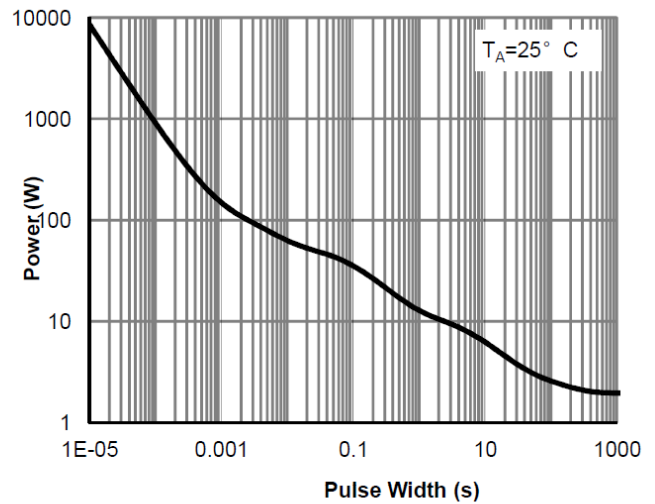


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

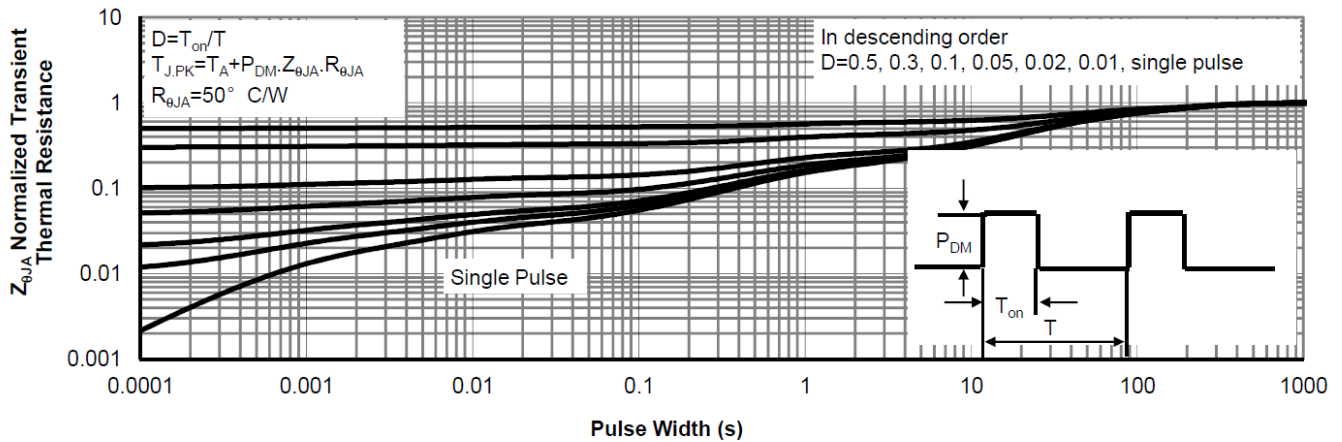


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

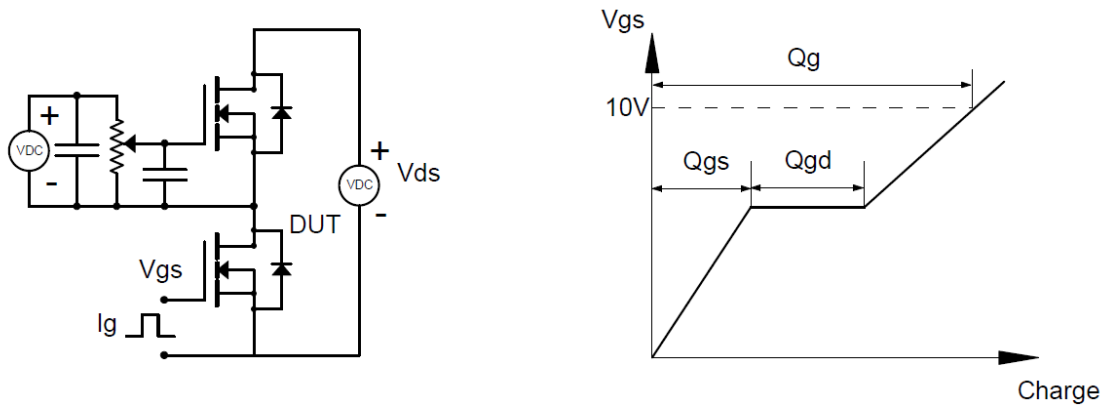


Figure B: Resistive Switching Test Circuit & Waveforms

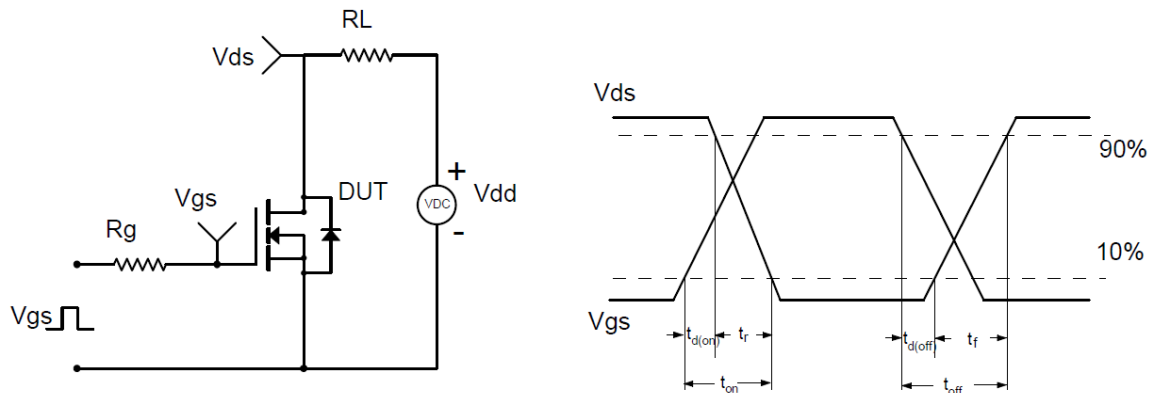


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

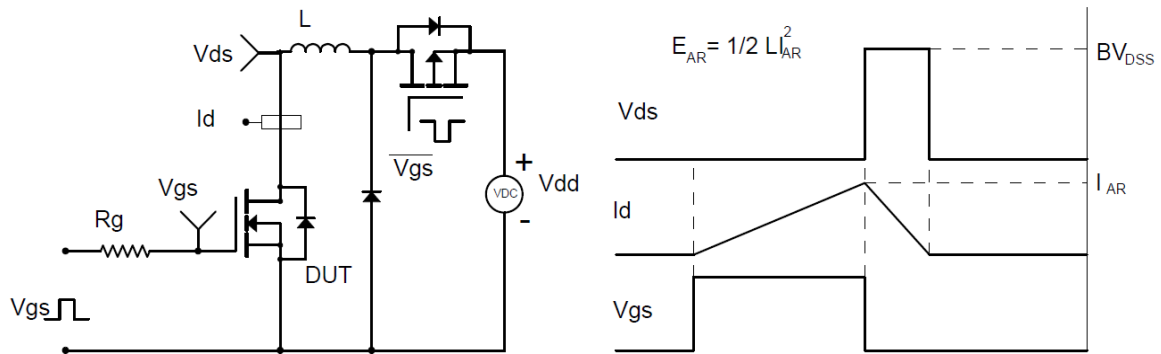
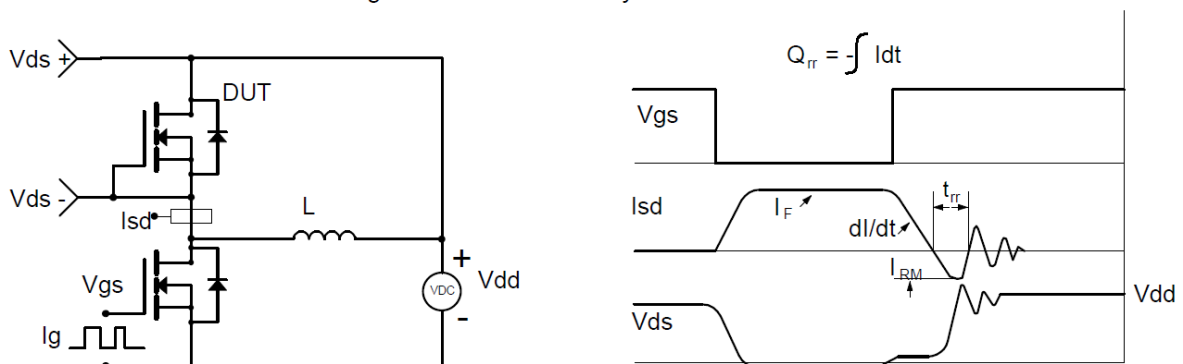
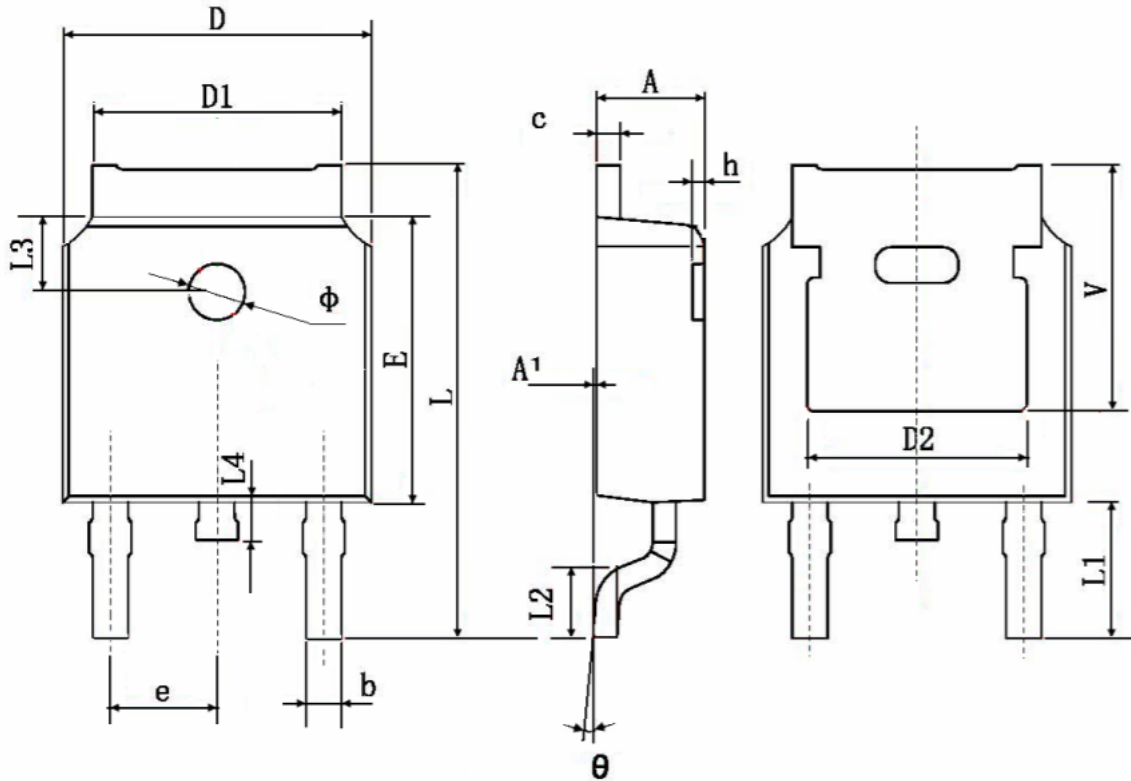


Figure D: Diode Recovery Test Circuit & Waveforms



Package Information

- TO-252-2L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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