

## 40V Dual N-Channel Enhancement Mode MOSFET

### Description

The NP6884D6 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  with low gate charge.

This device is suitable for high side switch in SMPS and general purpose applications.

### General Features

- ◆  $V_{DS} = 40V$ ,  $I_D = 26A$   
 $R_{DS(ON)} = 13.7\ m\Omega$  (typical) @  $V_{GS} = 10V$   
 $R_{DS(ON)} = 17.8\ m\Omega$  (typical) @  $V_{GS} = 4.5V$
- ◆ Excellent gate charge x  $R_{DS(ON)}$  product(FOM)
- ◆ Very low on-resistance  $R_{DS(ON)}$
- ◆ 150 °C operating temperature
- ◆ Pb-free lead plating
- ◆ 100% UIS tested

### Application

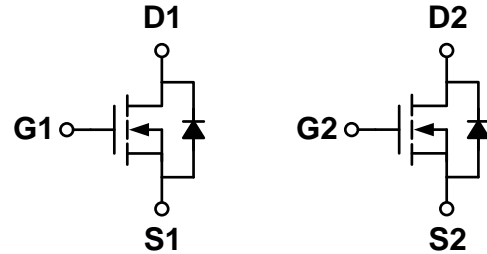
- ◆ DC/DC Converter
- ◆ Ideal for high-frequency switching and synchronous rectification

### Package

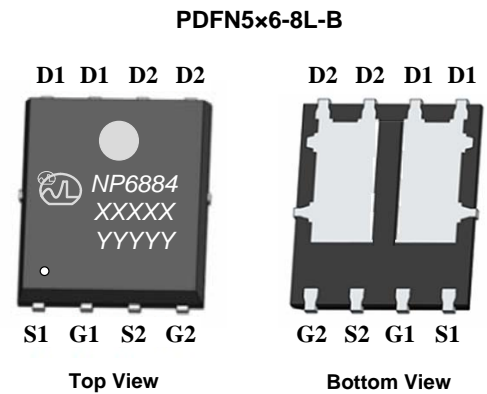
- ◆ PDFN5\*6-8L-B



### Schematic diagram



### Marking and pin assignment



XXXX—Wafer Information  
 YYYY—Quality Code

### Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP6884D6-G	-55°C to +150°C	PDFN5*6-8L-B	5000

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	$V_{DS}$	40	V
Gate-source voltage	$V_{GS}$	±20	V
Drain Current-Continuous (Silicon Limited)	$I_D$	$T_A = 25^\circ C$	26
		$T_A = 75^\circ C$	18
Pulsed Drain Current (Package Limited)	$I_{DM}$	104	A
Single pulse avalanche energy	$E_{AS}$	50	mJ
Maximum power dissipation	$P_D$	$T_A = 25^\circ C$	31
		$T_A = 75^\circ C$	16

Operating junction Temperature range	T <sub>j</sub>	-55—150	°C
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**Electrical Characteristics** (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF Characteristics</b>						
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40	-	-	V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-body leakage	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
<b>ON Characteristics</b>						
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.4	2.0	V
Drain-source on-state resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =26A	-	13.7	15	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	-	17.8	19	
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =10A	-	50	-	S
<b>Dynamic Characteristics</b>						
Input capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V f=1.0MHz	-	1226	-	pF
Output capacitance	C <sub>OSS</sub>		-	103	-	
Reverse transfer capacitance	C <sub>RSS</sub>		-	87	-	
Gate resistance	R <sub>g</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1.0MHz	-	3.5	5	Ω
<b>Switching Characteristics</b>						
Turn-on delay time	t <sub>D(ON)</sub>	V <sub>DS</sub> =20V V <sub>GS</sub> =10V R <sub>L</sub> =1.5Ω R <sub>GEN</sub> =3Ω	-	6.4	-	ns
Rise time	t <sub>r</sub>		-	17.2	-	
Turn-off delay time	t <sub>D(OFF)</sub>		-	29	-	
Fall time	t <sub>f</sub>		-	16	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =20V, I <sub>D</sub> =10A V <sub>GS</sub> =10V	-	24.8	-	nC
Gate-source charge	Q <sub>gs</sub>		-	4.3	-	
Gate-drain charge	Q <sub>gd</sub>		-	4.8	-	

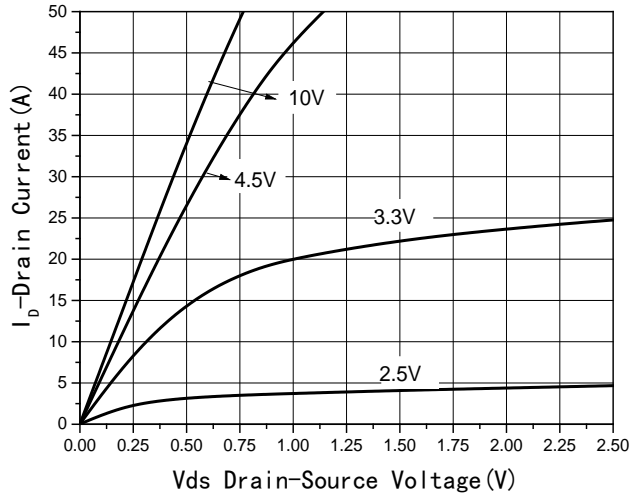
**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient <sup>A</sup>	R <sub>θJA</sub>	12	20	°C/W
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	33	
Maximum Junction-to-Lead <sup>B</sup>	R <sub>θJC</sub>	2.4	2.9	

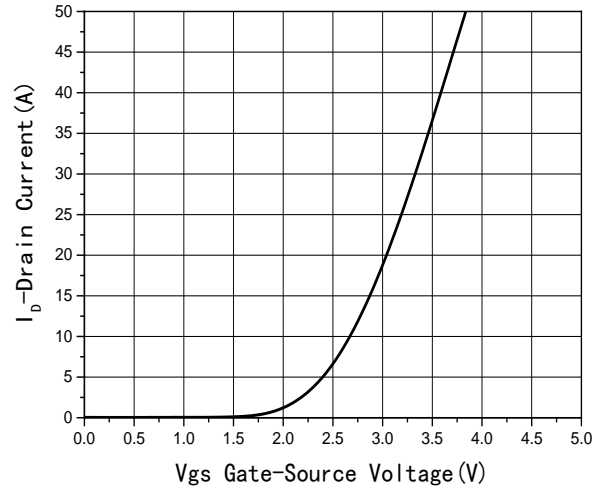
A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJC</sub> and lead to ambient.

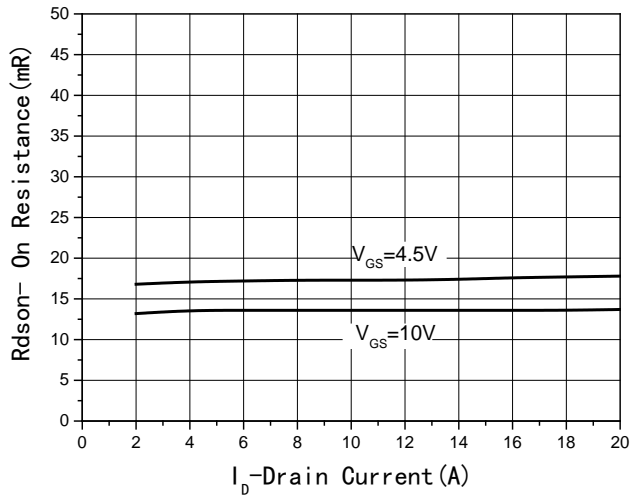
## Typical Performance Characteristics



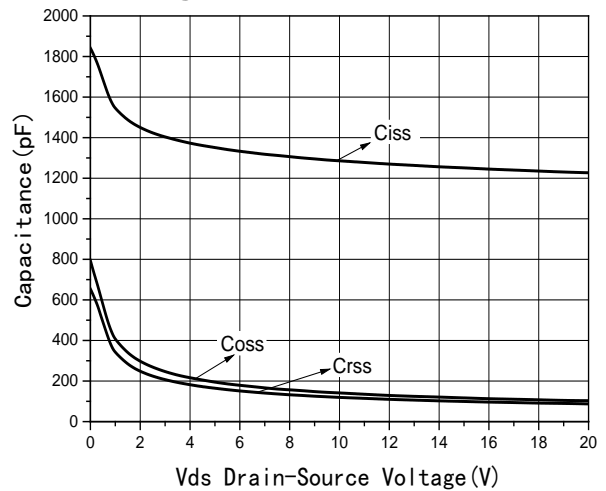
**Fig1 Output Characteristics**



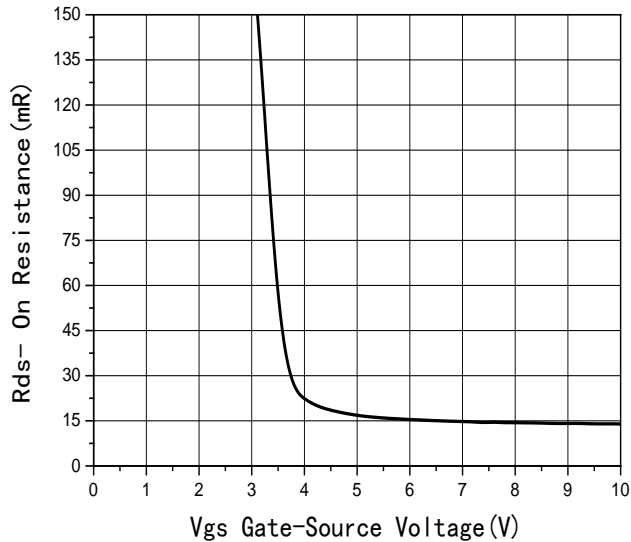
**Fig2 Transfer Characteristics**



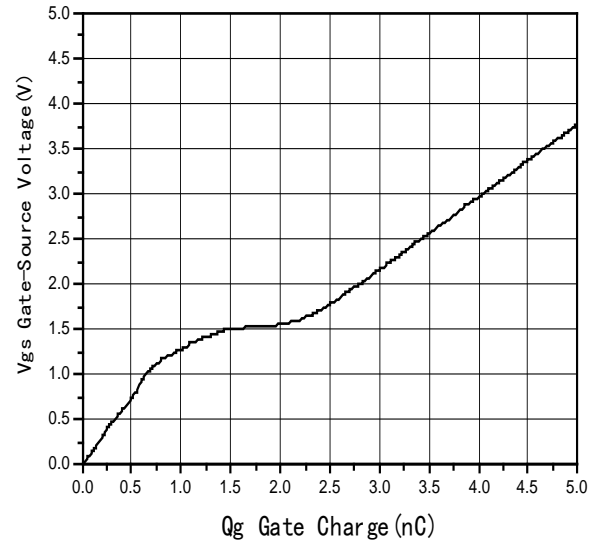
**Fig3  $R_{DS(on)}$ -Drain current**



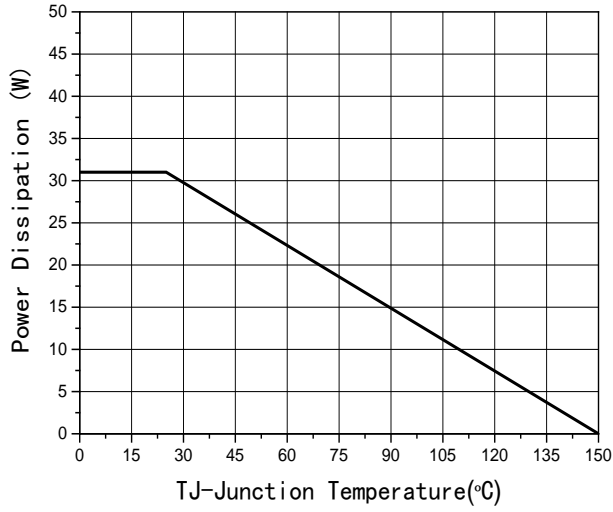
**Fig4 Capacitance vs  $V_{DS}$**



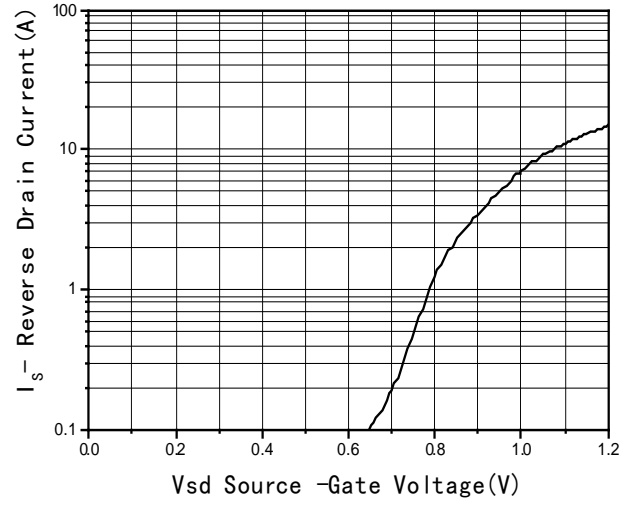
**Fig5  $R_{DS(on)}$ -Gate Drain voltage**



**Fig6 Gate Charge**



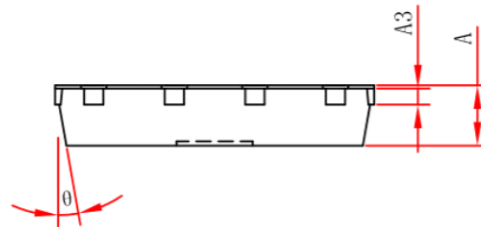
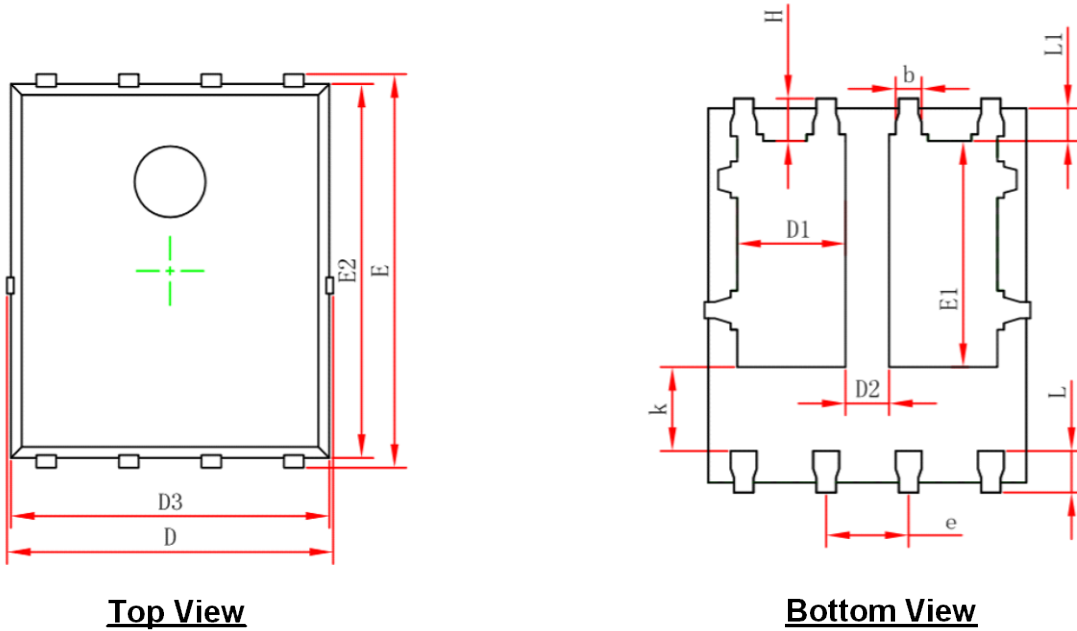
**Fig7 Power De-rating**



**Fig8 Source-Drain Diode Forward**

## Package Information

- PDFN5\*6-8L-B



**Side View**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.154REF.		0.006REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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