

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE4009S uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

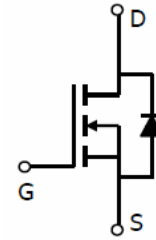
- **N-Channel**

$$V_{DS} = 40V, I_D = 9A$$

$$R_{DS(ON)} < 16m\Omega @ V_{GS}=10V$$

$$R_{DS(ON)} < 24m\Omega @ V_{GS}=4.5V$$

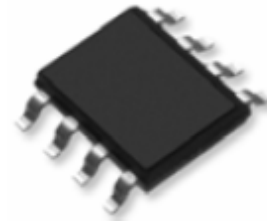
- High power and current handing capability
- Lead free product is acquired
- Surface mount package



Schematic diagram



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE4009S	NCE4009S	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	9	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	6.4	A
Pulsed Drain Current	I_{DM}	40	A
Maximum Power Dissipation	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	62.5	$^\circ C/W$
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N-CH Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.5	2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =8A	-	12.9	16	mΩ
		V _{GS} =4.5V, I _D =4A	-	18.9	24	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =8A	33	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, F=1.0MHz	-	964	-	PF
Output Capacitance	C _{oss}		-	109	-	PF
Reverse Transfer Capacitance	C _{rss}		-	96	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V, R _L =2.5Ω V _{GS} =10V, R _{GEN} =3Ω	-	5.5	-	nS
Turn-on Rise Time	t _r		-	14	-	nS
Turn-Off Delay Time	t _{d(off)}		-	24	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Q _g	V _{DS} =20V, I _D =8A, V _{GS} =10V	-	22.9	-	nC
Gate-Source Charge	Q _{gs}		-	3.5	-	nC
Gate-Drain Charge	Q _{gd}		-	5.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =9A	-	0.8	1.2	V

N- Channel Typical Electrical and Thermal Characteristics (Curves)

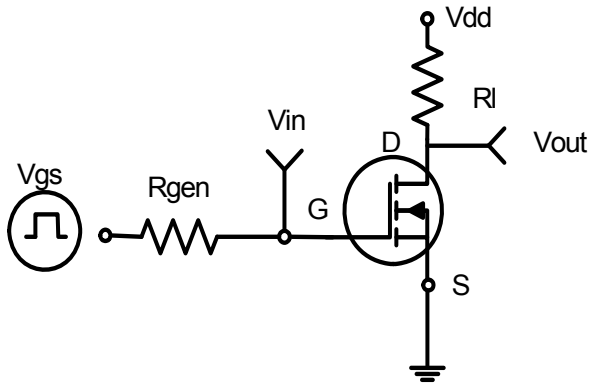


Figure 1: Switching Test Circuit

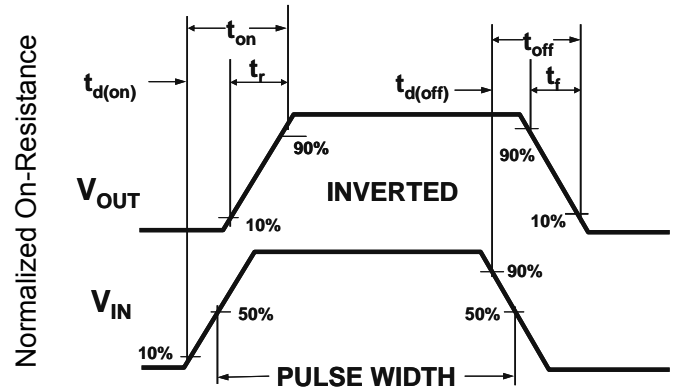


Figure 2: Switching Waveforms

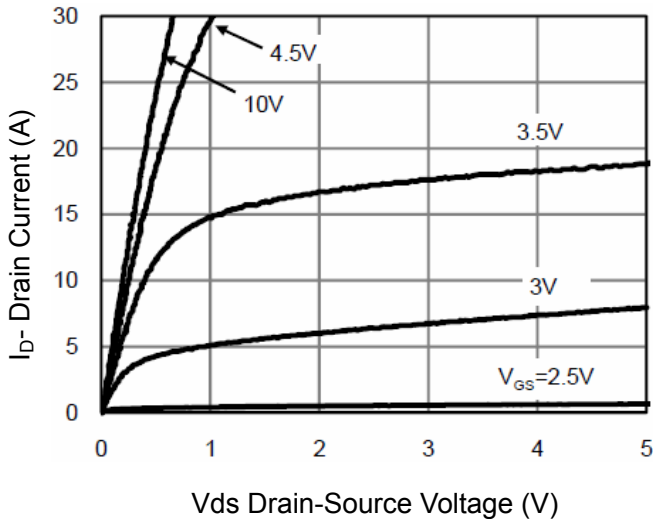


Figure 3 Output Characteristics

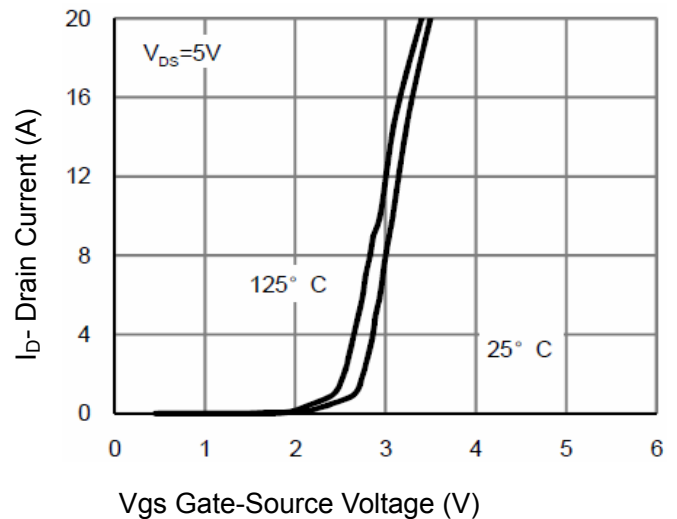


Figure 4 Transfer Characteristics

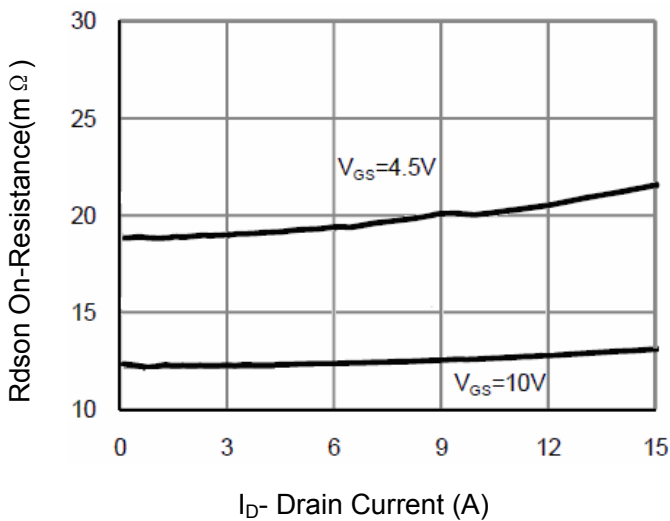


Figure 5 Drain-Source On-Resistance

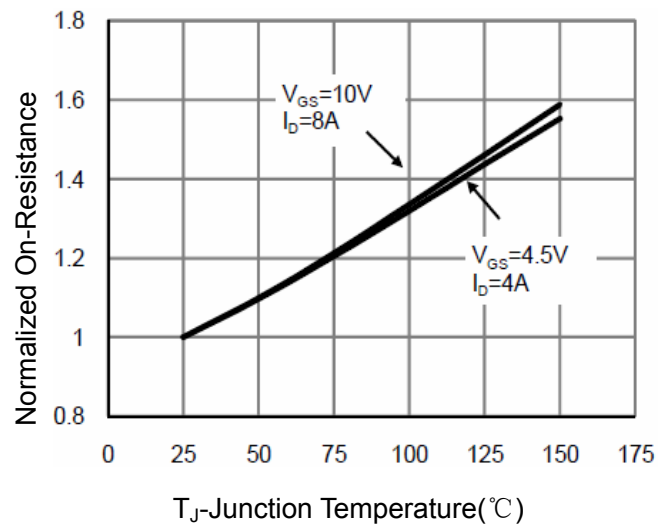
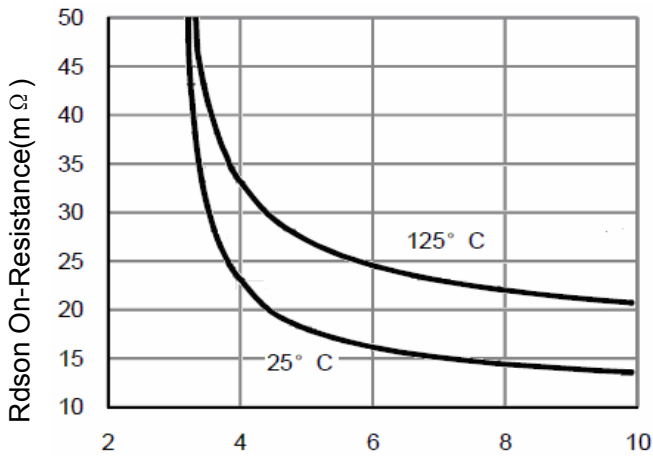
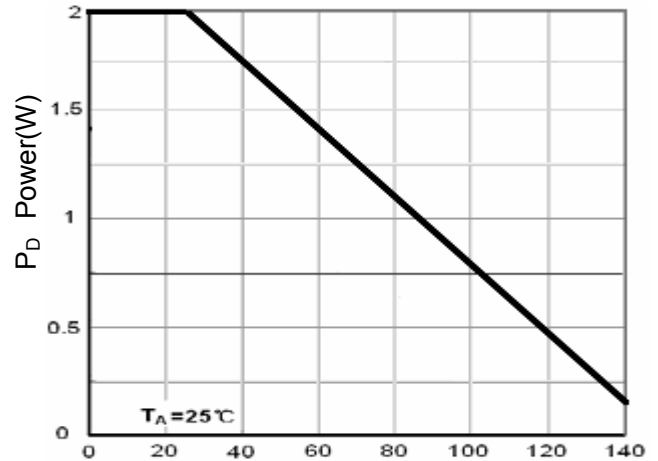


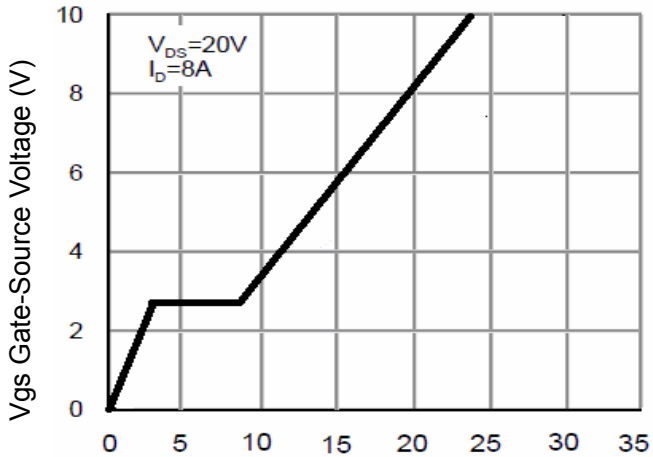
Figure 6 Drain-Source On-Resistance



Vgs Gate-Source Voltage (V)
Figure 7 Rdson vs Vgs



T_J-Junction Temperature(°C)
Figure 8 Power Dissipation



Qg Gate Charge (nC)
Figure 9 Gate Charge

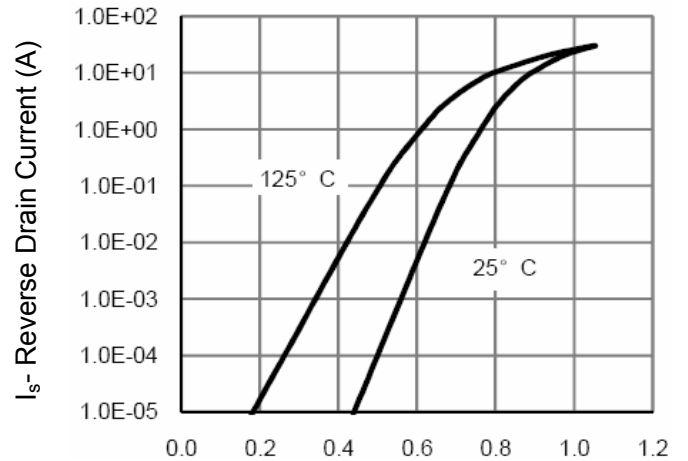
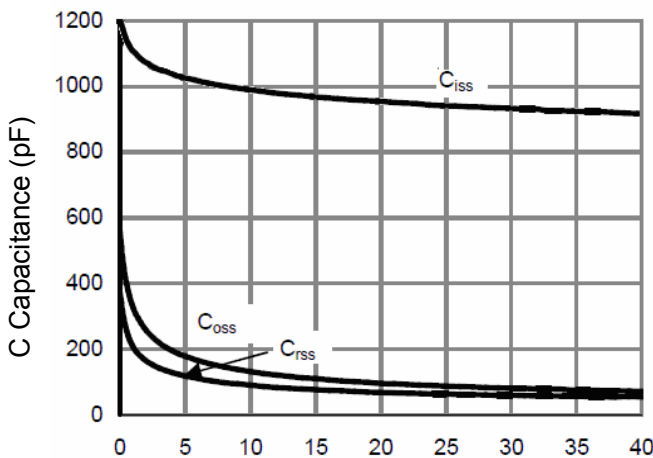


Figure 10 Source- Drain Diode Forward



Vds Drain-Source Voltage (V)
Figure 11 Capacitance vs Vds

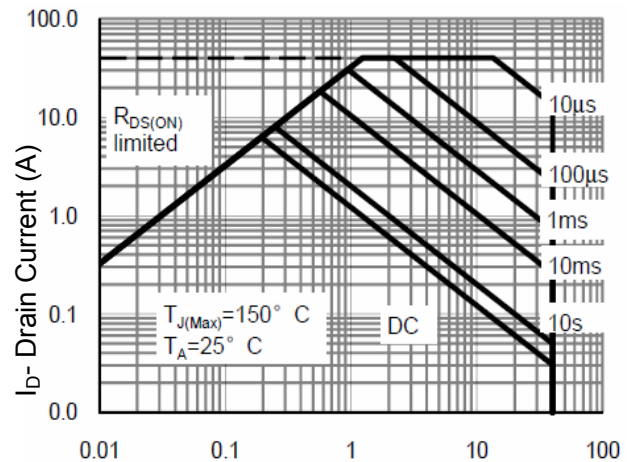


Figure 12 Safe Operation Area

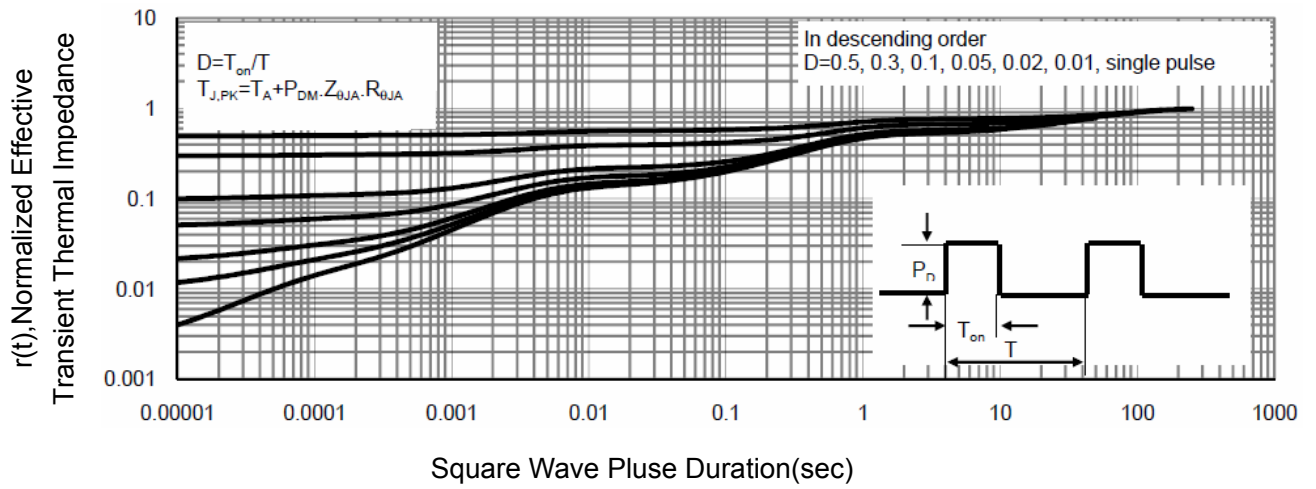
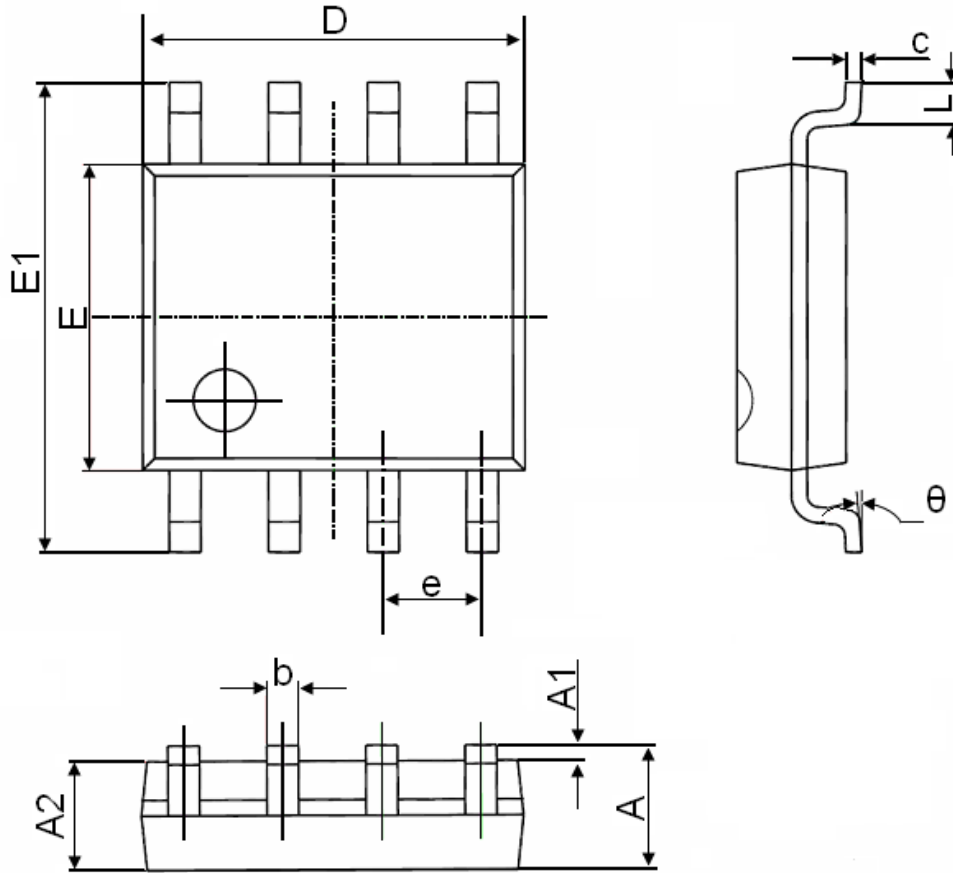


Figure 13 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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