



200V 1A Half Bridge Driver

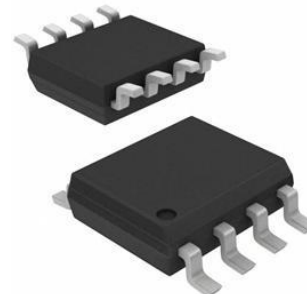
General description:

The XJNG2103 is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 200 V.

Features:

- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 6 V to 18 V
- 3.3 V input logic compatible
- Typically output Source/Sink current capability 1A/1A

Package top view



SOIC-8

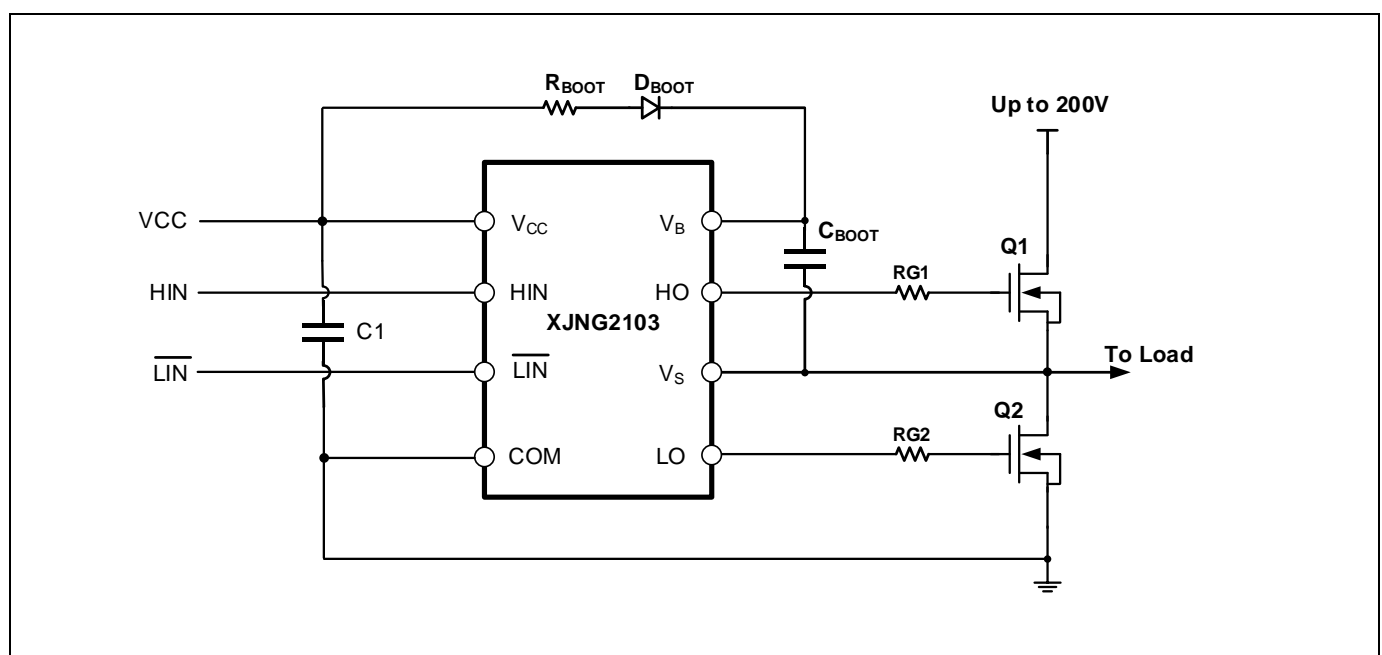
Application

- Switch Mode Power Supplies (SMPS)
- Small and medium- power motor driver
- Power MOSFET driver
- Half / Full-Bridge Power Converters
- Any Complementary Drive Converters

Package Marking and Ordering Information

Device	Order code	Device Package	Device Marking
XJNG2103	XJNG2103	SOIC8	XJNG2103

Typical Application Circuit





Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply	-0.3	225	V
V _S	High side floating supply return	V _B - 25	V _B + 0.3	V
V _{HO}	High side gate drive output	V _S -0.3	V _B + 0.3	V
V _{CC}	Low side and main power supply	-0.3	25	V
V _{LO}	Low side gate drive output	-0.3	V _{CC} + 0.3	V
V _{IN}	Logic input of HIN & $\overline{\text{LIN}}$	-0.3	V _{CC} + 0.3	V
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns
P _D	Package Power Dissipation @ TA ≤25°C (SOIC-8)	—	0.625	W
R _{thJA}	Thermal Resistance Junction to Ambient (SOIC-8)	—	200	°C/W
T _J	Junction Temperature	—	150	°C
T _S	Storage Temperature	-55	150	°C
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	°C
ESD	HBM Model	1500	—	V
	CDM Model	500	—	V

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply	V _S + 6	V _S + 20	V
V _S	High side floating supply return	-6	200	V
V _{HO}	High side gate drive output	V _S	V _B	V
V _{CC}	Low side and main power supply	6	20	V
V _{LO}	Low side gate drive output	0	V _{CC}	V
V _{IN}	Logic input of HIN & $\overline{\text{LIN}}$	0	V _{CC}	V
T _A	Ambient temperature	-40	125	°C

Dynamic Electrical Characteristics

VBIAS (V_{CC}, V_B) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified

Symbol	Definition	Min.	Typ.	Max.	Units
t _{ON}	Turn on propagation delay	—	150	250	ns
t _{OFF}	Turn off propagation delay	—	140	250	ns
MT	Delay matching time (t _{ON} , t _{OFF})	—	--	50	ns
DT	Dead time	—	200	--	ns
t _R	Turn on rising time	—	50	100	ns
t _F	Turn off falling time	—	40	100	ns

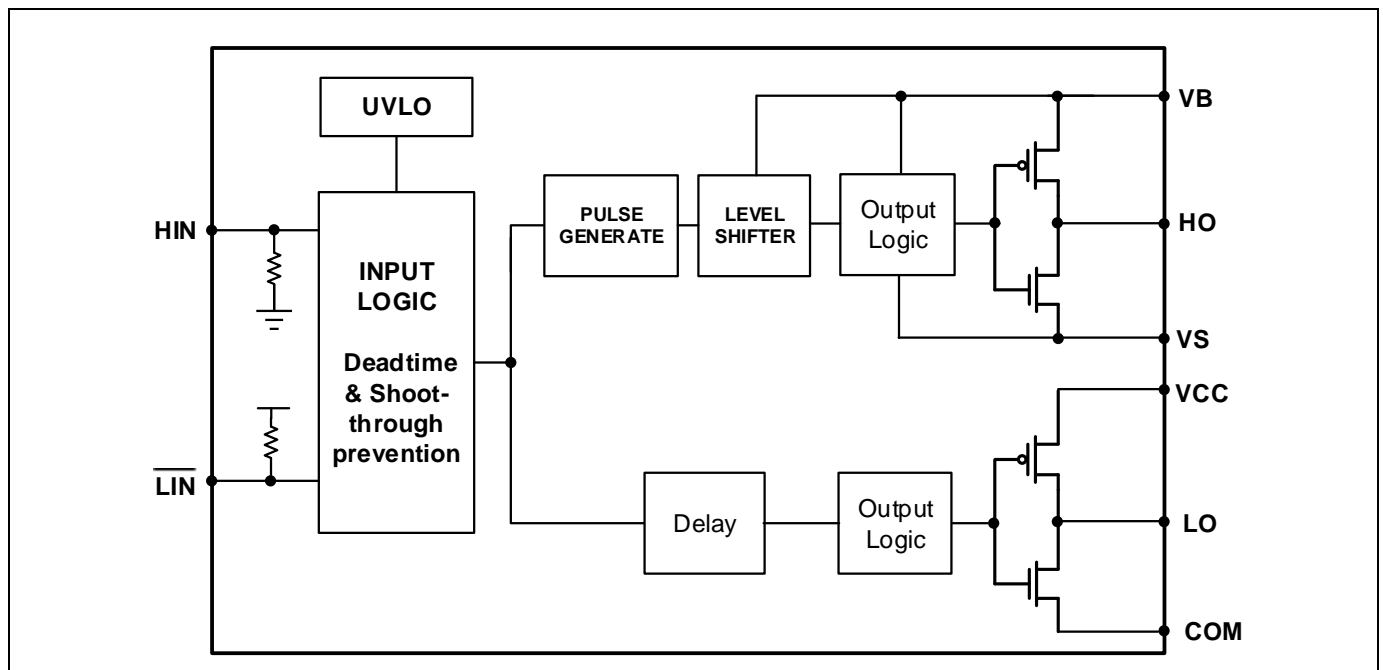


Static Electrical Characteristics

VBIAS (VCC, VBS) = 15V, CL = 1000 pF and TA = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units
V _{IH}	High level input threshold voltage	2.5	—	—	V
V _{IL}	Low level input threshold voltage	—	—	0.8	V
V _{OH}	High level output voltage drop, V _{BIAS} - V _O	—	—	0.2	V
V _{OL}	Low level output voltage drop, V _O	—	—	0.1	V
I _{LK}	High-side floating supply leakage current	—	—	50	μA
I _{QBS}	Quiescent V _{BS} supply current	—	40	120	μA
I _{QCC}	Quiescent V _{CC} supply current	—	160	280	μA
I _{IN+}	Logic “1” input bias current (HIN “1” & LIN “0”)	—	10	20	μA
I _{IN-}	Logic “0” input bias current (HIN “0” & LIN “1”)	—	15	30	μA
V _{CCUV+}	VCC supply undervoltage positive going threshold	—	5.5	—	V
V _{CCUV-}	VCC supply undervoltage negative going threshold	—	5.0	—	V
I _{O+}	Output High short circuit pulsed current	—	1	—	A
I _{O-}	Output low short circuit pulsed current	—	1	—	A

Function Block Diagram





Pin Configuration

Pin No.	Pin Name	Pin Function
1	V _{CC}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output, out of phase with LIN
6	V _S	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V _B	High side floating supply

Function Timing Diagram

Input and output timing waveform

Cross Conduction Prevention Delay Time Waveform Definition

Switching Time Waveform Definition

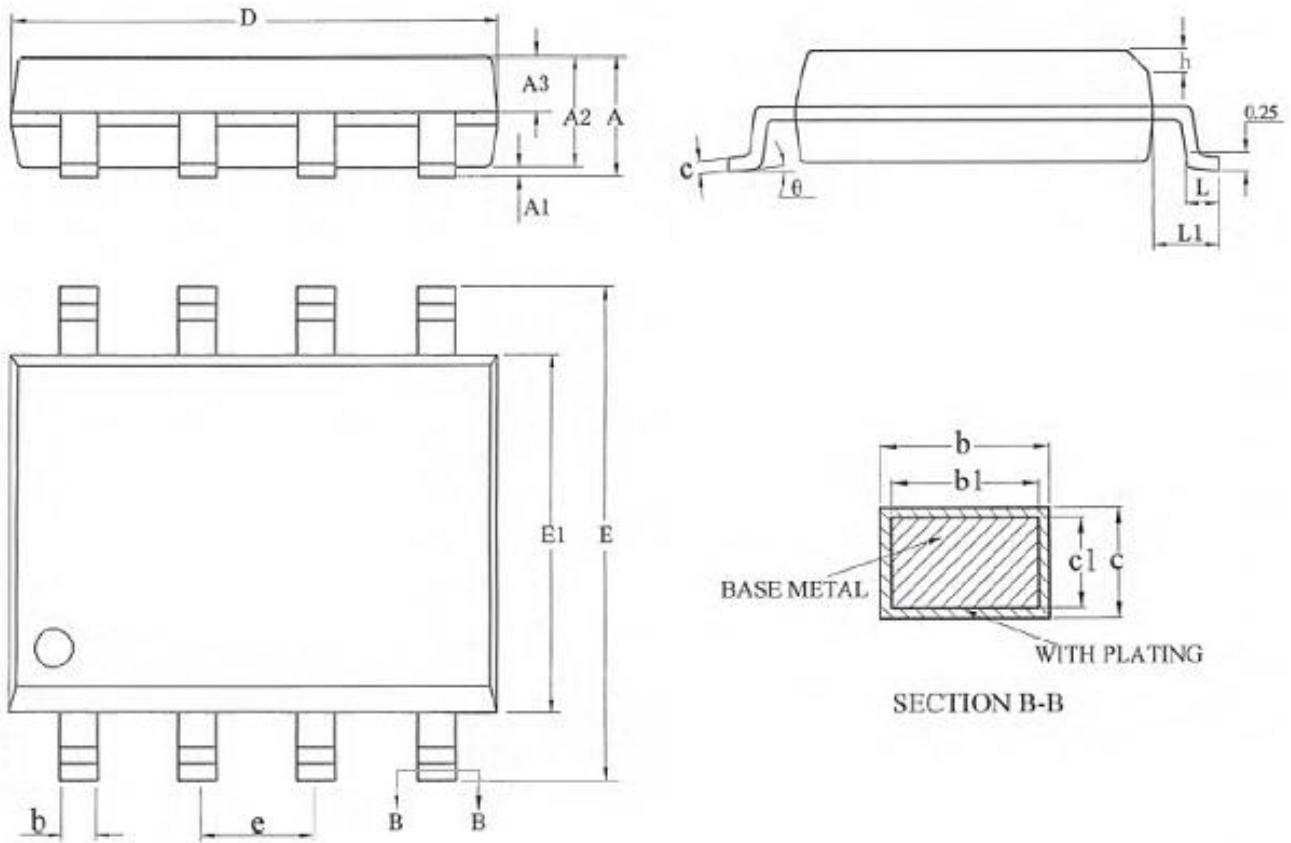


Package Information

SOIC-8 Package Dimensions

Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

SOIC-8 Package Outlines





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