NETLIST

Datasheet

Secure Digital (SD) Memory Card
256MB to 2GB
NLSDxxx11x-1xxHAAxxxxx

1. Overview

Netlist, the pioneer in the development of high-density memory subsystems, is proud to offer the Netlist High Performance SD Card, which provides 256MB to 2GB of non-volatile storage. The Netlist solution uses a controller that provides a fully compatible SD or SPI interface to the Flash memory. Netlist's SD Card is the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, and temperature. Because there are no moving parts to service or maintain, SD Cards are a reliable alternative to a mechanical hard disk drive for high availability and mission critical applications. While the inherent ruggedness and reliability of solid state storage relative to rotating hard drives is intuitive, new OEM applications are emerging due to the low cost per usable megabyte. Most applications that use embedded operating systems do not have large data storage requirements, and therefore a cost savings can be realized when using this robust media.

The Netlist Industrial Grade SD Card provides a high capacity data storage that electrically complies with the SD Card Association standard. The on-card intelligent controller manages interface protocols, data storage and retrieval as well as Error Correcting Code (ECC), wear leveling, detects handling and diagnostics, power management and control.

2. Features

- Up to 2GB of mass storage data utilizing SLC Flash technology
- Non-Volatile Storage and Completely Solid State (No Moving Parts)
- SD Card standards rev. 1.01, 1.10 compatible
- Industrial and Commercial Temperature Operating range
- Form Factor: SD Card 1.1
- SD and SPI Modes compatible
- 1.8V or 3.3V Power Supply Support
- RS-ECC Engine with 3-byte correction, 3-byte detection
- Static Wear-Leveling Algorithm
- RoHS-6 compliant (Pb-free)

3. Ordering Information

256MB to 2GB Secure Digital (SD) Memory Card Part Number: NLSDxxx11x-1xxHAAxxxxx		
Density	**Commercial Temperature Part Number**	**Industrial Temperature Part Number**
256MB	NLSD02511C-1SSHAA41110	NLSD02511I-1SSHAA41110
512MB	NLSD05111C-1SSHAA41110	NLSD05111I-1SSHAA41110
1GB	NLSD01G11C-1SSHAA42120	NLSD01G11I-1SSHAA42120
2GB	NLSD02G11C-1SSHAA44140	NLSD02G11I-1SSHAA44140

4. SD Part Number Decoder

N	L	*a*	*b*	*c*	*d*	*e*	*f*	*g*	*h*	-	*p*	*q*	*r*	*s*	*t*	*u*	*v*	*w*	*x*	*y*	*z*
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

Position	**Property**	**Definitions**
1,2	Netlist Code	NL = Netlist
3,4	Product Type	SD = Secure Digital
5,6,7	Memory Capacity	025 = 256MB 051 = 512MB 01G = 1GB 02G = 2GB
8	Feature Set A	1 = SD1.1 when 9 = 1
9	Feature Set B	1 = SD1.1 when 8 = 1
10	Temperature Range	I = Industrial (-40°C to +85°C) C = Commercial (0°C to +70°C)
11	"-"	-
12	Flash Controller	1 = S4
13	Flash Manufacturer	S = Samsung
14	Flash Type	S = SLC M = MLC P = Pseudo-SLC (pSLC)
15	Mount	H = Horizontal
16,17	OEM Code	AA = Standard Product
18	Flash Die Geometry	4 = 4x nm 2 = 2x nm 3 = 3x nm 1 = 1x nm
19	Number of CE per Flash Location	1 = 1 CE per Flash Location 4 = 4 CE per Flash Location 2 = 2 CE per Flash Location 8 = 8 CE per Flash Location
20	Number of Flash Location(s)	1 = 1 Flash Location 4 = 4 Flash Locations 2 = 2 Flash Locations 8 = 8 Flash Locations
21	Number of Die per Flash Location	1 = 1 Die per Flash Location 4 = 4 Die per Flash Location 2 = 2 Die per Flash Location 8 = 8 Die per Flash Location
22	Special Feature	0 = None (Standard Product)

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5. Product Specifications

5.1. SD Card Form-Factor

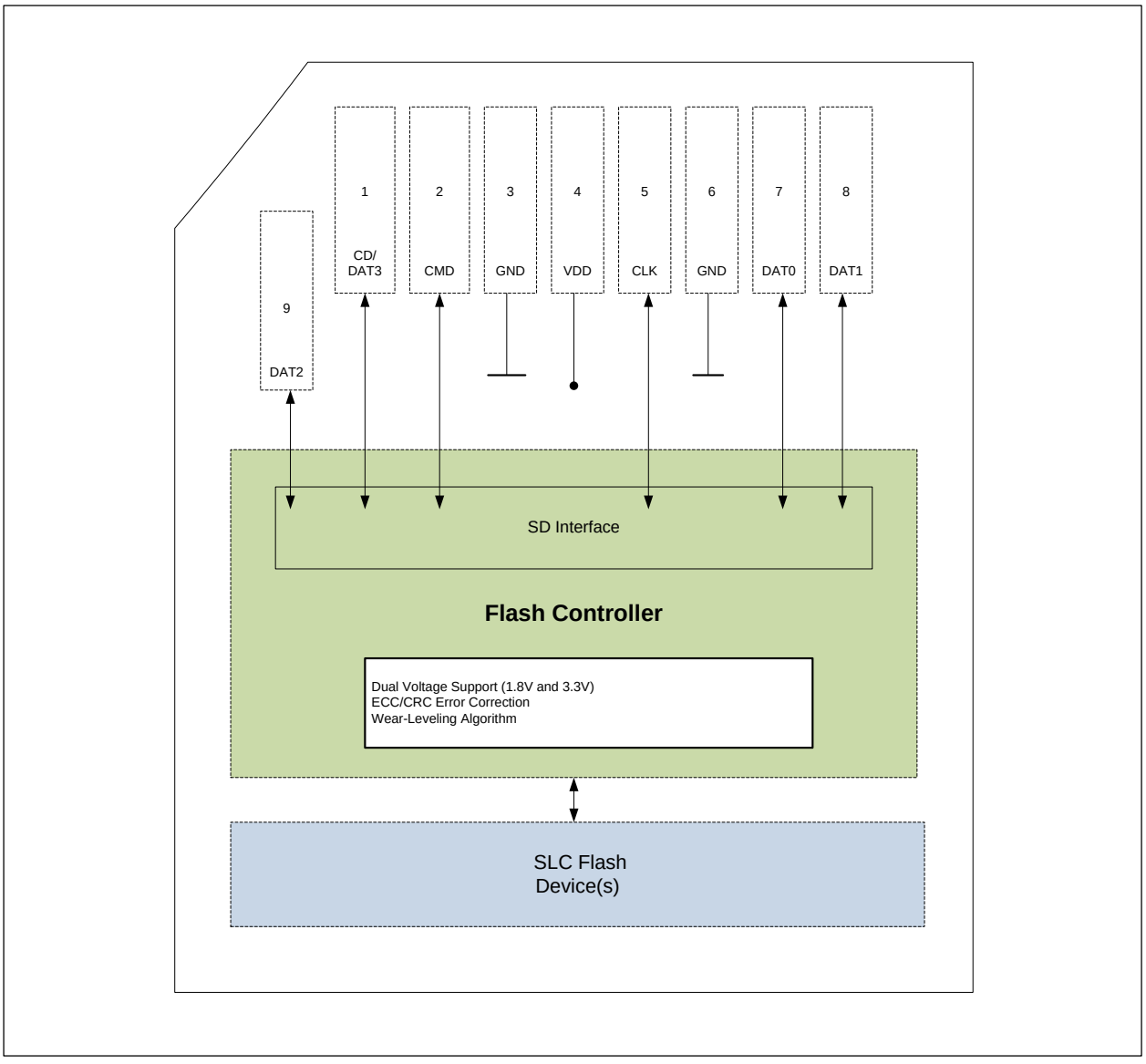
The host is connected to the SD Card using a standard 9-pin connector.

Table 1: SD Card Dimensions

Length:	32.00 ± 0.10 mm (1.260”)
Width:	24.0 ± 0.10 mm (0.945”)
Thickness Including Label Area:	2.10 ± 0.15 mm Max (0.083”)

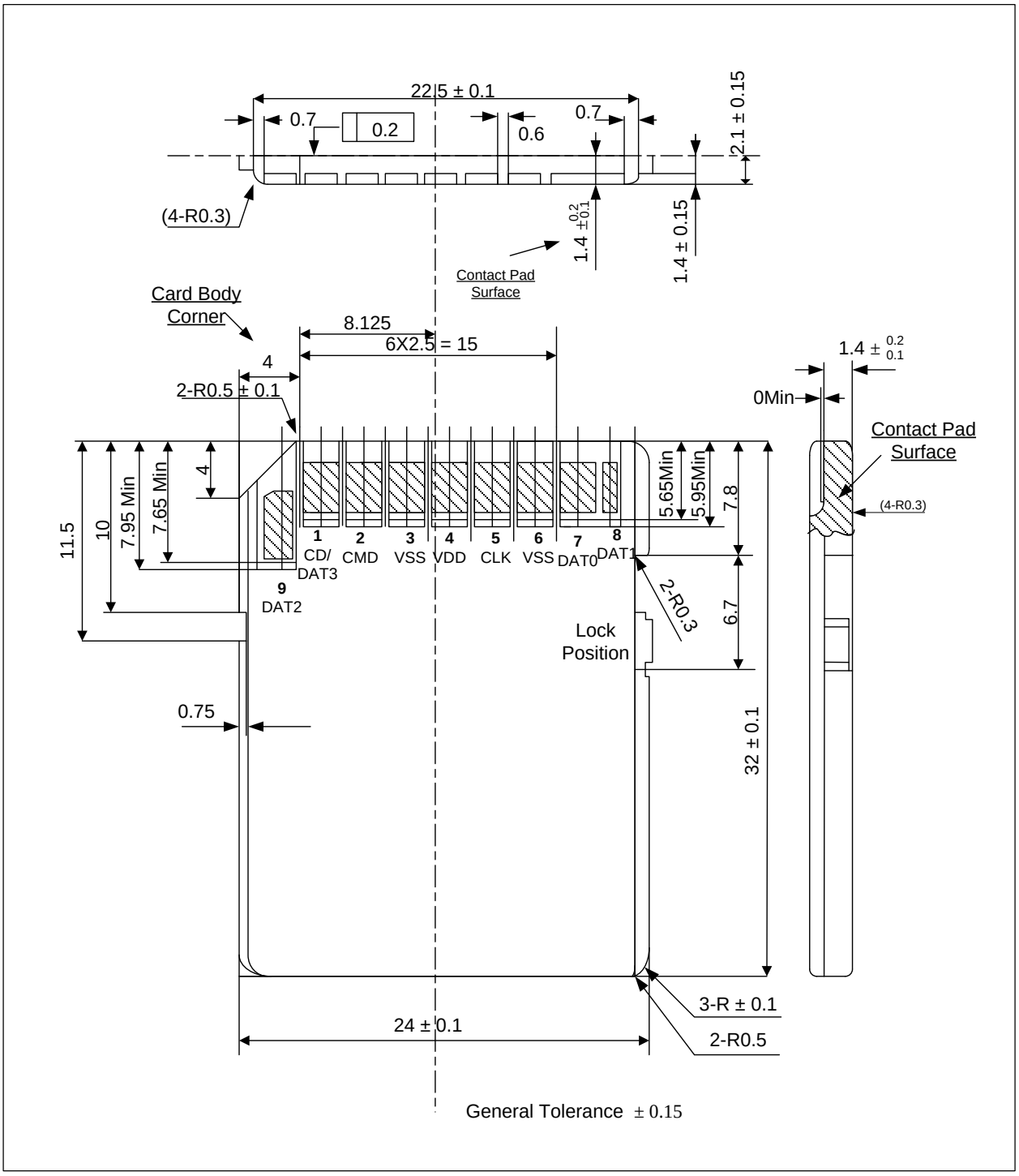
6. Block Diagram

Figure 1: Netlist SD Card Configuration Functional Block Diagram



7. Physical Diagram

Figure 2: Physical Diagram



8. Reliability & Durability

Table 2: Flash Controller

Temperature	Commercial Operation: 0°C to 70°C Industrial Operation: -40°C to 85°C
Vibration	15 G (Target spec; currently under test)
Acoustic Noise	0 dB
Shock	1000 G
Humidity	95% max. non-condensing
ESD Level	Contact Pads: Up to 4kV (pending 8kV characterization) Coupling Plane Discharge: Up to 8 kV Air Discharge: Up to 15kV

8.1. Wear Leveling for Flash Memory

The Netlist Industrial Grade SD Card makes use of the most advanced flash wear leveling and bad block management techniques. Wear leveling is performed with the use of reserved buffer blocks. "Wear leveled" blocks are swapped with replacement blocks that have the fewest erase cycles. Bad block management ensures that defective blocks created during device operation are mapped out and never accessed. In this manner, the life of the entire device is extended.

9. System Performance

Table 3: Data Transfer Rates (Controller Frequency @ 50MHz)[1]

Capacity	# of Flash Chips	Read	Write	Random Read	Random Write
256MB	1	18.188 MB/s	11.696 MB/s	17.700 MB/s	6.150 MB/s
512MB	1	18.188 MB/s	11.596 MB/s	17.700 MB/s	6.037 MB/s
1GB	2	18.188 MB/s	14.712 MB/s	17.700 MB/s	7.754 MB/s
2GB	4	18.188 MB/s	12.241 MB/s	17.700 MB/s	6.454 MB/s

[1] Based on initial testing; actual performance may vary on system and environmental factors.

10. Pin Assignment

Table 4: Pin Assignment

Pin Num	SD Card Memory Mode			SPI Mode		
	Signal Name	Type[2]	Description	Signal Name	Type[2]	Description
1	CD, DAT3[3]	I/O; PP[4]	Card Detect, Data Line[3]	CS#	Input[4]	Chip Select; Active Low
2	CMD	PP	Command	DI	Input	Data In
3	V_{SS1}	Supply	Ground	V_{SS1}	Supply	Ground
4	V_{DD}	Supply	Voltage Supply	V_{DD}	Supply	Voltage Supply
5	CLK	Input	Clock	SCLK	Input	Clock
6	V_{SS2}	Supply	Ground	V_{SS2}	Supply	Ground
7	DAT0	I/O; PP	Data Line [0]	DO	Output; PP	Data Out
8	DAT1	I/O; PP	Data Line [1]	-	-	Reserved
9	DAT2	I/O; PP	Data Line [2]	-	-	Reserved

[2] PP = I/O using push-pull drivers.
[3] The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
[4] After power up this line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

11. SD Operation

The SD Card provides applications with a low cost mass storage device, implemented as a removable card that supports high security level for copyright protection and a compact, easy-to-implement interface.

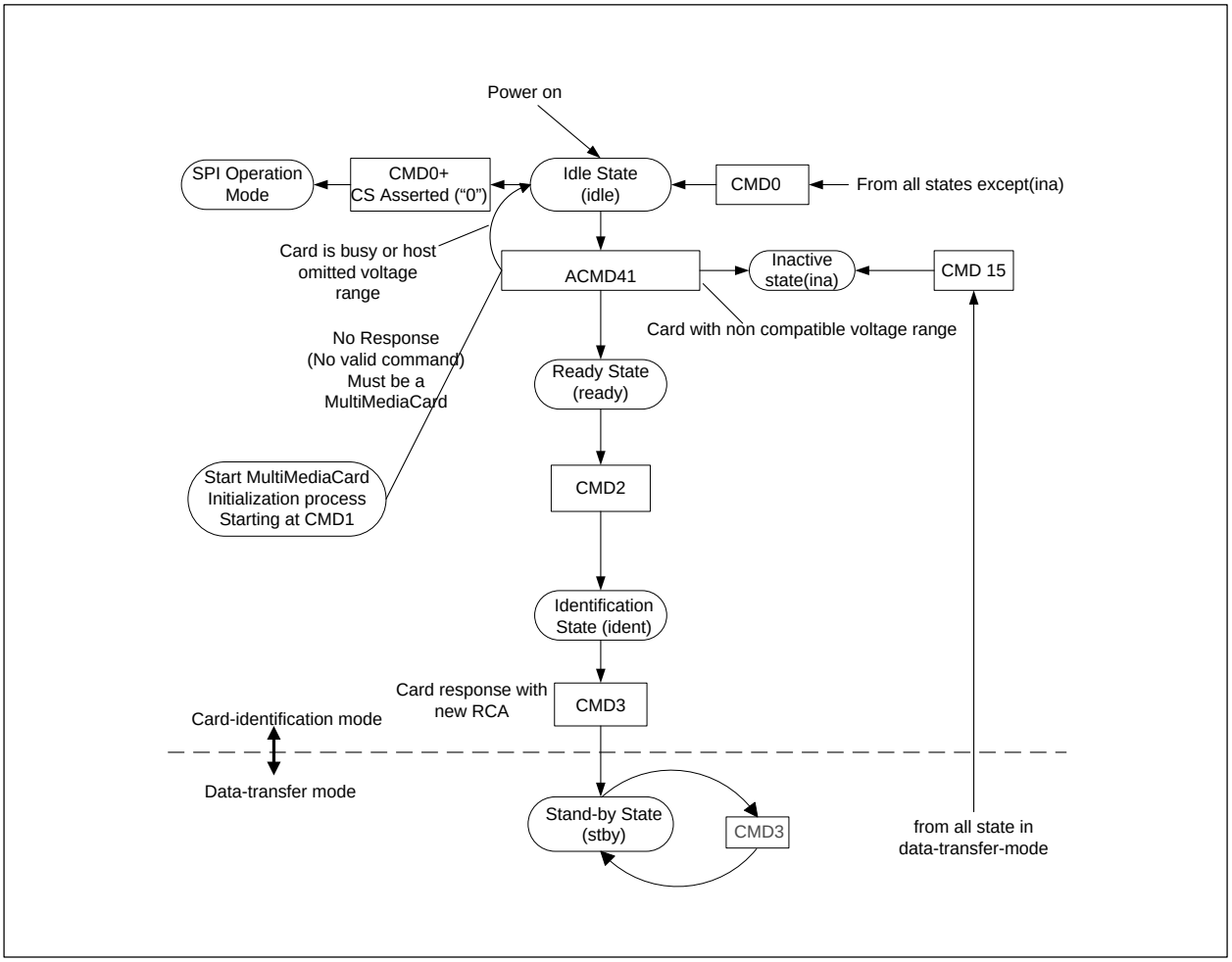
The SD Card supports two communication protocols: SD and SPI. Applications can choose either mode of operation. Mode selection is transparent to the host as the card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. Therefore, hosts that use only one mode of communication do not have to be aware of the other.

11.1. Card Identification Mode

The host will be in card identification mode after reset and while it is looking for new cards on the bus. Cards will be in this mode after reset until the SEND_RCA command (CMD3) is received.

While in card identification mode the host resets all the cards that are in card identification mode, validates operation voltage range, identifies cards and asks them to publish Relative Card Address (RCA). This operation is done to each card separately on its own CMD line. All data communication in the Card Identification Mode uses the command line (CMD) only.

Figure 3: SD Card State Diagram (Card Identification Mode)



11.2. Data Transfer Mode

Cards will enter data transfer mode once their RCA is first published. The host will enter data transfer mode after identifying all the cards on the bus.

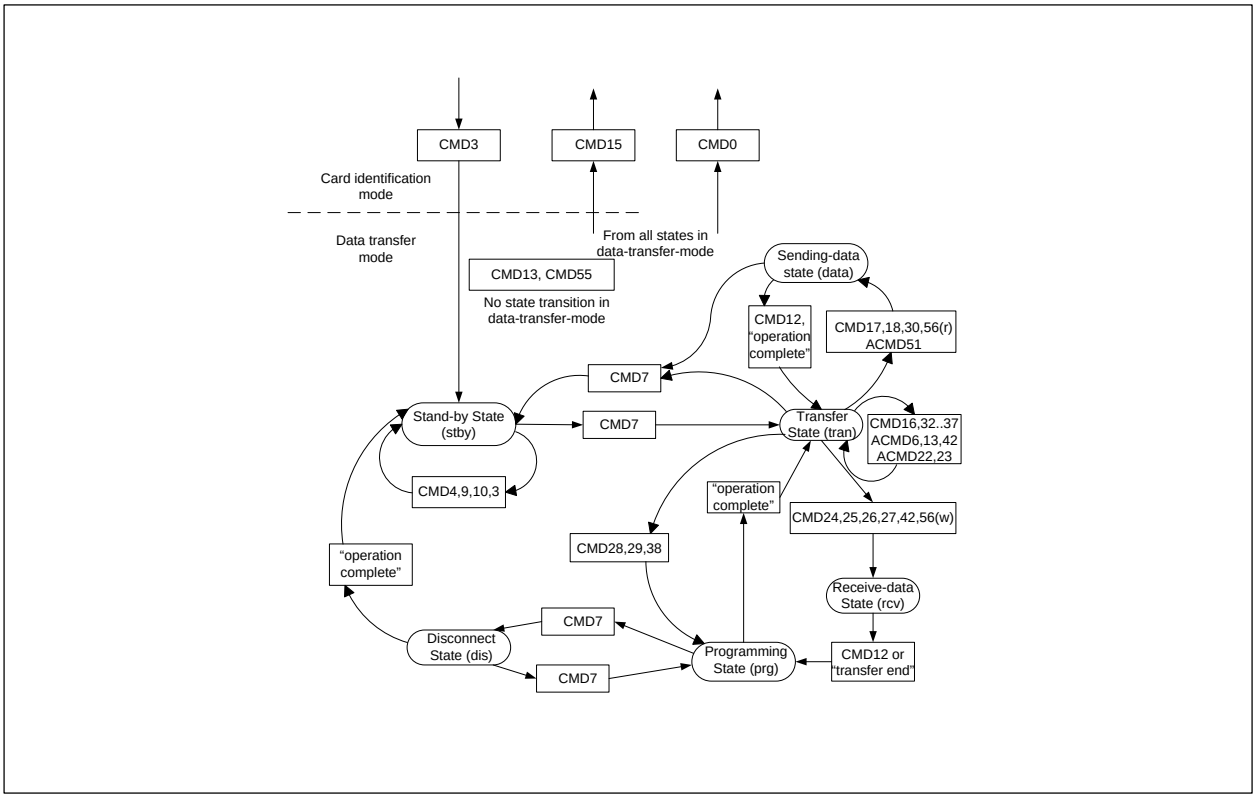
Until the end of Card Identification Mode the host must remain at fOD frequency because some cards may have operating frequency restrictions during the card identification mode. In Data Transfer Mode the host may operate the card in fPP frequency range. The host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g. block length, card storage capacity, etc.

The broadcast command SET_DSR (CMD4) configures the driver stages of all identified cards. It programs their DSR registers corresponding to the application bus layout (length) and the number of cards on the bus and the data transfer frequency. The clock rate is also switched from fOD to fPP at that point. SET_DSR command is an option for the card and the host.

CMD7 is used to select one card and put it into the Transfer State. Only one card can be in the Transfer State at a given time. If a previously selected card is in the Transfer State its connection with the host is released and it will move back to the Stand-by State. When CMD7 is issued with the reserved relative card address “0x0000”, all cards are put back to Stand-by State (Note that it is the responsibility of the Host to reserve the RCA=0 for card de-selection). This may be used before identifying new cards without resetting other already registered cards. Cards which already have an RCA do not respond to identification commands (CMD41, CMD2, CMD3) in this state.

All data communication in the Data Transfer Mode is point-to point between the host and the selected card (using addressed commands). All addressed commands get acknowledged by a response on the CMD line.

Figure 4: SD Card State Diagram (Data Transfer Mode)



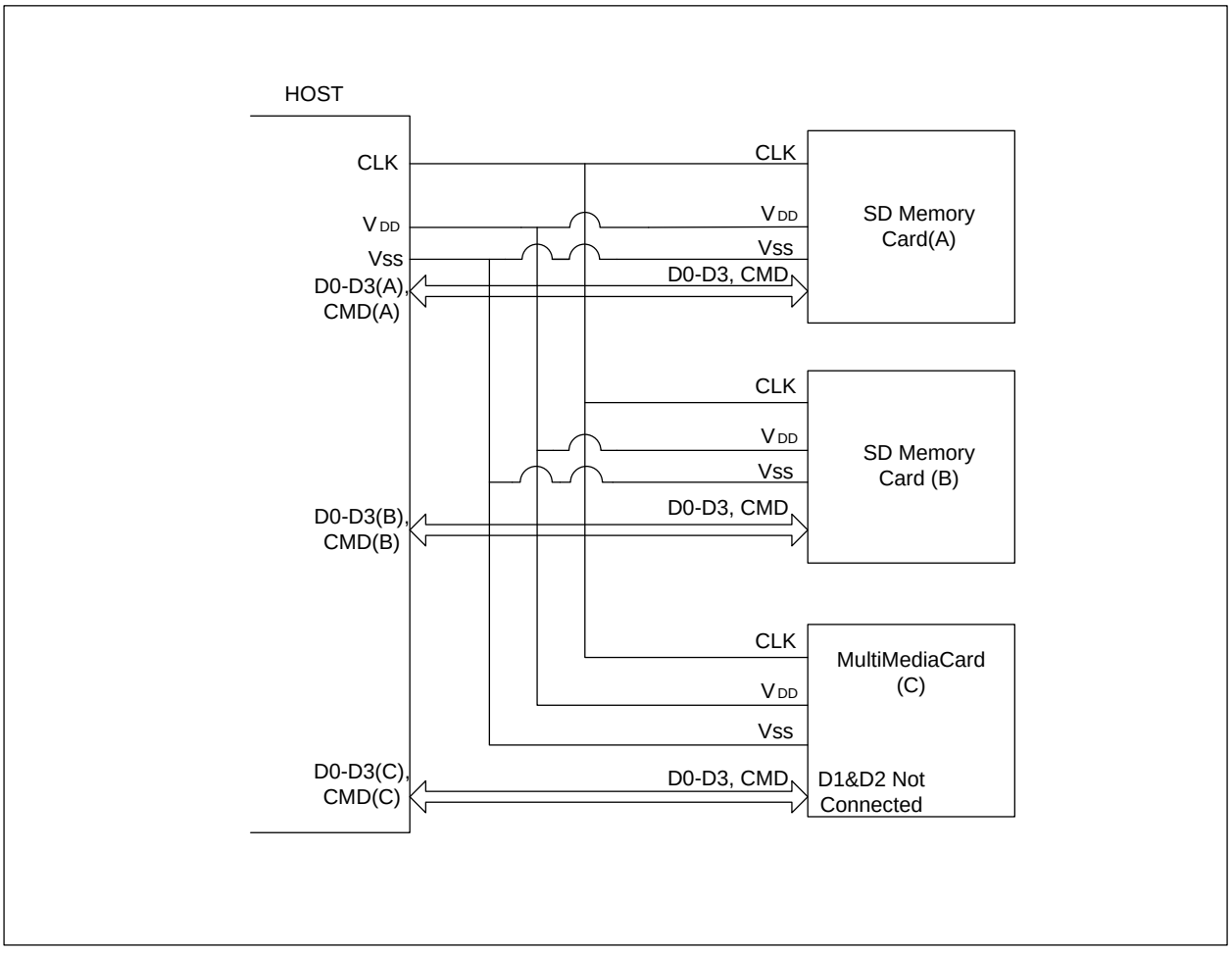
11.3. SD Mode

The SD Memory Card bus has a single master (host), multiple slaves (cards), synchronous star topology (see figure below). Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0 - DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.

Communication over the SD bus is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token that is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

Figure 5: SD System Bus Topology



11.4. SPI Mode

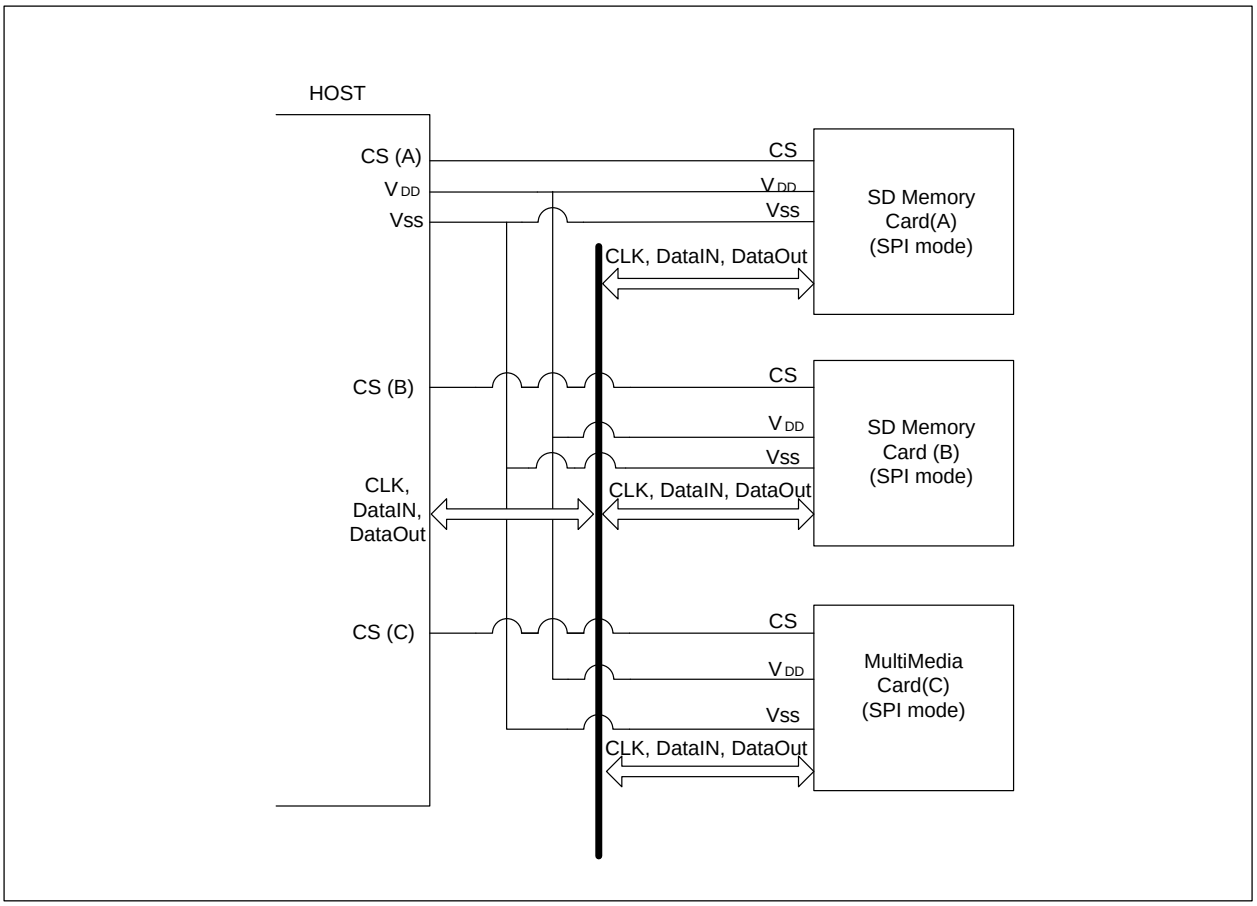
The Serial Peripheral Interface (SPI) mode is a subset of the SD Memory Card protocol, designed to communicate with a SPI channel, commonly found in microcontrollers. The interface is selected during the first reset command after power up (CMD0) and cannot be changed once the part is powered on.

The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses a subset of the SD Memory Card protocol and command set. The advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance of the SPI mode versus SD mode (e.g. Single data line and hardware CS signal per card).

While the SD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.

Similar to the SD Memory Card protocol, the SPI messages consist of command, response and datablock tokens. The host starts every bus transaction by asserting the CS signal low and the selected card always responds to the command. When the card encounters a data retrieval problem in a read operation, it will respond with an error response (which replaces the expected data block). Additionally, every data block sent to the card during write operations will be responded with a data response token.

Figure 6: SPI System Bus Topology



11.5. Mode Selection

The SD Card is powered up in the SD mode. It will enter SPI mode if the CS signal is asserted (active low) during the reception of the reset command (CMD0) and the card is in idle_state. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required, the card will switch to SPI and respond with the SPI mode R1 response. The only way to return to the SD mode is by entering the power cycle. In SPI mode, the SD Card protocol state machine in SD mode is not observed. All the SD Card commands supported in SPI mode are always available.

11.6. SD Card Register Descriptions

Table 5: SD Card Register Descriptions

Name	Width	Description
CID	128	Card Identification Number; card individual number for identification
RCA	16	Relative Card Address; local system address of a card, dynamically suggested by the card and approved by the host during initialization
DSR	16	Driver Stage Register; to configure the card's output drivers
CSD	128	Card Specific Data; information about the card operation conditions
SCR	64	SD Configuration Register; information about the SD Memory Card's Special Features capabilities
OCR	32	Operation Conditions Register
SSR	512	SD Status; information about the card proprietary features
CSR	32	Card Status; information about the card status

11.7. Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have a unique identification number.

Table 6: CID Bit Description

Bits	Name	Description
[127:120]	MID	Manufacturer ID
[119:104]	OID	OEM/Application ID
[103:64]	PNM	Product Name
[63:56]	PRV	Product Revision
[55:24]	PSN	Product Serial Number
[23:20]	-	Reserved
[19:8]	MDT	Manufacturing Date
[7:1]	CRC	CRC7 Checksum
[0]	-	Reserved; High(1)

11.8. Operation Conditions Register (OCR)

The 32-bit operation conditions register stores the VDD voltage profile of the card. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. The OCR register shall be implemented by the cards which do not support the full operating voltage range of the SD Memory Card bus, or if the card power up extends the definition in the timing diagram.

Table 7: OCR Bit Description

Bits	Description/Value
[31]	Card Power Up Status Bit (busy)[5]
[30:24]	Reserved
[23]	3.5-3.6
[22]	3.4-3.5
[21]	3.3-3.4
[20]	3.2-3.3
[19]	3.1-3.2
[18]	3.0-3.1
[17]	2.9-3.0
[16]	2.8-2.9
[15]	2.7-2.8
[14]	2.6-2.7
[13]	2.5-2.6
[12]	2.4-2.5
[11]	2.3-2.4
[10]	2.2-2.3
[9]	2.1-2.2
[8]	2.0-2.1
[7]	1.9-2.0
[6]	1.8-1.9
[5]	1.7-1.8
[4]	1.6-1.7
[3:0]	Reserved

The supported voltage range is coded as shown in table above. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

[5] Valid only when the card power up status bit is set.

11.9. Card-Specific Data Register (CSD)

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

Table 8: CSD Version 1.0 for SD Card Densities from 128MB to 2GB

Bits	Name	R/W	Value	Description
[127:126]	CSD_STRUCTURE	R	00b	CSD structure
[125:120]	Reserved	R	00 0000b	Reserved
[119:112]	TAAC	R	xxh	Data Read Access-Time-1
[111:104]	NSAC	R	xxh	Data Read Access-Time-2 in CLK cycles (NSAC*100)
[103:96]	TRAN_SPEED	R	32h or 5Ah	Max. Data Transfer Rate
[95:84]	CCC	R	01x11011010 1b	Card Command Classes
[83:80]	READ_BL_LEN	R	xh	Max. Read Data Block Length
[79]	READ_BL_PARTIAL	R	1b	Partial Blocks for Read Allowed
[78]	WRITE_BLK_MISALIGN	R	xb	Write Block Assignment
[77]	READ_BLK_MISALIGN	R	xb	Read Block Assignment
[76]	DSR_IMP	R	xb	DSR Implemented
[75:74]	Reserved	R	00b	Reserved
[73:62]	C_SIZE	R	xxxh	Device Size
[61:59]	VDD_R_CURR_MIN	R	xxxb	Max. Read Current @ VDDmin
[58:56]	VDD_R_CURR_MAX	R	xxxb	Max. Read Current @ VDDmax
[55:53]	VDD_W_CURR_MIN	R	xxxb	Max. Write Current @ VDDmin
[52:50]	VDD_W_CURR_MAX	R	xxxb	Max. Write Current @ VDDmax
[49:47]	C_SIZE_MULT	R	xxxb	Device Size Multiplier
[46]	ERASE_BLK_EN	R	xb	Erase Single Block Enable
[45:39]	SECTOR_SIZE	R	xxxxxxxb	Erase Sector Size
[38:32]	WP_GRP_SIZE	R	xxxxxxxb	Write Protect Group Size
[31]	WP_GRP_ENABLE	R	xb	Write Protect Group Enable
[30:29]	Reserved	R	00b	Reserved
[28:26]	R2W_FACTOR	R	xxxb	Write Speed Factor
[25:22]	WRITE_BL_LEN	R	xxxxb	Max. Write Data Block Length
[21:21]	WRITE_BL_PARTIAL	R	xb	Partial Blocks for Write Allowed
[20:16]	Reserved	R	00000b	Reserved
[15]	FILE_FORMAT_GRP	R/W	xb	File Format Group
[14]	COPY	R/W	xb	Copy Flag (OTP)
[13]	PERM_WRITE_PROTECT	R/W	xb	Permanent Write Protection
[12]	TMP_WRITE_PROTECT	R/W	xb	Temporary Write Protection
[11:10]	FILE_FORMAT	R/W	xxb	File Format

Bits	Name	R/W	Value	Description
[9:8]	Reserved	R/W	00b	Reserved
[7:1]	CRC	R/W	xxxxxxxb	CRC
[0]	-	-	1b	Not Used; Always '1'

11.10. SD Card Configuration Register (SCR)

In addition to the CSD register, there is another configuration register named - SD Card Configuration Register (SCR). SCR provides information on SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bits. This register shall be set in the factory by the SD Memory Card manufacturer.

Table 9: SCR Register Content

Bits	Name	R/W	Value	Description
[63:60]	SCR_STRUCTURE	R	0h	SCR Structure
[59:56]	SD_SPEC	R	x	SD Memory Card – Spec. Version
[55]	DATA_STAT_AFTER_ERASE	R	x	Data Status After Erases
[54:52]	SD_SECURITY	R	x	SD Security Support
[51:48]	SD_BUS_WIDTHS	R	x	DAT Bus Widths Supported
[47:32]	Reserved	R	0	Reserved
[31:0]	-	R	0	Reserved for Manufacturer Usage

11.11. Driver Stage Register (DSR)

The Driver Stage Register (DSR) is a 16-bit register. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

11.12. Relative Card Address Register (RCA)

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

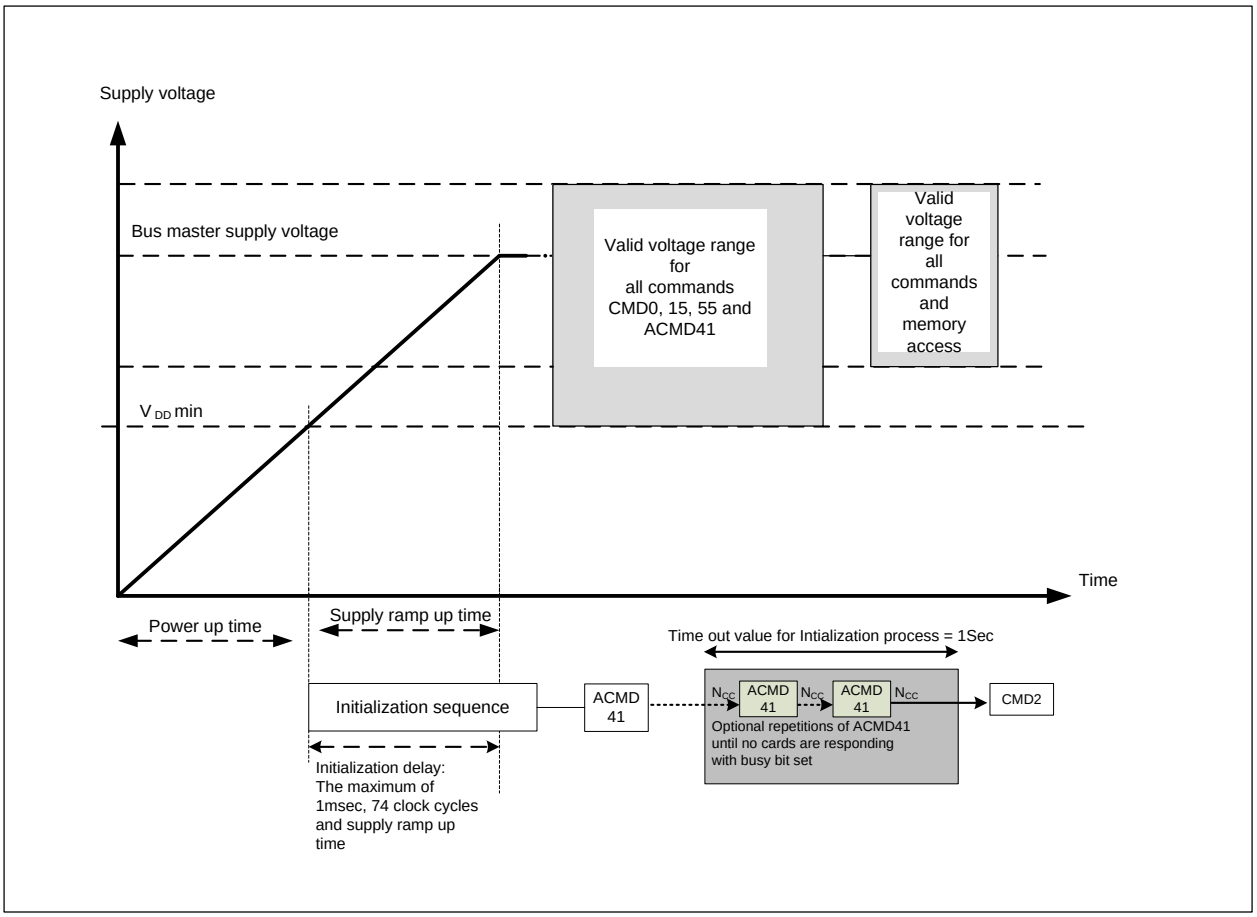
12. Power Schemes

12.1. Power Up

'Power up time is defined as voltage rising time from 0 volt to VDD min and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

- After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the idle state. During this state the SD Card ignores all bus transactions until ACMD41 is received (ACMD command type shall always precede with CMD55).
- ACMD41 is a special synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. Besides the operation voltage profile of the cards, the response to ACMD41 contains a busy flag, indicating that the card is still working on its power-up procedure and is not ready for identification. This bit informs the host that the card is not ready. The host has to wait (and continue to poll the cards, each one on his turn) until this bit is cleared. The maximum period of power up procedure of single card shall not exceed 1 second.
- Getting individual cards, as well as the whole SD Memory Card system, out of idle state is the responsibility of the bus master. Since the power up time and the supply ramp up time depend on application parameters such as the maximum number of SD Memory Cards, the bus length and the power supply unit, the host must ensure that the power is built up to the operating level (the level which will be specified in ACMD41) before ACMD41 is transmitted.
- After power up the host starts the clock and sends the initializing sequence on the CMD line. This sequence is a contiguous stream of logical '1's. The sequence length is the maximum of 1msec, 74 clocks or the supply-ramp-up-time; the additional 10 clocks (over the 64 clocks after what the card should be ready for communication) is provided to eliminate power-up synchronization problems.
- Every bus master shall have the capability to implement ACMD41. The ACMD41 shall be sent separately to each card accessing it through its own CMD line.

Figure 7: Power Up Sequence



12.2. Power Down

When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

13. DC Characteristics

Following Tables define all D.C. Characteristics for the SD Card.

Table 10: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Operating Temperature Range	T_{AMB}	-40°C to +85°C
Storage Temperature	$T_{STORAGE}$	-40°C to +125°C
Voltage on any pin with respect to GND.	V_{MAX}	-0.3V min. to V_{DD} + 0.3V max.

Table 11: Maximum Operating Current (at VDD = 3.3V)

Operation	Current	Units
Sleep Mode	0.2	mA
Initialization	70	mA
Default Mode	50	mA
Maximum	70	mA

Table 12: Bus Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	2.7	3.6	V
V_{DD}	SD Low Voltage Supply	1.6	3.6	V
V_{IL}	Input LOW Voltage	V_{SS}-0.3	0.25*V_{DD}	V
V_{IH}	Input HIGH Voltage	0.625* V_{DD}	V_{DD}+ 0.3	V
V_{OL}	Output LOW Voltage[6]		0.125* V_{DD}	V
V_{OH}	Output HIGH Voltage[6]	0.75* V_{DD}		V

Table 13: Leakage Current

Symbol	Parameter	Min	Max	Units
I_{LI}	Input Leakage Current	-10	+10	µA
I_{LO}	Output Leakage Current	-10	+10	µA

[6] at 100µA

14. AC Characteristics

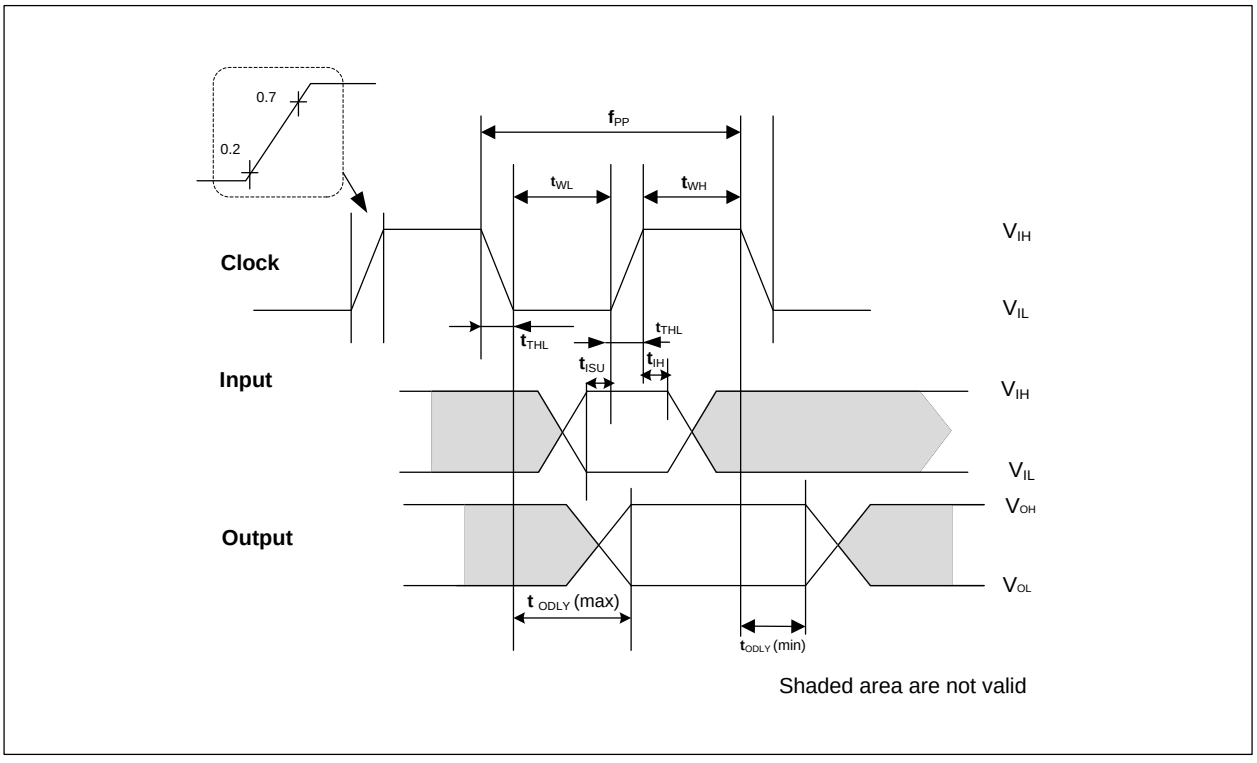
The SD card interface characteristics refer to the symbols used in the timing definition of the SD 1.1 standards.

14.1. SD Card Timing Specification (Low Speed Mode)

Table 14: Timing Specification (Low Speed Mode)

Symbol	Item	Min	Max	Units	Notes
f_{PP}	Clock, Data Transfer Mode	0	25	MHz	C_{CARD} ≤ 10pF
f_{OD}	Clock, Identification Mode	0	400	kHz	C_{CARD} ≤ 10pF
t_{WL}	Clock Low Time	10		ns	C_{CARD} ≤ 10pF
t_{WH}	Clock High Time	10		ns	C_{CARD} ≤ 10pF
t_{TLH}	Clock Rise Time		10	ns	C_{CARD} ≤ 10pF
t_{THL}	Clock Fall Time		10	ns	C_{CARD} ≤ 10pF
t_{ISU}	CMD, DAT Input Setup Time	5		ns	C_{CARD} ≤ 10pF
T_{IH}	CMD, DAT Input Hold Time	5		ns	C_{CARD} ≤ 10pF
t_{ODLY}	CMD, DAT output delay time during Data Transfer Mode	0	14	ns	C_{CARD} ≤ 40pF
t_{ODLY}	CMD, DAT output delay time during Identification Mode	0	50	ns	C_{CARD} ≤ 40pF

Figure 8: Timing Diagram (Low Speed Mode)

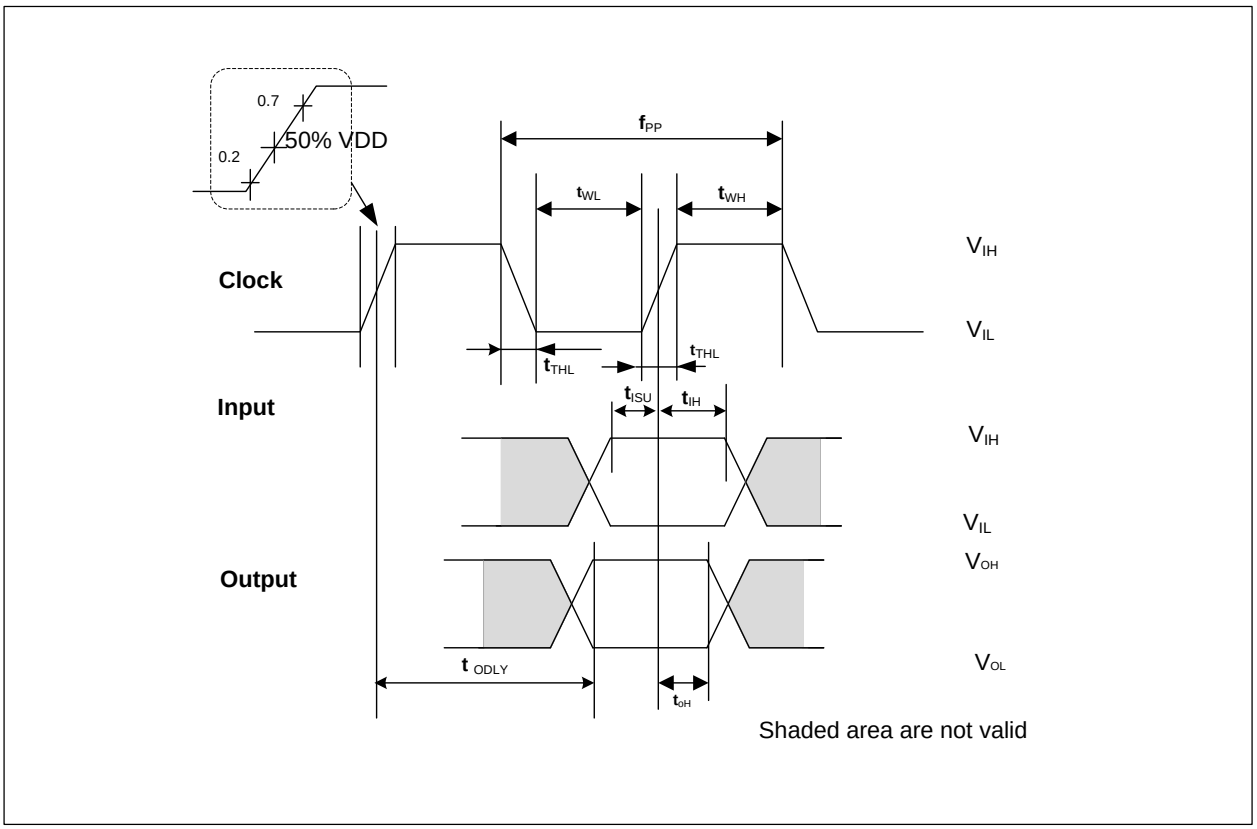


14.2. SD Card Timing Specification (High Speed Mode)

Table 15: Timing Specification (High Speed Mode)

Symbol	Item	Min	Max	Units	Notes
f_{PP}	Clock, Data Transfer Mode	0	50	MHz	C_{CARD} ≤ 10pF
f_{OD}	Clock, Identification Mode			kHz	C_{CARD} ≤ 10pF
t_{WL}	Clock Low Time	7		ns	C_{CARD} ≤ 10pF
t_{WH}	Clock High Time	7		ns	C_{CARD} ≤ 10pF
t_{TLH}	Clock Rise Time		3	ns	C_{CARD} ≤ 10pF
t_{THL}	Clock Fall Time		3	ns	C_{CARD} ≤ 10pF
t_{ISU}	CMD, DAT Input Setup Time	6		ns	C_{CARD} ≤ 10pF
T_{IH}	CMD, DAT Input Hold Time	2		ns	C_{CARD} ≤ 10pF
t_{ODLY}	CMD, DAT output delay time during Data Transfer Mode	0	14	ns	C_{CARD} ≤ 40pF
t_{ODLY}	CMD, DAT output delay time during Identification Mode	0	50	ns	C_{CARD} ≤ 40pF
t_{OH}	Output Hold Time	2		ns	C_{CARD} ≤ 40pF

Figure 9: Timing Diagram (High Speed Mode)



15. Appendix I (Standards and Specifications)

Copies of the following SD Card standards can be obtained from:

SD Card Association
2400 Camino Ramon, Suite 375
San Ramon, CA 94583 USA

Phone: (925) 275-6615
Fax: (925) 886-4870
www.sdcard.org

16. Revision History

Revision	Date	Author	Notes
1v0	March 12, 2014	NL	▪ Initial Release
1v1	December 13, 2010	NL	▪ Clarified Industrial temperature range
1v3	April 13, 2011	NL	▪ Removed preliminary from datasheet
1v5	February 22, 2012	HS	▪ Changed the part numbers based on Netlist's new part number scheme. ▪ Added Netlist's new part number decoder. ▪ Added Commercial Temp.
1v6	June 17, 2013	DP	▪ 2GB specific with sector count
1v7	March 4, 2015	BR	▪ Updated part numbers

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