NETLIST

Datasheet
Secure Digital (SD)
1GB to 256GB
NLSDabc30d-FstuAAvwxyz

1. Overview

The Netlist Secure Digital (SD) Card, Secure Digital High-Capacity (SDHC), and Secure Digital eXtended-Capacity (SDXC) card provide more removable non-volatile storage than ever before at increased transfer rates.

The Netlist SD card has been designed to meet SD Card Association version 3.0x specifications and is SD and SPI mode compatible. The on-card intelligent controller manages interface protocols, data storage and retrieval, Error Code Correction (ECC), wear leveling, power management and control, and diagnostics.

The Netlist SD card can be customized with respect to color, labeling and card identification registers (CID).

2. Features

- SD Card Association Specification V3.0 compliant
- SD & SPI mode compatibility
- Memory Capacity:
  - Up to 256GB of mass storage data
- MLC and SLC NAND flash technologies
- Non-volatile solid state storage
- 1.8V or 3.3V power supply support
- Available in the Industrial or Commercial temperature grades
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
- ECC engine
- Static wear-Leveling algorithm
- Built-in write protect switch to prevent accidental loss
- RoHS-6 compliant

3. Ordering Information

1GB to 128GB Secure Digital (SD) **Part Number:** **NLSDabc30d-FstuAAvwxyz**		
Density	**Commercial Part Number**	**Industrial Part Number**
1GB	NLSD01G30C-FMMHAAwxyz0	NLSD01G30I-FMMHAAwxyz0
2GB	NLSD02G30C-FMMHAAwxyz0	NLSD02G30I-FMMHAAwxyz0
4GB	NLSD04G30C-FMMHAAwxyz0	NLSD04G30I-FMMHAAwxyz0
8GB	NLSD08G30C-FMMHAA21110	NLSD08G30I-FMMHAA21110
16GB	NLSD16G30C-FMMHAAwxyz0	NLSD16G30I-FMMHAAwxyz0
32GB	NLSD32G30C-FMMHAAwxyz0	NLSD32G30I-FMMHAAwxyz0
64GB	NLSD64G30C-FMMHAAwxyz0	NLSD64G30I-FMMHAAwxyz0
128GB	NLSD12830C-FMMHAAwxyz0	NLSD12830I-FMMHAAwxyz0
256GB	NLSD25630C-FMMHAAwxyz0	NLSD25630I-FMMHAAwxyz0

4. SD Part Number Decoder

N	L	*a*	*b*	*c*	*d*	*e*	*f*	*g*	*h*	-	*p*	*q*	*r*	*s*	*t*	*u*	*v*	*w*	*x*	*y*	*z*
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

Position	Property	Definitions
1,2	Netlist Code	NL = Netlist
3,4	Product Type	SD = Secure Digital
5,6,7	Memory Capacity	01G = 1GB 02G = 2GB 04G = 4GB 08G = 8GB 16G = 16GB 32G = 32GB 64G = 64GB 128 = 128GB 256 = 256GB
8	Feature Set A	3 = SD3.0 when 9 = 0
9	Feature Set B	0 = SD3.0 when 8 = 3
10	Temperature Range	I = Industrial (-40°C to +85°C) C = Commercial (0°C to +70°C)
11	"-"	-
12	Flash Controller	F = SM2702
13	Flash Manufacturer	M = Micron
14	Flash Type	S = SLC M = MLC
15	Mount	H = Horizontal
16,17	OEM Code	AA = Standard Product
18	Flash Die Geometry	4 = 4x nm 3 = 3x nm 2 = 2x nm 1 = 1x nm
19	Number of CE per Flash Location	1 = 1 CE per Flash Location 2 = 2 CE per Flash Location 4 = 4 CE per Flash Location 8 = 8 CE per Flash Location
20	Number of Flash Location(s)	1 = 1 Flash Location 2 = 2 Flash Locations 4 = 4 Flash Locations 8 = 8 Flash Locations
21	Number of Die per Flash Location	1 = 1 Die per Flash Location 2 = 2 Die per Flash Location 4 = 4 Die per Flash Location 8 = 8 Die per Flash Location
22	Special Feature	0 = None (Standard Product)

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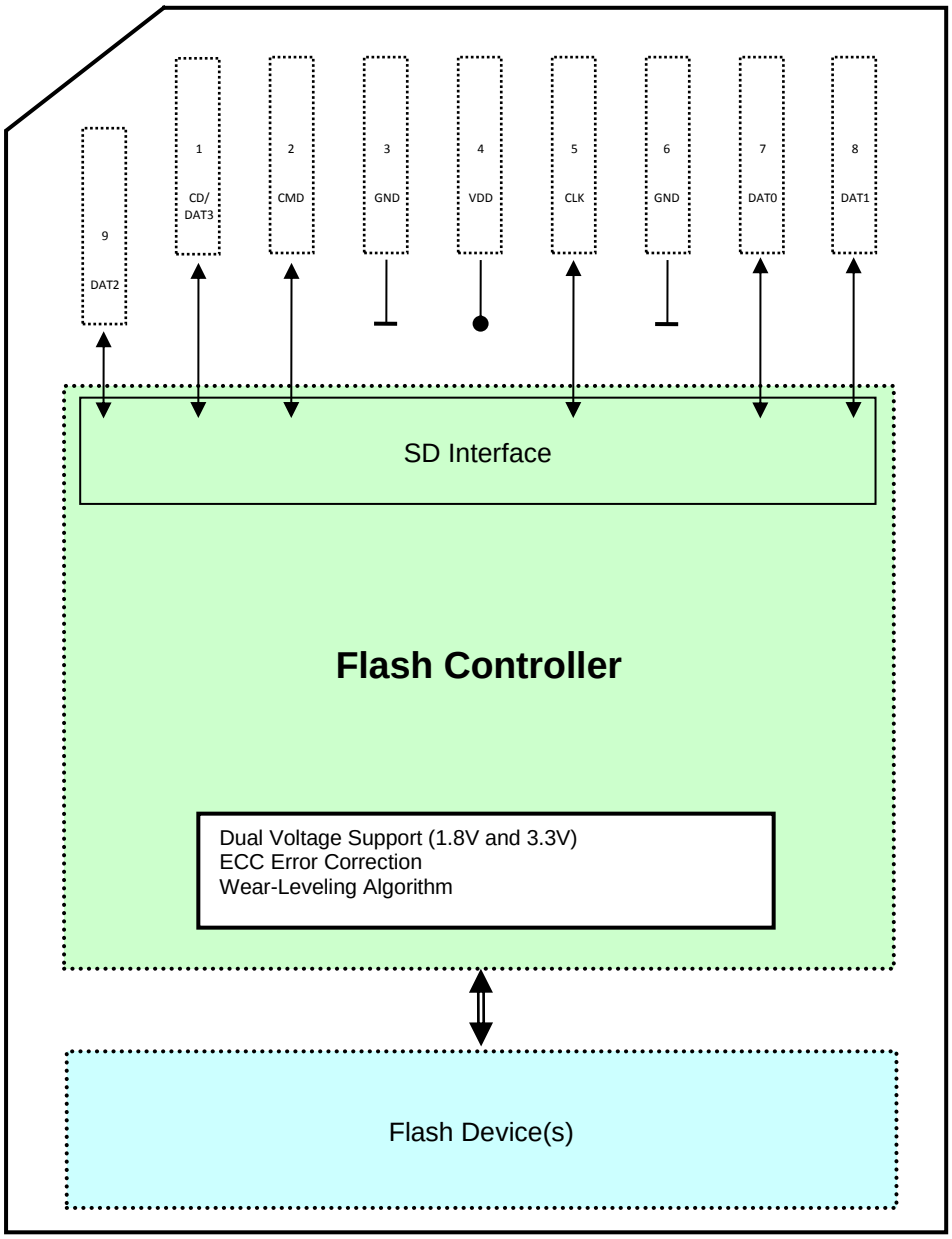
Figure 1: Netlist SD Card Configuration Functional Block Diagram



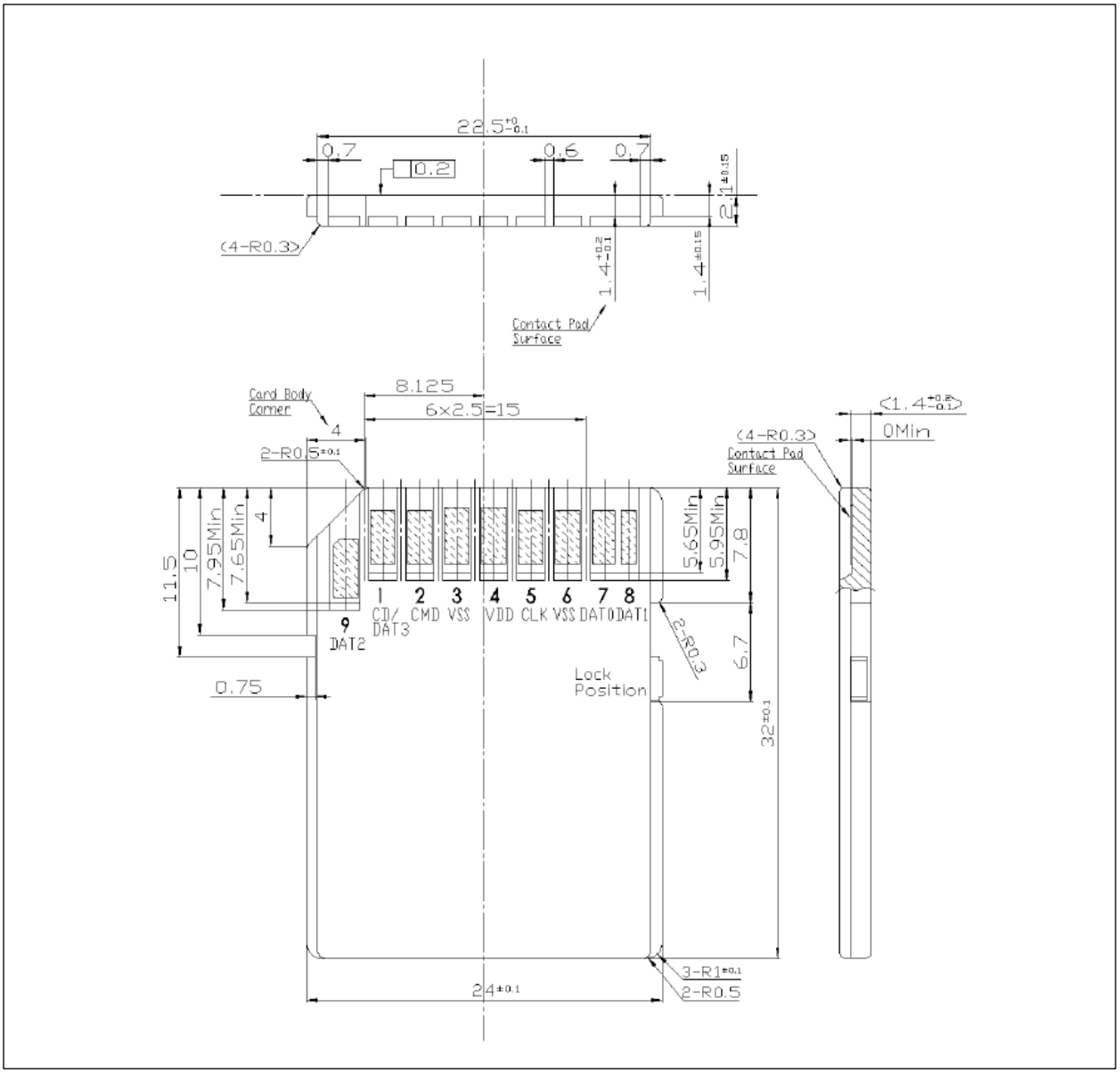
5. Physical Specifications

The host is connected to the SD Card using a standard 9-pin connector.

Table 1: Physical Specifications

Length	32.00 ± 0.10 mm (1.260”)
Width	24.0 ± 0.10 mm (0.945”)
Thickness Including Label Area	2.10 ± 0.15 mm Max (0.083”)
Color	Black
Front Label	Netlist label

Figure 2: Package Dimensions



6. Reliability and Durability

Table 2: Reliability and Durability

Temperature	Commercial Operation: 0°C to 70°C Industrial Operation : -40°C to 85°C
Vibration	15 G peak to peak maximum
Acoustic Noise	0 dB
Shock	1000 G
Humidity	95% maximum non-condensing
ESD Level	Contact Pads: Up to 4kV Coupling Plane Discharge: Up to 8 kV Air Discharge: Up to 8kV

7. Wear Leveling for Flash Memory

The Netlist SD Card makes use of advanced flash wear leveling and bad block management techniques. Wear leveling is performed with the use of reserved buffer blocks. "Wear leveled" blocks are swapped with replacement blocks that have the fewest erase cycles. Bad block management ensures that defective blocks created during device operation are mapped out and never accessed. In this manner, the life of the entire device is extended.

8. System Performance

Data transfer rates (Controller frequency @ 50 MHz)

Table 3: System Performance

CMD (Capacity)	Data-rate
Read	93 MB/s
Write	53 MB/s

9. SD Card Operation

The SD Card provides applications with a low cost mass storage device, implemented as a removable card that supports high security level for copyright protection and a compact, easy-to-implement interface.

The SD Card defines two communication protocols: SD and SPI. Applications can choose either mode of operation. Mode selection is transparent to the host as the card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. Therefore, hosts that use only one mode of communication do not have to be aware of the other.

9.1. SD MODE

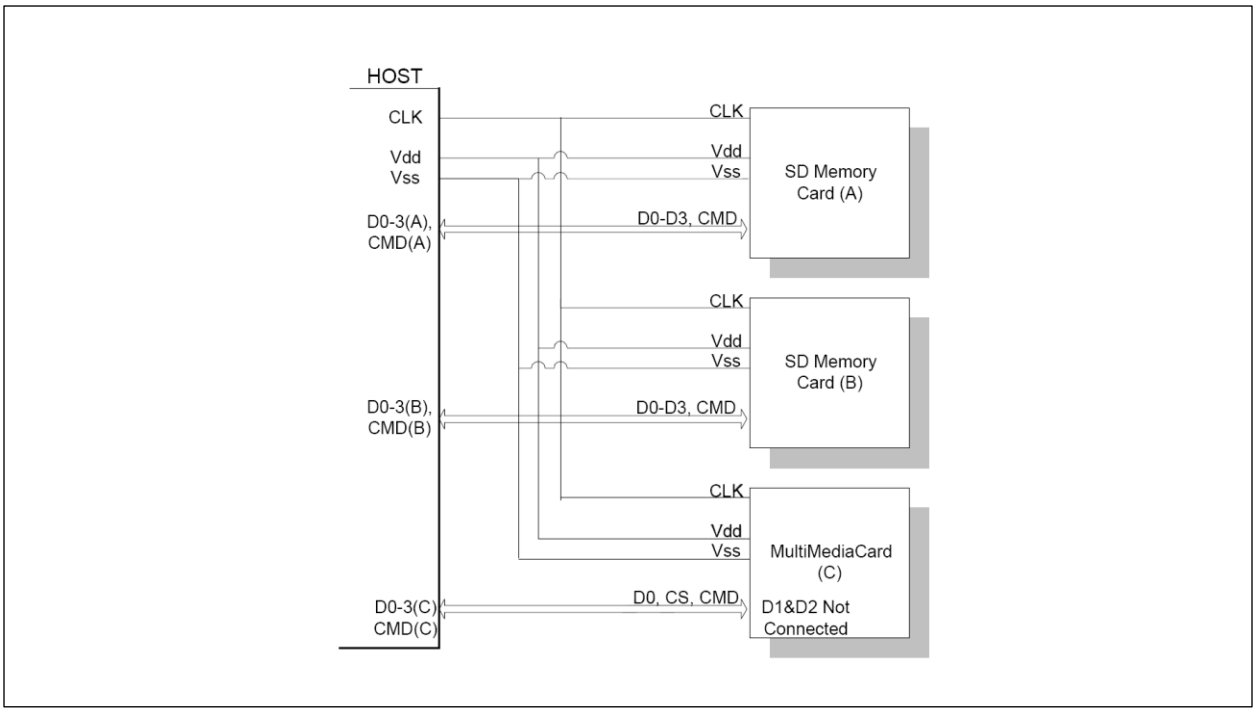
The SD Memory Card bus has a single master (host), multiple slaves (cards), synchronous star topology (see figure below). Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0 - DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.

Communication over the SD bus is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token that is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.

Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

Figure 3: SD System Bus Topology



9.2. SPI Mode

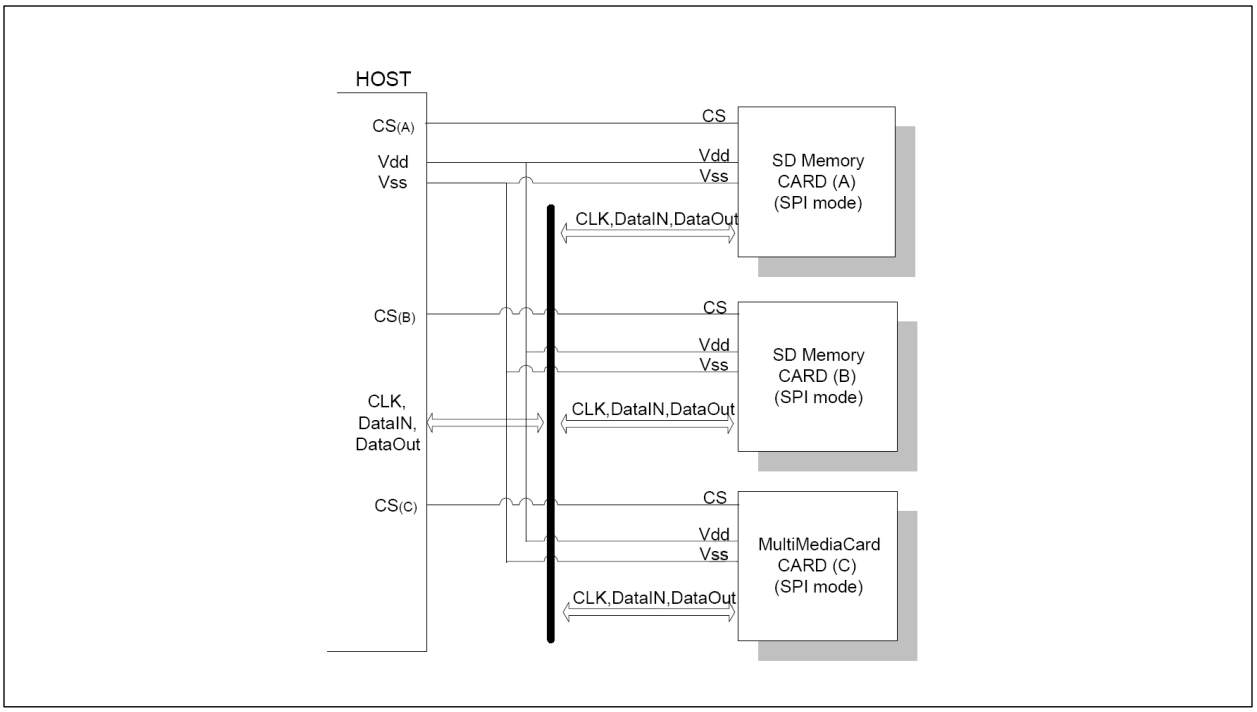
The Serial Peripheral Interface (SPI) mode is a subset of the SD Memory Card protocol, designed to communicate with a SPI channel, commonly found in microcontrollers. The interface is selected during the first reset command after power up (CMD0) and cannot be changed once the part is powered on.

The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses a subset of the SD Memory Card protocol and command set. The advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance of the SPI mode versus SD mode (e.g. Single data line and hardware CS signal per card).

While the SD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.

Similar to the SD Memory Card protocol, the SPI messages consist of command, response and data block tokens. The host starts every bus transaction by asserting the CS signal low and the selected card always responds to the command. When the card encounters a data retrieval problem in a read operation, it will respond with an error response (which replaces the expected data block). Additionally, every data block sent to the card during write operations will be responded with a data response token.

Figure 4: SPI System Bus Topology



9.3. Mode Selection

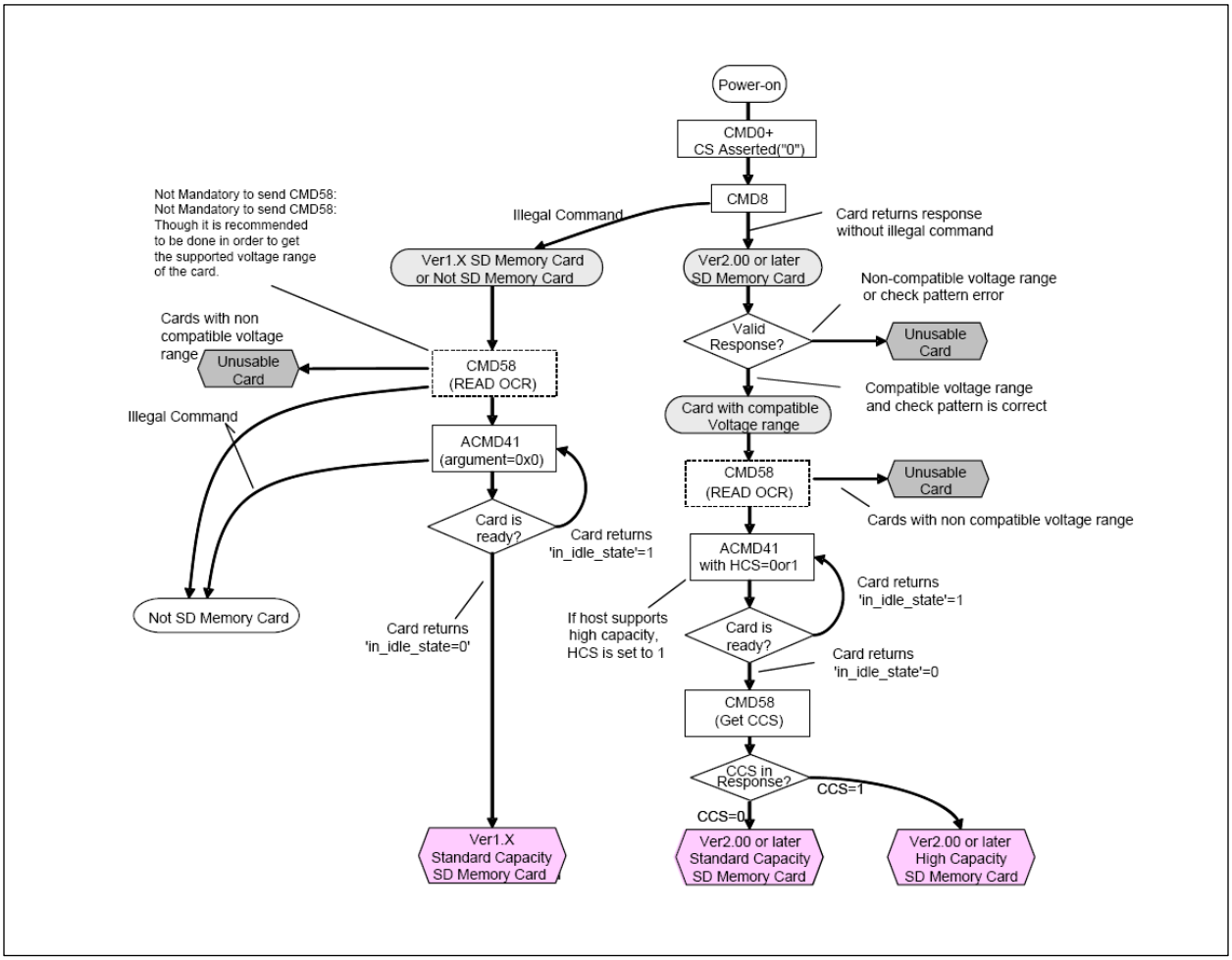
The SD Card is powered up in the SD mode. It will enter SPI mode if the CS signal is asserted (active low) during the reception of the reset command (CMD0). If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required, the card will switch to SPI and respond with the SPI mode R1 response.

The only way to return to the SD mode is by entering the power cycle. In SPI mode, the SD Card protocol state machine in SD mode is not observed. All the SD Card commands supported in SPI mode are always available. The figure below shows the initialization sequence of SPI mode.

The card checks the validity of operating condition by analyzing the argument of CMD8 and the host checks the validity by analyzing the response of CMD8. If the card indicates an illegal command, the card is legacy and does not support CMD8. If the card supports CMD8 and can operate on the supplied voltage, the response echoes back the supply voltage and the check pattern that were set in the command argument.

After initialization is completed, the host should get CCS information in the response of CMD58. CCS is valid when the card accepted CMD8 and after the completion of initialization. CCS=1 means that the card is a High Capacity SD Memory Card. CCS=0 means that the card is a Standard Capacity SD Memory Card.

Figure 5: SPI Mode Initialization State Diagram



10. SD Card Register Descriptions

Table 4: SD Card Register Descriptions

Name	Width	Description
CID	128	Card Identification Number; card individual number for identification
RCA1	16	Relative Card Address; local system address of a card, dynamically suggested by the card and approved by the host during initialization
DSR	16	Driver Stage Register; to configure the card's output drivers
CSD	128	Card Specific Data; information about the card operation conditions
SCR	64	SD Configuration Register; information about the SD Memory Card's Special Features capabilities
OCR	32	Operation Conditions Register
SSR	512	SD Status; information about the card proprietary features
CSR	32	Card Status; information about the card status

11. Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have a unique identification number.

Table 5: 11. Card Identification Register (CID)

Name	Field	Width (Bits)	Slice	Required Value
Manufacturer ID	MID	8	[127:120]	61_h
OEM/Application ID	OID	16	[119:104]	4E_h 4C_h
Product Name	PNM	40	[103:64]	
Product Revision	PRV	8	[63:56]	
Product Serial Number	PSN	32	[55:24]	
Reserved	-	4	[23:20]	
Manufacturing Date	MDT	12	[19:8]	
CRC7 Checksum	CRC	7	[7:1]	
Reserved; High(1)	-	1	[0]	

12. Operation Conditions Register (OCR)

The 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by the cards.

The 32-bit operation conditions register stores the VDD voltage profile of the card. Bit 7 of OCR is newly defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets this bit to 1.

Additionally, this register includes 2 more status information bits.

Bit 31 - Card power up status bit, this status bit is set if the card power up procedure has been finished.

Bit 30 - Card capacity status bit, this status bit is set to 1 if card is High Capacity SD Memory Card. 0 indicates that the card is Standard Capacity SD Memory Card. The Card Capacity status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify a Standard or High Capacity SD Memory Card.

The OCR register shall be implemented by the cards.

Table 6: Operation Conditions Register (OCR)

Bits	Description/Value	Notes
[31]	Card Power Up Status Bit (busy)	Valid only when the card power up status bit is set.
[30]	Card Capacity Status (CCS)	Bit is set LOW if the card has not finished the power up routine
[29:24]	Reserved	
[23:15]	2.7-2.6	
[14:8]	Reserved	
[7]	Reserved for Low Voltage Range	
[6:0]	Reserved	

The supported voltage range is coded as shown in table above. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

Table 7: SD Memory Card Pad Assignment

Pin Num	SD Card Memory Mode			SPI Mode		
	Type[1]	Signal Name	Description	Type[1]	Signal Name	Description
1	I/O; PP[2]	CD, DAT3[3]	Card Detect, Data Line[3]	Input[2]	CS#	Chip Select; Active Low
2	PP	CMD	Command	Input	DI	Data In
3	Supply	VSS1	Ground	Supply	VSS1	Ground
4	Supply	V_{DD}	Voltage Supply	Supply	V_{DD}	Voltage Supply
5	Input	CLK	Clock	Input	SCLK	Clock
6	Supply	VSS2	Ground	Supply	VSS2	Ground
7	I/O; PP	DAT0	Data Line [0]	Output; PP	DO	Data Out
8	I/O; PP	DAT1	Data Line [1]	-	-	Reserved
9	I/O; PP	DAT2	Data Line [2]	-	-	Reserved

[1] PP = I/O using push-pull drivers.

[2] At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

[3] The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.

13. Revision History

Revision	Date	Author	Notes
1v0	March 12, 2014	BR	▪ Revision notes

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