NETLIST

Datasheet
mSATA
4GB to 256GB
NLSSabcV3d-9TuHAAvwxyz

1. Overview

Netlist, a pioneer in the development of high-density memory subsystems, is proud to offer the mSATA Flash Disk Module in a JEDEC MO-300B, variation A form factor. The mSATA module follows the same form factor as the mini PCI Express module and uses the same 52 pin PCB edge style connector. The Netlist solution provides a fully compatible SATA V3.0 interface to the host system and supports serial data rates to 6.0Gbps.

Netlist's mSATA is the product of choice in applications requiring the smallest form factor with high memory density, low power, high performance, high reliability and high tolerance to shock, vibration, humidity, altitude, and temperature. Because there are no moving parts to service or maintain, the mSATA is the solution of choice for reliable alternatives to mechanical hard disk drives for high availability and mission critical applications. The on-card intelligent controller manages interface protocols, data storage and retrieval as well as Error Correcting Code (ECC), detects handling and diagnostics, power management and clock control.

Specifically designed for small form factor requirements, the Netlist mSATA is an extremely compelling solution for embedded applications such as boot loaders, virtualization systems, industrial applications, thin clients and many other applications in the enterprise environment.

The Netlist mSATA is available in capacities of 4GB to 256GB. The Netlist mSATA hosts most computing or embedded operating systems with the solid-state disk technology delivering fast boot, load, and execution of applications, with no moving parts, leading to faster system responsiveness, and durability.

Applications include virtualized boot loaders, boot and OS loaders, embedded storage, medical diagnostics, inventory management and barcode readers, and mobile industrial computer.

2. Features

- 4GB to 256GB capacity (48-bit addressing)
- SATA V3.0 compliant with NCQ support
- NCQ support for up to 32 commands
- Support for SATA 48-bit addressing mode
- SATA interface for 1.5Gbps, 3.0Gbps and 6Gbs
- Commercial or Industrial Temperature Grades
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- Available with MLC or SLC NAND Flash
- MTBF More than 2,000,000 hours
- Advanced Flash Management
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - TRIM
  - Over-Provisioning
  - Firmware Update
- Extended S.M.A.R.T. Command support
- Low Power Management
  - DEVSLP Mode
  - DIPM/HIPM Mode
- RoHS compliant
- Performance
  - Sequential Read Bandwidth: Up to 500MB/s
  - Sequential Write Bandwidth: Up to 200MB/s
- Power Consumption - 3.3V +/-0.3VDC supply
  - Read: 174 mA (typical)
  - Write: 230.6 mA (typical)
  - Idle: 53.2mA (typical)
- JEDEC MO-300B Variation A Form Factor
  - 50.80 x 29.85 mm (L x W)
- RoHS-6 compliant (Pb-free)

3. Ordering Information

4GB to 256GB mSATA Part Number: NLSSabcV3d-9TuHAAvwxyz			
Capacity	**Operating Temp Temperature**	**NAND Type**	**Part Number**
4GB	C	MLC	NLSS04GV3C-9TMHAA*xxxxx*
8GB	C	MLC	NLSS08GV3C-9TMHAA*xxxxx*
16GB	C	MLC	NLSS16GV3C-9TMHAA*xxxxx*
32GB	C	MLC	NLSS32GV3C-9TMHAA*xxxxx*
40GB	C	MLC	NLSS40GV3C-9TMHAA12421
64GB	C	MLC	NLSS64GV3C-9TMHAA*xxxxx*
128GB	C	MLC	NLSS128V3C-9TMHAA*xxxxx*
256GB	C	MLC	NLSS256V3C-9TMHAA*xxxxx*
4GB	C	SLC	NLSS04GV3C-9TSHAA*xxxxx*
8GB	C	SLC	NLSS08GV3C-9TSHAA*xxxxx*
16GB	C	SLC	NLSS16GV3C-9TSHAA21410
32GB	C	SLC	NLSS32GV3C-9TSHAA22420

4. SATA Part Number Decoder

N	L	*a*	*b*	*c*	*d*	*e*	*f*	*g*	*h*	-	*p*	*q*	*r*	*s*	*t*	*u*	*v*	*w*	*x*	*y*	*z*
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

Position	Property	Definitions	
1,2	Netlist Code	NL = Netlist	
3,4	Product Type	SS = mSATA	
5,6,7	Memory Capacity	064 = 64MB 012 = 128MB 025 = 256MB 051 = 512MB 01G = 1GB 02G = 2GB 04G = 4GB 08G = 8GB	16G = 16GB 32G = 32GB 40G = 40GB 64G = 64GB 128 = 128GB 256 = 256GB 512 = 512GB
8	Feature Set A	V = UDMA & Auto Detect	
9	Feature Set B	3 = SATA III (up to 6Gbps)	
10	Temperature Range	I = Industrial (-40°C to +85°C)	C = Commercial (0°C to +70°C)
11	"-"	-	
12	Flash Controller	9 = PS3109	
13	Flash Manufacturer	T = Toshiba	
14	Flash Type	S = SLC M = MLC	
15	Mount	H = Horizontal	
16,17	OEM Code	AA = Standard Product	
18	Flash Die Geometry	4 = 4x nm 3 = 3x nm	2 = 2x nm 1 = 1x nm
19	Number of CE per Flash Location	1 = 1 CE per Flash Location 2 = 2 CE per Flash Location	4 = 4 CE per Flash Location 8 = 8 CE per Flash Location
20	Number of Flash Location(s)	1 = 1 Flash Location 2 = 2 Flash Locations	4 = 4 Flash Locations 8 = 8 Flash Locations
21	Number of Die per Flash Location	1 = 1 Die per Flash Location 2 = 2 Die per Flash Location	4 = 4 Die per Flash Location 8 = 8 Die per Flash Location
22	Special Feature	0 = None (Standard Product) 1 = Custom Over Provisioning	

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5. mSATA Block Diagram

Figure 1: mSATA Module Block Diagram

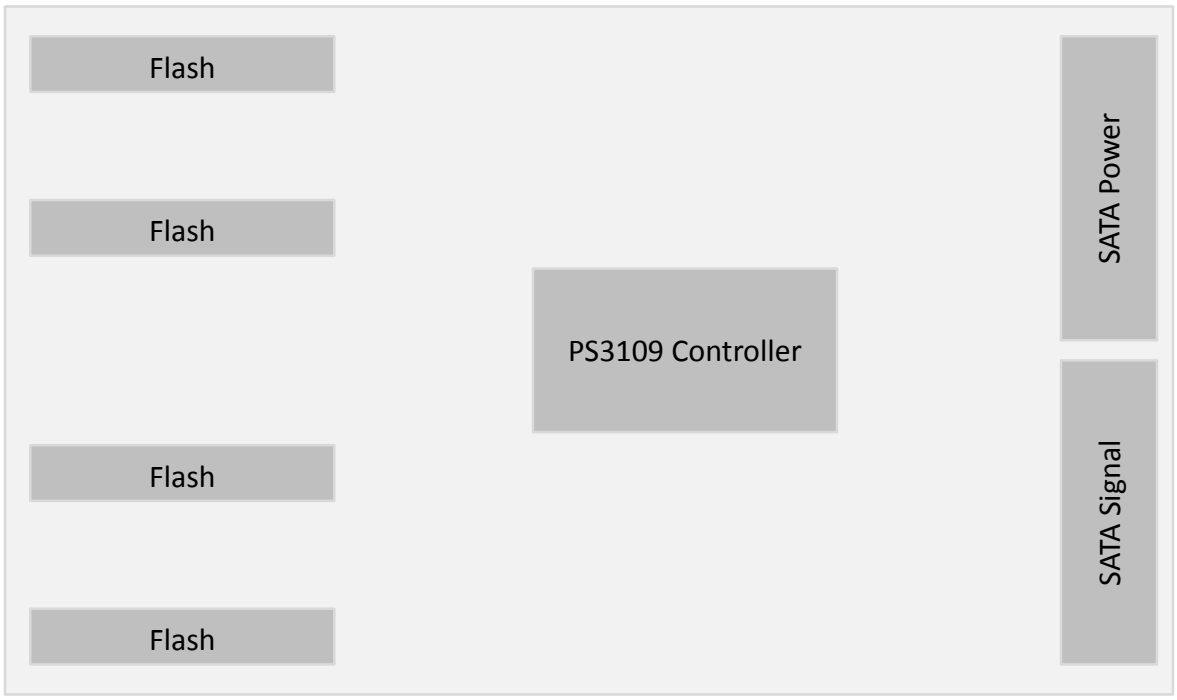
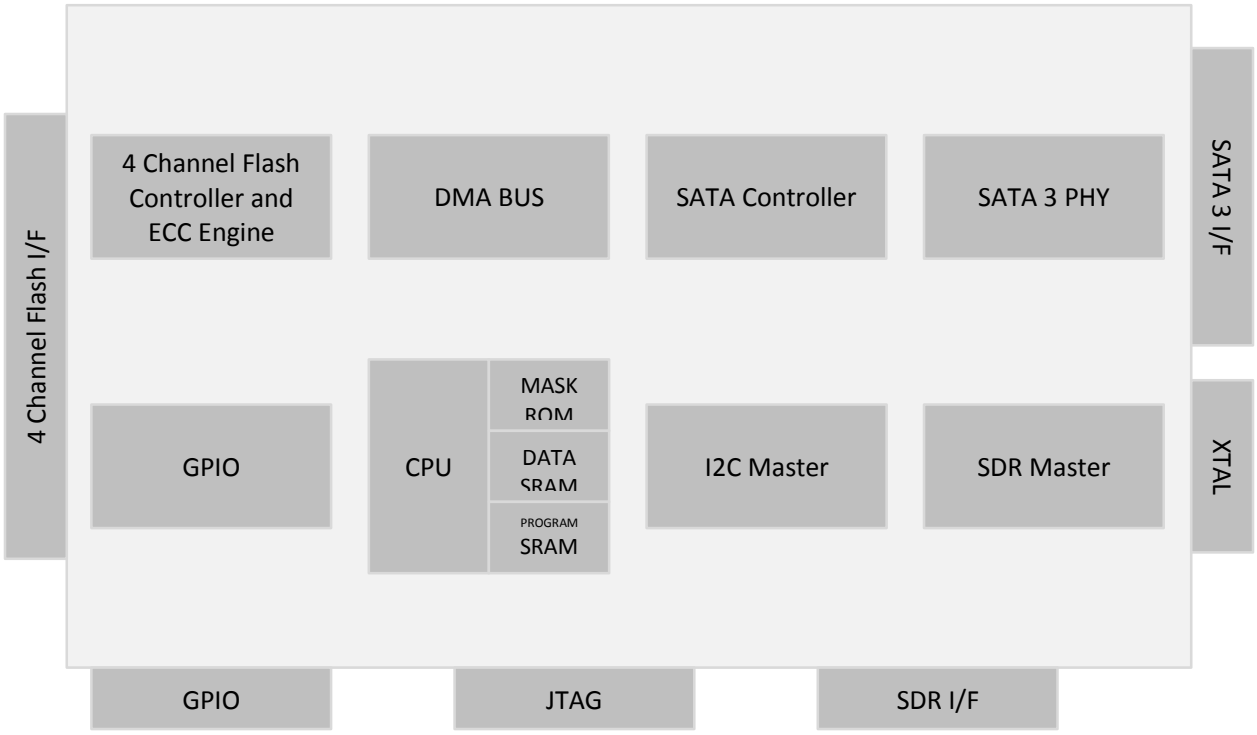


Figure 2: mSATA Controller Block Diagram



6. Physical Specifications

mSATA Flash Disk Module form-factor - JEDEC MO-300B (Variation A).

The host is connected to the mSATA module using the 52 pin mini PCIe edge type connector.

Table 1: mSATA Form-Factor

Length	50.80 ± 0.15 mm
Width	29.85 ± 0.15 mm
Thickness Including Label Area (Max)	4.85 mm

Figure 3: mSATA Outline Dimensions

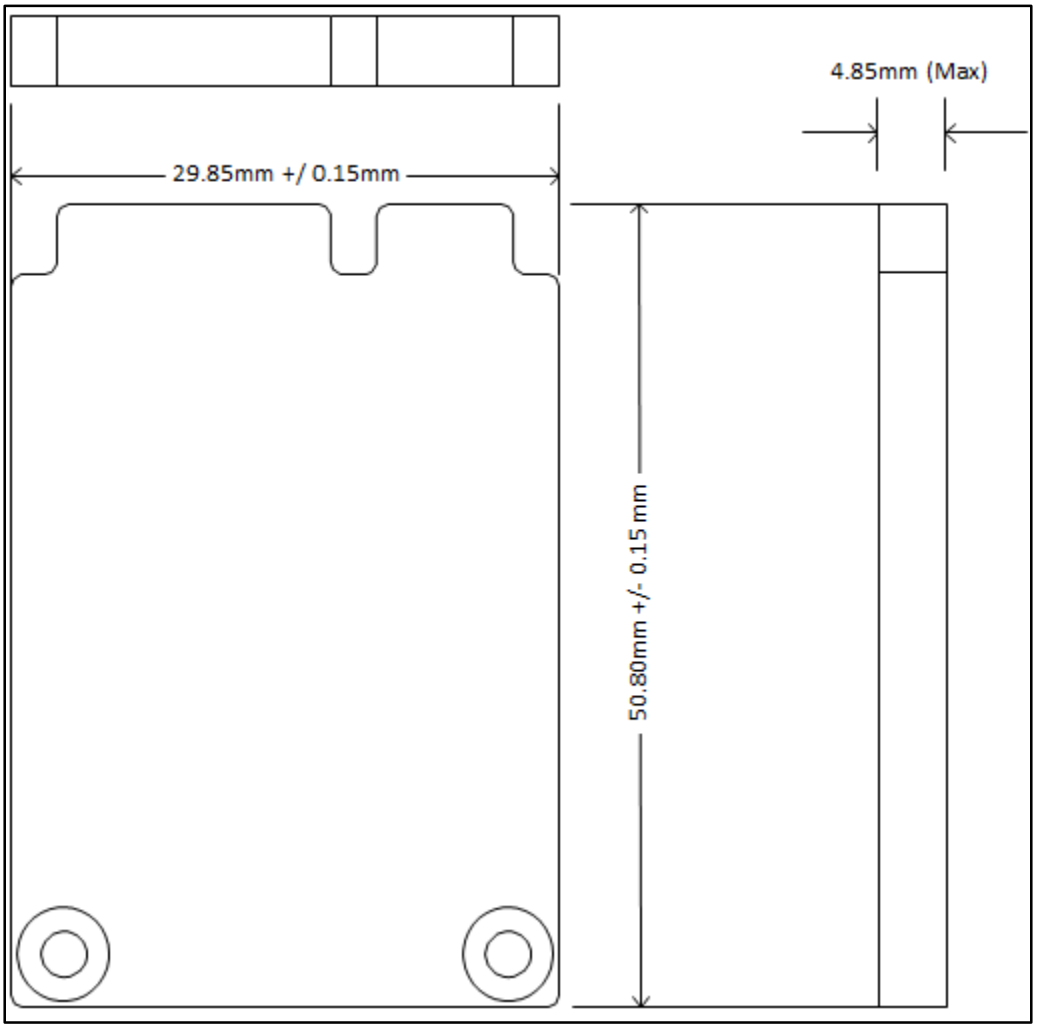


Figure 4: mSATA Physical Dimensions (1 of 2)

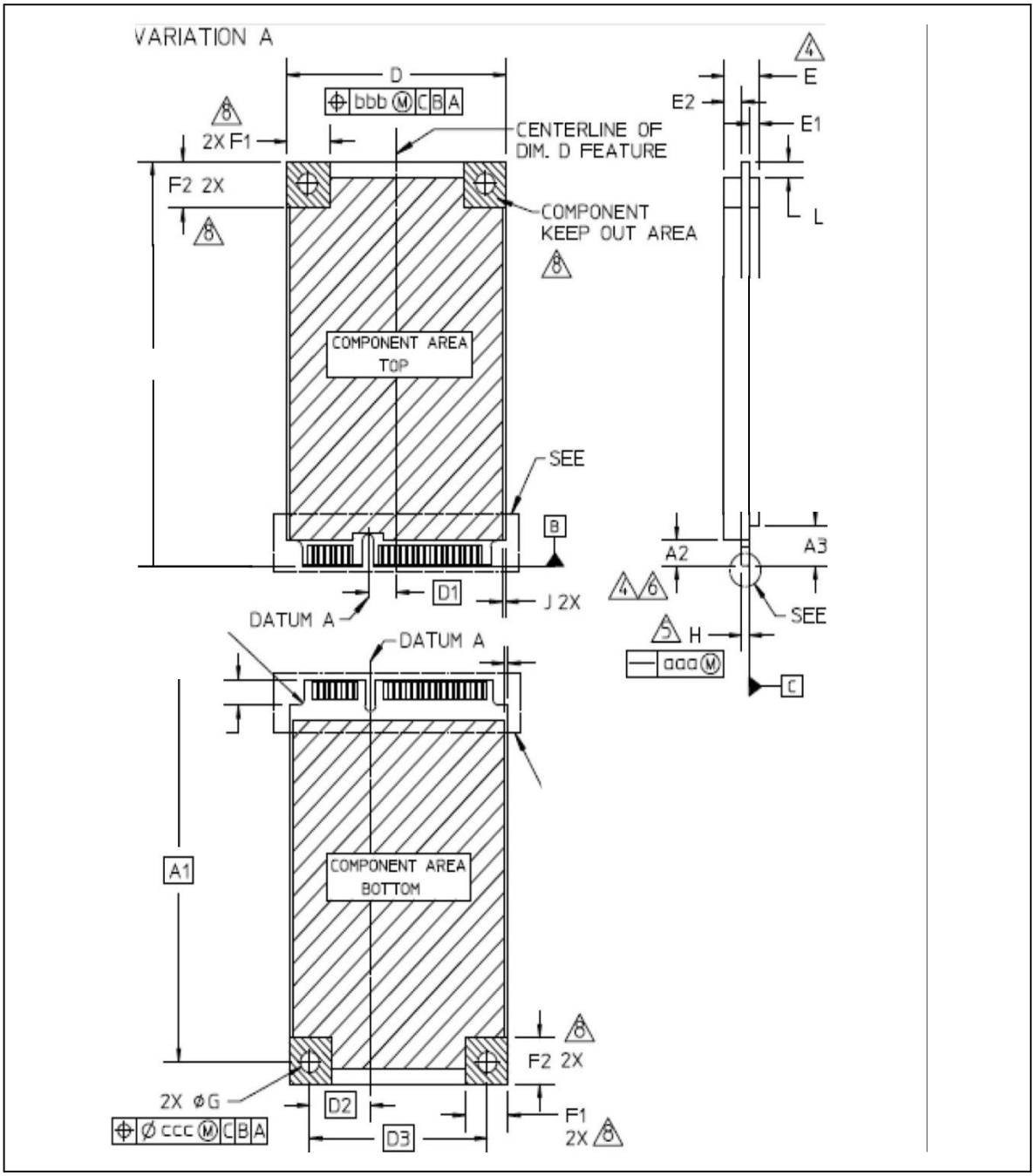


Figure 5: mSATA Physical Dimensions (2 of 2)

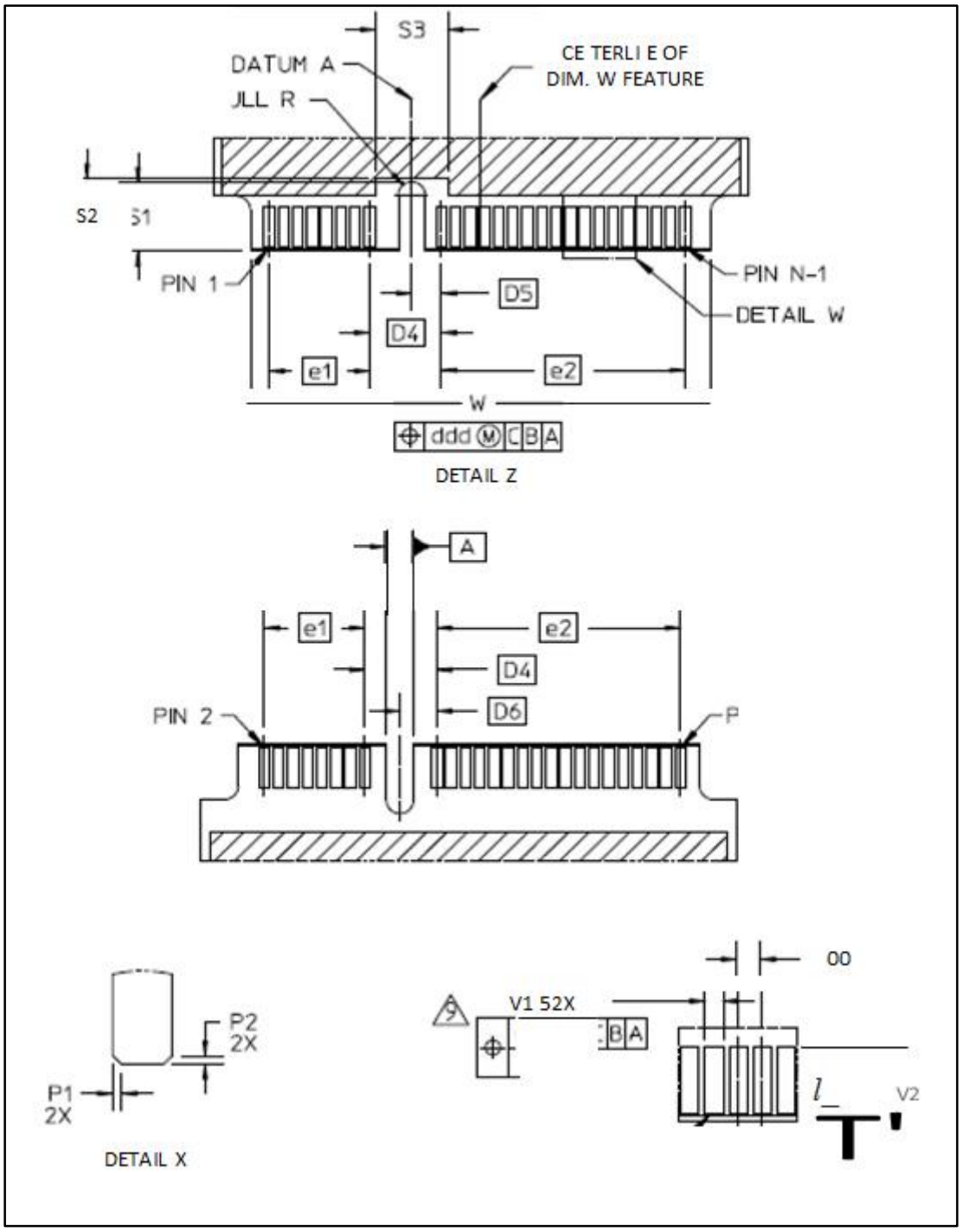


Table 2: Physical Dimensions (1 of 2)

Common Dimension Table				
Symbol	**Min**	**Nom**	**Max**	**Notes**
A2	3.20	-	-	4.6
A3	5.10	-	-	4.6
D	29.70	29.85	30	
G	2.50	2.60	2.70	
H	0.90	1.00	1.10	5
J	0.50	-	-	
K	3.20	-	-	
M	-	-	0.80	
P1	-	-	0.25	
P2	-	-	0.25	
S1	3.90	4.00	4.10	
S2	4.20	-	-	
S3	4.00	-	-	
T	1.40	1.50	1.60	
V1	0.55	0.60	0.65	
V2	2.40	2.55	2.70	
W	25.55	25.70	25.85	
Y	-	-	0.25	
N		52		
ISSUE	A			
REF	14 -131			
NOTES	1, 2, 3			

Table 3: Physical Dimensions (2 of 2)

Symbol	Value
D1	3.85
D2	8.25
D3	24.20
D4	4.00
D5	1.65
D6	2.05
e1	5.60
e2	13.60
X	0.80
ISSUE	A
REF	14-131
NOTES	1, 2, 3

Table 4: mSATA - JEDEC MO-300 Variation A

Symbol	mSATA Full Size Variation A			Notes
	Min	Nom	Max	
A	50.65	50.85	50.95	
A1	48.05 BASIC			
E	-	-	4.85	4
E1	-	-	1.35	
E2	-	-	2.40	
F	-	-	-	8
F1	5.65	5.80	5.95	8
F2	5.65	5.80	5.95	8
L	2.00	-	-	
Issue	A			
Ref	14-131			
Notes	1, 2, 3			

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

2. TOLERANCES ON ALL DIMENSIONS ±0.15 UNLESS OTHERWISE SPECIFIED.

3. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.

4. DIMENSIONS APPLICABLE WHEN COMPONENTS ARE MOUNTED ON BOTH SIDES.

5. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

6. BORDER OF COMPONENT AREA.

7. EDGE OF CONTACT PADS SHALL BE FREE OF BURRS AND EXTERNAL TIE BARS.

8. COMPONENT AND ROUTING (TOP/BOTTOM LAYER) KEEP OUT AREA FOR HOLD DOWN SOLUTIONS.

APPLICATION NOTES :

9. RECOMMENDED PLATING FOR THE CONTACT PADS ARE;
   A) PREFERABLE PLATING : ELECTROLYTIC GOLD PLATING 0.76 MICROMETERS MINIMUM OVER ELECTROLYTIC NICKEL 2.00 MICROMETERS MINIMUM.
   B) ALTERNATE PLATING : GOLD PLATING 0.05 TO 0.75 MICROMETERS OVER NICKEL 2.00 MICROMETERS MINIMUM. MUST USE AN ELECTRONIC CONTACT GRADE CORROSIVE BARRIER LUBRICANT.

7. Reliability and Durability

Table 5: mSATA Flash Disk Module Environmental Conditions

Operating Temperature	Commercial: 0°C to 70°C, or Industrial: -40°C to 85°C
Vibration	15G (80 - 2000Hz)
Humidity	8% to 95% non-condensing with T_{AMB} less than 55°C
ESD Level	Contact discharge: Up to 8 kV Air discharge: Up to 15kV
Acoustic Noise	0 dB
Shock	1,500G (0.5ms)
Typical Power Requirements	3.3V +/- 10% Idle: 53.2mA Read: 174 mA Write: 230.6 mA

7.1. Wear Leveling for Flash Memory

The Netlist mSATA module makes use of advanced flash wear leveling and bad block management techniques. Wear leveling is performed with the use of reserved buffer blocks. "Wear leveled" blocks are swapped with replacement blocks that have the fewest erase cycles. Bad block management ensures that defective blocks created during device operation are mapped out and never accessed. In this manner, the life of the entire device is extended.

8. System Performance

- Performance is obtained from CrystalDiskMark with SATA 6Gbps host.
- Samples are made of Toshiba 19nm Toggle NAND Flash.
- Performance may vary from flash configuration, SDR configuration, and platform.
- The table above is for your reference only. The criteria for MP (mass production) and for accepting goods shall be discussed based on different flash configuration.

Table 6: Module Speed

Capacity	Flash Structure	Performance				Power Consumption		
		CrystalDiskMark		ATTO		Read (mW)	Write (mW)	DEVSLP (mW)
		Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)			
4GB	4GBx1, TSOP, TSB A19nm	150	45	530	430	860	720	4.9
8GB	4GBx2, TSOP, TSB A19nm	295	85	530	430	1,155	885	4.9
16GB	8GBx2, TSOP, TSB A19nm	300	170	530	430	1,105	1,165	4.8
32GB	8GBx4, TSOP, TSB A19nm	510	180	530	430	1,535	1,315	4.9
64GB	16GBx4, TSOP, TSB A19nm	515	180	530	430	1,465	1,260	4.8
128GB	32GBx4, BGA, TSB A19nm	520	175	530	430	1,760	1,410	4.8
256GB	64GBx4, BGA, TSB A19nm	515	180	530	430	1,960	1,730	4.9
30GB	16GBx2, TSOP, Micron L85A 20nm	245	70	530	430	965	890	4.9
60GB	16GBx4, TSOP, Micron L85A 20nm	475	140	530	430	1,385	1,210	4.9
120GB	32GBx4, TSOP, Micron L85A 20nm	480	175	530	430	1,400	1,415	4.9
30GB	16GBx2, TSOP, Micron L95B 16nm	230	60	530	430	1,345	1,430	4.9
60GB	16GBx4, TSOP, Micron L95B 16nm	430	130	530	430	1,920	1,885	4.9
60GB	32GBx2, BGA, Micron L95B 16nm	500	135	530	430	1,600	1,445	4.9
120GB	32GBx4, BGA, Micron L95B 16nm	470	120	530	430	1,920	1,735	4.9
120GB	64GBx2, BGA, Micron L95B 16nm	500	125	530	430	1,640	1,480	4.9
16GB	16GBx1, TSOP, TSB 15nm	125	84	530	430	TBD	TBD	TBD
30GB	16GBx2, TSOP, TSB 15nm	245	145	530	430	TBD	TBD	TBD
60GB	16GBx4, TSOP, TSB 15nm	415	165	530	430	TBD	TBD	TBD
120GB	32GBx4, TSOP, TSB 15nm	420	175	530	430	TBD	TBD	TBD
256GB	128GBx2, BGA, TSB 15nm	430	175	530	430	TBD	TBD	TBD

9. Pin Name and Signal Description

Table 7: Pin and Signal Assigment

Pin	Signal Name	Signal Description
1	NC	No Connect
2	3.3V	3.3V Source
3	NC	No Connect
4	DGND	Digital Ground
5	NC	No Connect
6	NC	No Connect
7	NC	No Connect
8	NC	No Connect
9	DGND	Digital Ground
10	NC	No Connect
11	NC	No Connect
12	NC	No Connect
13	NC	No Connect
14	NC	No Connect
15	DGND	Digital Ground
16	NC	No Connect
17	NC	No Connect
18	DGND	Digital Ground
19	NC	No Connect
20	NC	No Connect
21	SATA GND	SATA Ground Return
22	NC	No Connect
23	TX_OUT	Host Receiver Differential Signal - Positive
24	3.3V	3.3V Source
25	TX_OUT	Host Receiver Differential Signal - Negative
26	SATA GND	SATA Ground Return
27	SATA GND	SATA Ground Return
28	NC	No Connect
29	SATA GND	SATA Ground Return
30	NC	No Connect
31	RX_IN	Host Transmitter Differential Signal - Negative
32	NC	No Connect
33	RX_IN	Host Transmitter Differential Signal - Positive
34	DGND	Digital Ground
35	SATA GND	SATA Ground Return
36	NC	No Connect
37	SATA GND	SATA Ground Return
38	NC	No Connect

Pin	Signal Name	Signal Description
39	3.3V	3.3V Source
40	DGND	Digital Ground
41	3.3V	3.3V Source
42	NC	No Connect
43	NC	No Connect
44	NC	No Connect
45	NC	No Connect
46	NC	No Connect
47	NC	No Connect
48	NC	No Connect
49	DA/DSS	Option for LED Output
50	DGND	Digital Ground
51	GND	Default Connection to Ground
52	3.3V	3.3V Source

10. DC Characteristics

Following Tables define the D.C. Characteristics for the Module using the conditions listed below.

Vcc = 3.3V ± 5%

Table 8: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Voltage	V_{CC}	-0.3V min. to 3.6V max.
Voltage on any pin except V_{CC} with respect to GND.	V	-0.5V min. to V_{CC} + 0.5V max.
Storage Temperature	T_{ST}	-50°C to +125°C

Table 9: Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Input Voltage	V_{CC}	3.0	3.3	3.6	V
Commercial Temperature	T_{AMB_C}	0°		70°	C
Industrial Temperature[1]	T_{AMB_I}	-40°		+85°	C

Table 10: Input Leakage Current

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Input Leakage Current	I_L	$V_{IH} = V_{CC}$ V_{IL} = GND	-1		1	µA

Table 11: Logic Level Output Drive Characteristics

Parameter	Symbol	MIN	TYP	MAX	Units
Logic High Output Voltage	V_{OH}	V_{CC} - 0.3V		V_{CC}	V
Logic Low Output Voltage	V_{OL}	0		0.4V	V
Logic High Input Voltage	V_{IH}	V_{CC} x 0.8V		V_{CC}	V
Logic Low Input Voltage	V_{IL}	0		V_{CC} x 0.2V	V
Tri-State Leakage Current	I_{L_HIZ}	-10	+/- 1	10	µA

[1] Contact the factory for Industrial Temperature grade module lead times and availability.

11. ATA Command Set

This section defines the software requirements and commands the host sends to the mSATA module. Commands are issued by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 17: ATA Command Set) of command acceptance, all dependent on the host not issuing commands unless the mSATA is not busy (BSY=0).

All commands listed in this specification shall be implemented. Commands can be implemented as "no operation" to meet this requirement. The Security Mode feature set (command codes F1, F2, F3, F4, F5, and F6) should not be implemented unless the device is intended to be used in an embedded, non-removable application. The Security Mode feature set was not designed for removable devices and certain problems may be encountered when using these commands in a removable application. This specification introduces some new commands and features.

Upon receipt of a Class 1 command, the mSATA sets BSY within 400 ns.

Upon receipt of a Class 2 command, the mSATA sets BSY within 400 ns, sets up the sector buffer for a write operation, sets DRQ within 700 ns, and clears BSY within 400 ns of setting DRQ.

Upon receipt of a Class 3 command, the mSATA sets BSY within 400 ns, sets up the sector buffer for a write operation, sets DRQ within 20 ms (assuming no re-assignments), and clears BSY within 400 ns of setting DRQ.

Table 12: Command Set

No.	Command Set	OP Code (hex)	No.	Command Set	OP Code (hex)
1	Check Power Mode	E5	30	Security Disable Password	F6
2	Data Set Management	06	31	Security Erase Prepare	F3
3	DCO	B1	32	Security Erase Unit	F4
4	Download Microcode PIO	92	33	Security Freeze Lock	F5
5	Download Microcode DMA	93	34	Security Set Password	F1
6	Execute Drive Diagnostics	90	35	Security Unlock	F2
7	Flush Cache	E7	36	Seek	70
8	Flush Cache Ext	EA	37	Set Features	EF
9	Identify Device	EC	38	Set Max Address	F9
10	Idle	E3	39	Set Max Address Ext	37
11	Idle Immediate	E1	40	Set Multiple Mode	C6
12	Initialize Drive Parameters	91	41	Sleep	E6
13	Read Buffer	E4	42	SMART	B0
14	Read DMA (without Retry)	C9	43	Standby	E2
15	Read DMA (with Retry)	C8	44	Standby Immediate	E0
16	Read DMA Ext	25	45	Write Buffer	E8
17	Read FPDMA Queued	60	46	Write DMA (without Retry)	CB
18	Read Log Ext	2F	47	Write DMA (with Retry)	CA
19	Read Multiple	C4	48	Write DMA Ext	35
20	Read Multiple Ext	29	49	Write DMA FUA Ext	3D
21	Read Native Max Address	F8	50	Write FDMA Queued	61
22	Read Native Max Ext	27	51	Write Log Ext	3F

No.	Command Set	OP Code (hex)	No.	Command Set	OP Code (hex)
23	Read Sectors (without Retry)	21	52	Write Multiple	C5
24	Read Sectors (with Retry)	20	53	Write Multiple Ext	39
25	Read Sectors Ext	24	54	Write Multiple FUA Ext	CE
26	Read Verify Ext	42	55	Write Sectors (without Retry)	31
27	Read Verify Sectors (without Retry)	41	56	Write Sectors (with Retry)	30
28	Read Verify Sectors (with Retry)	40	57	Write Sectors Ext	34
29	Recalibrate	10	58	Write Uncorrectable	45

Table 13: Identity Drive Information

Word Address	F: Fixed V: Variable X: Both	Default Value (hex)	Data Field Type Information
0	F	045A	General configuration - bit significant information
1	X	3FFF	Obsolete - Number of Logical Cylinders (16,383)
2	V	0000	Specific Configuration
3	X	0010	Obsolete - Number of Logical Heads (16)
4	X	7E00	Retired
5	X	0200	Retired
6	X	003F	Obsolete - Number of Logical Sectors per Track (63)
7 - 8	V	0	Reserved for Assignment by the Compact Flash Association
9	X	0000	Retired
10 - 19	F	xxxx	Serial Number in ASCII (20 Characters)
20	X	0000	Retired
21	X	0000	Retired
22	X	0000	Obsolete
23 - 26	F	xxxx	Firmware revision in ASCII (8 Characters)
27 - 46	F	xxxx	Model Number in ASCII
47	F	8001	7:0 - Maximum number of sectors transferred per interrupt on MULTIPLE commands
48	F	0000	Reserved
49	F	0F00	Capabilities
50	F	4000	Capabilities
51	X	0200	Obsolete
52	X	0000	Obsolete
53	F	0007	Words 88 and 70:64 are valid
54	X	3FFF	Obsolete - Number of Logical Cylinders (16383)
55	X	0010	Obsolete - Number of Logical Heads (16)

Word Address	F: Fixed V: Variable X: Both	Default Value (hex)	Data Field Type Information
56	X	003F	Obsolete - Number of Logical Sectors per Track (63)
57	X	FC10	Obsolete
58	X	00FB	Obsolete
59	F	0100	Number of Sectors Transferred per Interrupt on MULTIPLE Commands
60 - 61	F	037DFF40 (32GB)	Total Number of User Addressable Sectors
60 - 61	F	xxxxxxxx (64GB)	Total Number of User Addressable Sectors
62	X	0	Obsolete
63	F	0007	Multi-word DMA modes Supported / Selected
64	F	0003	Advance Transfer Modes Supported
65	F	0078	Minimum Multi-word DMA transer cycle time per word
66	F	0078	Manufacturer's recommended Multi-word DMA transfer cycle time
67	F	0078	Minimum PIO transfer cycle time without flow control
68	F	0078	Minimum PIO transfer cycle time with IORDY flow control
69	F	0000	Reserved
70	F	0000	Reserved
71	F	0	Reserved for the IDENTIFY PACKET DEVICE Command
72	F	0	Reserved for the IDENTIFY PACKET DEVICE Command
73	F	0	Reserved for the IDENTIFY PACKET DEVICE Command
74	F	0	Reserved for the IDENTIFY PACKET DEVICE Command
75	F	0	Queue Depth
76	F	0002	SATA Capabilities
77	F	0	Reserved - future Serial ATA Definition
78	F	0000	Serial ATA Features Supported
79	V	0000	Serial ATA Features Enabled
80	F	00F8	Major Version Number
81	F	0021	Minor Version Number
82	F	7429	Command Set Supported
83	F	7008	Command Set Supported
84	F	4000	Command Set / Feature Supported Extension
85	V	7028	Command Set / Feature Enabled
86	V	3000	Command Set / Feature Enabled
87	V	4000	Command Set / Feature Default
88	V	007F	Ultra DMA Modes
89	F	0000	Time Required for Security Unit Erase Completion
90	F	0000	Time Required for Enhanced Security Erase Completion
91	V	0	Current Advanced Power Management Value

Word Address	F: Fixed V: Variable X: Both	Default Value (hex)	Data Field Type Information
92	V	0000	Master Password Revision Code
93	F	0	Hardware Reset Result. The contents of bits (12:0) of this word shall change only during the execution of a hardware Reset.
94	V	0	Vendor's Recommended and Actual Acoustic Management Value
95	F	0	Stream Minimum Request Size
96	V	0	Streaming Transfer Time - DMA
97	V	0	Streaming Access Latency - DMA and PIO
98	F	0	Streaming Performance Granularity
99	F	0	Streaming Performance Granularity
100 - 103	V	xxxxxxxx - 32GB xxxxxxxx - 64GB xxxxxxxx - 128GB	Maximum User LBA for 48-bit Address Feature Set
104	V	0	Streaming Transfer Time – PIO
105	F	0	Reserved
106	F	0	Physical Sector Size / Logical Sector Size
107	F	0	Interseek Delay for ISO-7779 Acoustic Testing (in microseconds)
108 - 111	F	0	Unique ID
112 - 115	F	0	Reserved
116	V	0	Reserved
117 - 118	F	0	Words per Logical Sector
119	F	0	Supported Settings
120	F	0	Command Set / Feature Enabled/Supported
121 - 126	F	0	Reserved
127	F	0	Removable Media Status Notification Feature Set Support
128	V	0	Security Status
129 - 159	X	0	Vendor Specific
160	F	0	Compact Flash Association (CFA) Power Mode 1
161 - 175	X	0	Reserved for Assignment by the CFA
176 - 205	V	0	Current Media Serial Number
206 - 216	F	0	Reserved
217	F	0	Non-rotating Media Device
218 - 221	F	0	Reserved
222	F	0	Reserved
223 - 233	F	0	Reserved
234		0	Reserved
235		0	Reserved
236 - 254	F	0	Reserved
255	X	Varies	Integrity Word (Checksum and Signature)

12. Low Power Management

12.1. DEVSLP Mode (Optional)

With the increasing need of aggressive power/battery life, SATA interfaces include a new feature, Device Sleep (DEVSLP) mode, which helps further reduce the power consumption of the device. DEVSLP enables the device to completely power down the device PHY and other sub-systems, making the device reach a new level of lower power operation. The DEVSLP does not specify the exact power level a device can achieve in the DEVSLP mode, but the power usage can be dropped down to 5mW or less.

12.2. DIPM / HIPM Mode

SATA interfaces contain two low power management states for power saving: Partial and Slumber modes. For Partial mode, the device has to resume to full operation within 10 microseconds, whereas the device will spend 10 milliseconds to become fully operational in the Slumber mode. SATA interfaces allow low power modes to be initiated by Host (HIPM, Host Initiated Power Management) or Device (DIPM, Device Initiated Power Management). As for HIPM, Partial or Slumber mode can be invoked directly by the software. For DIPM, the device will send requests to enter Partial or Slumber mode.

13. Power Loss Protection: Flushing Mechanism

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, the controller applies the GuaranteedFlush technology, which requests the controller to transfer data to the cache. For this device, SDR performs as a cache, and its sizes include 8MB or 32MB. Only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

Additionally, it is critical for a controller to shorten the time the in-flight data stays in the cache. Thus, Netlist applies an algorithm to reduce the amount of data that resides in the cache to provide better performance. This SmartCacheFlush technology allows incoming data to only have a “pit stop” in the cache and then move to the NAND flash at once. If the flash is jammed due to particular file sizes (such as random 4KB data), the cache will be treated as an “organizer”, consolidating incoming data into groups before written into the flash to improve write amplification.

With the Flush Mechanism, Netlist’s device provide the reliability required by consumer, industrial, and enterprise-level applications.

14. Advanced Device Security Features

14.1. Secure Erase

Secure Erase is a standard ATA command and will write all “0xFF” to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will erase its storage blocks and return to its factory default settings.

14.2. Write Protect

When a SSD contains too many bad blocks and data are continuously written in, then the SSD might not be usable anymore. Thus, Write Protect is a mechanism to prevent data from being written in and protect the accuracy of data that are already stored in the SSD.

15. SMART Command Set Description

Communication to or from the device through Data Register and 7 Command Block Registers(28bit Command Format) includes: Feature Register, Error Register, Sector Count Register, Sector Number Register, Cylinder Low Register, Cylinder High Register, Drive Head Register, Status Register, Command Register.

Direction: Input = from Host to Device; Output = from Device to Host

Table 14: SMART Command Block Register Addressing

Offset Address	Read	Write	Value Type
0x00	Data	Data	WORD
0x01	Error	Feature	BYTE
0x02	Sector Count	Sector Count	BYTE
0x03	Sector Number - (LBA low current)	Sector Number - (LBA low current)	BYTE
0x04	Cylinder Low - (LBA mid current)	Cylinder Low - (LBA mid current)	BYTE
0x05	Cylinder High - (LBA high current)	Cylinder High - (LBA high current)	BYTE
0x06	Drive Head	Drive Head	BYTE
x007	Status	Command	BYTE

Table 15: SMART READ Attribute Register Addressing

ID	Vendor Command	Feature	Sector Count	Sector Number	Cylinder Low	Cylinder High	Drive Head	Command
0	SMART READ Attribute	0xD0	0x01	XX	0x4F	0xC2	0xA0	0xB0
1	SMART READ Attribute Thresholds	0xD1	0x01	XX	0x4F	0xC2	0xA0	0xB0
2	SMART ENABLE Attributes AUTOSAVE	0xD2	0xF1	XX	0x4F	0xC2	0xA0	0xB0
3	SMART DISABLE Attribute AUTOSAVE	0xD2	0x00	XX	0x4F	0xC2	0xA0	0xB0
5	SMART ENABLE Operations	0xD8	XX	XX	0x4F	0xC2	0xA0	0xB0
6	SMART DISABLE Operations	0xD9	XX	XX	0x4F	0xC2	0xA0	0xB0
7	SMART Return Status	0xDA	XX	XX	0x4F	0xC2	0xA0	0xB0

15.1. SMART Read Attribute - PIO Data

This command will return 1 sector of SMART Read Attribute information. PIO Data Protocol

Table 16: Read Attribute - Normal Output

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	XX							
Cylinder High - (LBA high current)	XX							
Drive Head	XX							
Status	0x50							

Table 17: Read Attribute - Input

Register	7	6	5	4	3	2	1	0
Feature	0xD0							
Sector Count	0x01							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	0x4F							
Cylinder High - (LBA high current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

Table 18: Attribute Description

Standard	ID (Hex)	ID (Dec)	Unit	Description
Standard	01	1	count	Number of accumulation of uncorrectable error (ECC error)
Standard	09	9	hour	Power-on hours count
Standard	0C	12	count	Power on/off cycles count
Standard	A8	168	count	SATA PHY error count
Standard	AA	170	count	Early bad block #
Standard	B0	176	count	Later bad block #
Standard	AD	173	count	Max. erase count
Standard	AD	173	count	Average erase count
Standard	C0	192	count	Number of unexpected power loss count
Standard	DA	218	count	Number of accumulation CRC error
Additional	E7	231	%	SSD life left
Additional	E9	233	MB	Lifetime Writes to Flash
Additional	F1	241	MB	Lifetime Writes from Host

Table 19: SMART Attribute Actual Data Format (all values in hex)

0	1	2	3	4	5	6	7	8	9	10	Threshold
ID	Flag	Flag	Value	Worst	DATA						
01	0A	00	Read Error Rate (1~100)	Read Error Rate (1~100)	Number of ECC Error				0	0	00
09	12	00	64	64	Power-on Hours Count				0	0	00
0C	12	00	64	64	Power On/Off Cycles Count				0	0	00
A8	12	00	64	64	SATA PHY Error Count				0	0	00
AA	13	00	64	64	Max Early Bad Block Count				0	0	00
AD	00	00	64	64	Average Erase Count		Max Erase Count		0	0	00
C0	12	00	64	64	Unexpected Power Loss Count				0	0	00
C4	00	00	64	64	Total Later Bad				0	0	00
DA	0b	00	64	64	CRC Error Count				0	0	00
E7	13	00	64	64	SSD Life Left	0	0	0	0	0	00
E9	13	00	64	64	NAND Writes (MB)						00
F1	12	00	64	64	Host Write MB						00

15.2. SMART Read Attribute - Thresholds

This command will return 1 sector of SMART Thresholds Attribute information. PIO Data Protocol

Table 20: Thresholds Attribute – Input

Register	7	6	5	4	3	2	1	0
Feature	0xD1							
Sector Count	0x01							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	0x4F							
Cylinder High - (LBA high current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

Table 21: Thresholds Attribute – Normal INPUT

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	XX							
Cylinder High - (LBA high current)	XX							
Drive Head	XX							
Status	0x50							

15.3. SMART Enable Attribute - Auto Save

This command will Enable the optional attribute, Auto Save, feature of the device. Non-PIO Data protocol

Table 22: Enable Auto Save Attribute - Input

Register	7	6	5	4	3	2	1	0
Feature	0xD2							
Sector Count	0xF1							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	0x4F							
Cylinder High - (LBA high current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

Table 23: Enable Auto Save Attribute - Normal Output

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	XX							
Cylinder High - (LBA high current)	XX							
Drive Head	XX							
Status	0x50							

15.4. SMART Disable Attribute - Auto Save

This command will Disable the optional attribute, Auto Save, feature of the device. Non-PIO Data protocol.

Table 24: Disable Auto Save Attribute - Input

Register	7	6	5	4	3	2	1	0
Feature	0xD2							
Sector Count	0x00							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	0x4F							
Cylinder High - (LBA high current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

Table 25: Disable Auto Save Attribute - Normal Output

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	XX							
Cylinder High - (LBA high current)	XX							
Drive Head	XX							
Status	0x50							

15.5. SMART ENABLE Operations

This command will enable access to all SMART capabilities within the device. Non-PIO data protocol.

Table 26: ENABLE SMART Access – Input

Register	7	6	5	4	3	2	1	0
Feature	0xD8							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	0x4F							
Cylinder High - (LBA high current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

Table 27: ENABLE SMART Access - Normal Output

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	XX							
Cylinder High - (LBA high current)	XX							
Drive Head	XX							
Status	0x50							

15.6. SMART DISABLE Operations

This command will disable access to all SMART capabilities within the device, including any and all timer and event count functions exclusively related to this feature. Non-PIO data protocol.

Table 28: DISABLE SMART Access – Input

Register	7	6	5	4	3	2	1	0
Feature	0xD9							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	0x4F							
Cylinder High - (LBA high current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

Table 29: DISABLE SMART Access - Normal Output

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	XX							
Cylinder High - (LBA high current)	XX							
Drive Head	XX							
Status	0x50							

15.7. SMART Return Status

This command will return the reliability status of the device to the Host. Non-PIO data protocol. Status Return:

If Current Reserved Block > 3; Return 0x4F, 0xC2

If Current Reserved Block <= 3; Return 0xF4, 0x2C (Exceeded threshold detection condition)

Table 30: Return Status – Input

Register	7	6	5	4	3	2	1	0
Feature	0xDA							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	0x4F							
Cylinder High - (LBA high current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

Table 31: Return Status - Normal Output

Register	7	6	5	4	3	2	1	0
Error	XX							
Sector Count	XX							
Sector Number - (LBA low current)	XX							
Cylinder Low - (LBA mid current)	XX							
Cylinder High - (LBA high current)	XX							
Drive Head	XX							
Status	0x50							

16. Revision History

Revision	Date	Author	Notes
0v97	06/10/2011	TK	Initial draft release.
0v98	07/25/2011	HS	Changed the module thickness from 4.0 mm to 4.85 mm according to JEDEC MO-300B specification.
1v0	08/05/2011	HS	Tables were reformatted, PDS was changed to DS.
1v1	02/17/2011	HS	Part numbers were updated to new Netlist part numbering schema. The vibration test requirement was changed from 20G to 15G.
1v2	12/18/2013	SS	Updated SATA controller and associated specifications.
1v3	03/10/2014	BR	Updated Part Numbers.
1v4	04/11/2014	BR	Updated Part Numbers. Updated Block Diagram.
1v5	06/10/2014	BR	Updated part number table and ordering information.
1v6	10/20/2014	BR	Updated Ordering Information.
1v7	10/23/2014	BR	Updated Table 18: Attribute Description and Table 19: SMART Attribute Actual Data Format (all values in hex).
1v8	10/27/2014	BR	Updated Table 18: Attribute Description.
1v9	03/19/2015	BR	Updated Features
2v0	04/14/2015	BR	Updated Ordering Information
2v1	04/17/2015	BR	Added Low Power Management, Power Loss Protection: Flushing Mechanism, and Advanced Device Security Features
2v2	05/13/2015	BR	Updated System Performance

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