

Product Specification

NHD-2.7-12864WDY3M-CTP

Graphic OLED Display Module

NHD-	Newhaven Display
2.7-	2.7" Diagonal Size
12864-	128 x 64 Pixel Resolution
WD-	Model
Y-	Emitting Color: Yellow
3-	+3.3V Power Supply
M-	Molex (52271-2079) Connector Interface
CTP-	Capacitive Touch Panel

Table of Contents

Document Revision History.....	2
Mechanical Drawing	3
Pin Description	4
Interface Selection.....	5
On-Board Jumper Options	6
Electrical Characteristics	7
Optical Characteristics	8
Driver/Controller Information	8
Table of Commands.....	9
Capacitive Touch Panel Registers	12
MPU Interface	15
Timing Characteristics – Capacitive Touch Panel.....	19
Recommended Initialization	22
Example Software Routines	23
Quality Information.....	24

Additional Resources

- **Support Forum:** <https://support.newhavendisplay.com/hc/en-us/community/topics>
- **GitHub:** <https://github.com/newhavendisplay>
- **Example Code:** <https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/>
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** <https://www.newhavendisplay.com/specs/precautions.pdf>
- **Warranty / Terms & Conditions:** <https://www.newhavendisplay.com/terms.html>



Document Revision History

Revision	Date	Description	Changed By
-	07/13/2023	Initial Release	KL

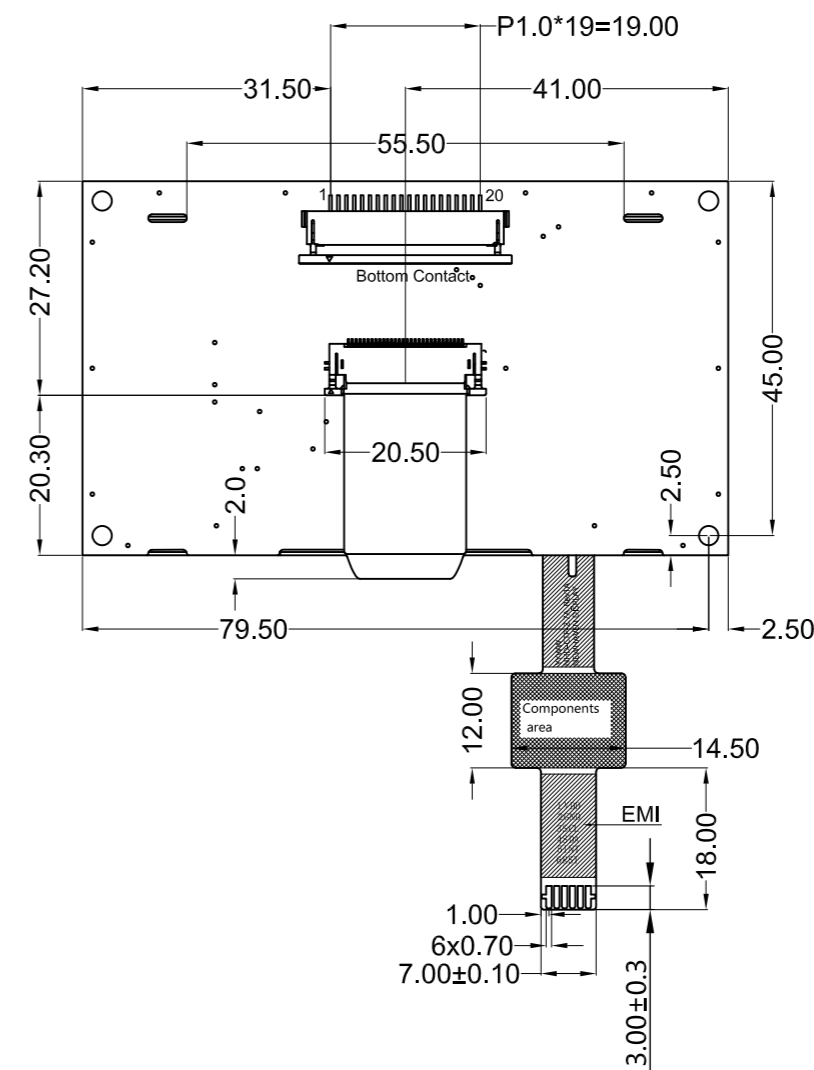
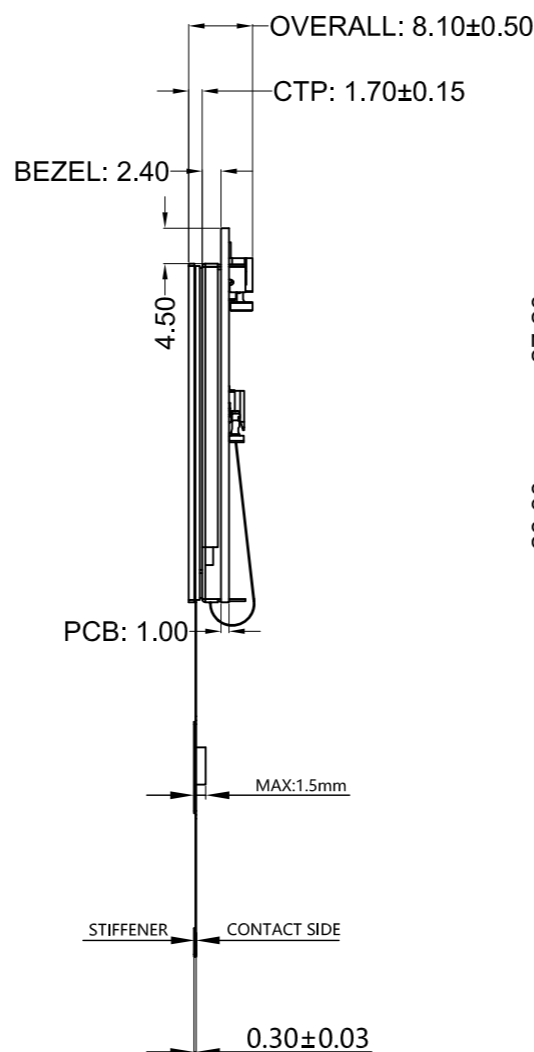
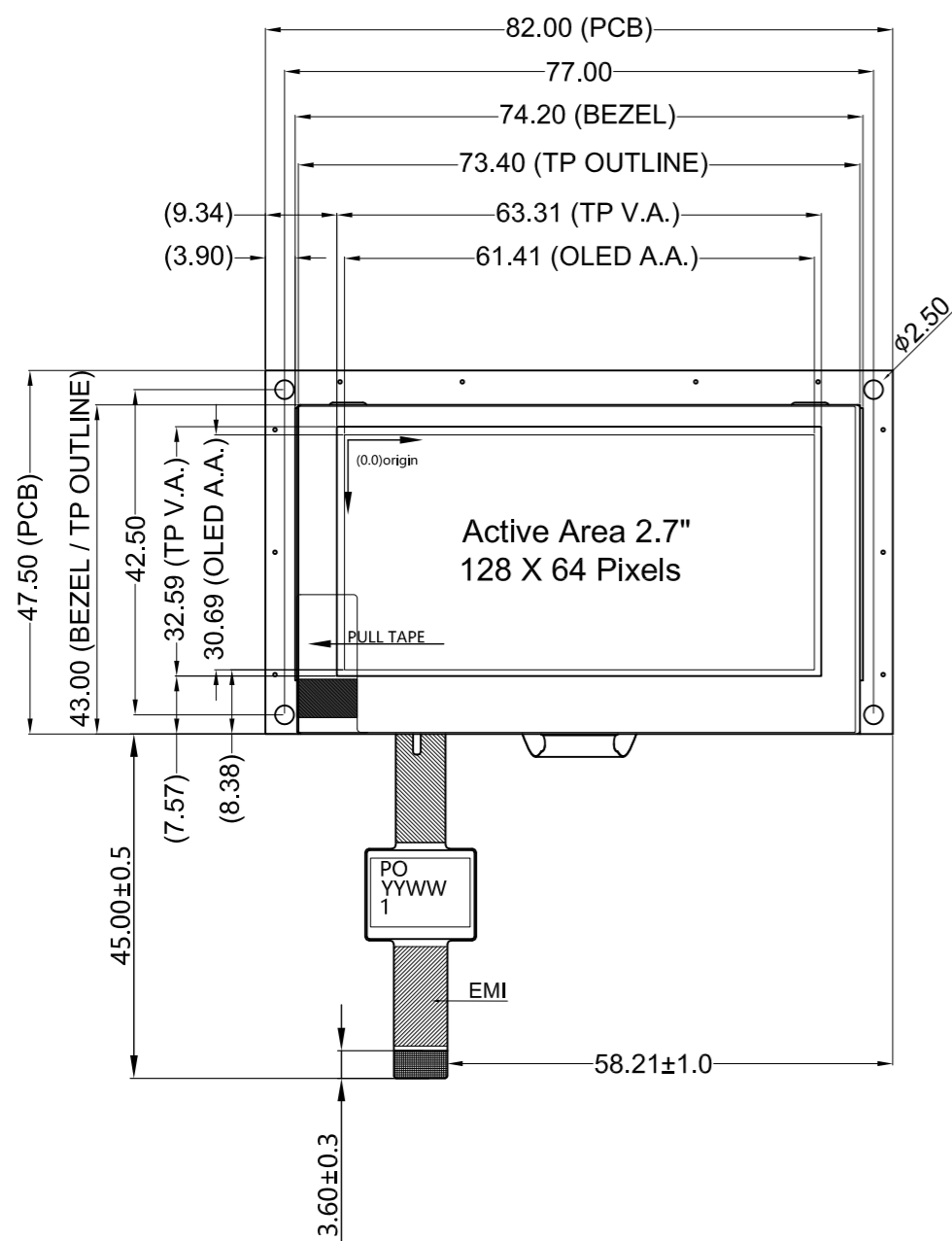
Mechanical Drawing

Newhaven Display

NHD-2.7-12864WDY3M-CTP

Date Code

Part Label (type/format may vary)



OLED

Pin No.	Symbol
1	Vss
2	Vdd
3	NC (BC_VDD)
4	D/C
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	N.C. (Vcc)
16	/RES
17	/CS
18	/SHDN (N.C.)
19	BS1
20	BS0

CTP

PIN	DEFINE
1	VDD 3.3V
2	GND
3	SCL 3.3V
4	SDA 3.3V
5	INT 3.3V
6	RESET 3.3V

Product Description: 2.7" 128x64 Graphic OLED w/ Capacitive Touch

1. Driver IC: SSD1322 OLED, FT5426-003 CTP
2. Interface: 8-bit 6800/8080 Parallel, 3/4-wire SPI OLED, I²C CTP
3. Power Requirement: 3.3V OLED, 3.3V CTP
4. Optical Features: Yellow Color, Full View
5. Recommended OLED Cable: 20pin 1.0mm pitch FFC; Ex. Molex 52271-2079
6. Recommended CTP Connector: 6pin 1.0mm pitch; Ex. Molex 52271-0679
7. EMI Shielded FPC

Standard Tolerance: (Unless otherwise specified) Linear: ±0.3mm		
	Drawing/Part Number: NHD-2.7-12864WDY3M-CTP	Revision: -
Unless otherwise specified: • Dimensions are in Millimeters • Third Angle Projection	Drawn By: K. Lewis	Approved By: K. Lewis
	Drawn Date: 07/13/2023	Approved Date: 07/13/2023
This drawing is solely the property of Newhaven Display International, Inc. The information it contains is not to be disclosed, reproduced or copied in whole or part without written approval from Newhaven Display.		

Pin Description

Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	V _{SS}	Power Supply	Ground
2	V _{DD}	Power Supply	Supply Voltage for OLED module
3	N.C. (BC_V _{DD})	-	No Connect by default. Can be configured to provide independent supply voltage (2.8V – 12V DC) for boost converter. (refer to On-Board Jumper Options table below)
4	D/C	MPU	Data/Command select signal, D/C=0: Command; D/C=1: Data (tie LOW for 3-wire Serial Interface)
5	R/W or /WR	MPU	6800-interface: Read/Write select signal, R/W=1: Read, R/W=0: Write 8080-interface: Active LOW Write signal
6	E or /RD	MPU	6800-interface: Operation Enable signal Active High 8080-interface: Active LOW Read signal
7-14	DB0 – DB7	MPU	8-bit bi-directional Data Bus
15	N.C. (VCC)	-	No Connect by default. Can be configured for external VCC (+15V). (refer to On-Board Jumper Options section below)
16	/RES	MPU	Active LOW Reset signal
17	/CS	MPU	Active LOW Chip Select signal
18	/SHDN (N.C.)	MPU	Active LOW Shutdown control pin for boost converter (pulled HIGH via on-board 15kΩ resistor) Can be made a No Connect by removing resistor R1.
19	BS1	MPU	MPU Interface select signal
20	BS0	MPU	MPU Interface select signal

Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	V _{SS}	Power Supply	Ground
2	V _{DD}	Power Supply	Supply Voltage for OLED module
3	N.C. (BC_V _{DD})	-	No Connect by default. Can be configured to provide independent supply voltage (2.8V – 12V DC) for boost converter. (refer to On-Board Jumper Options table below)
4	D/C	MPU	Data/Command select signal, D/C=0: Command; D/C=1: Data (tie LOW for 3-wire Serial Interface)
5-6	V _{SS}	Power Supply	Ground
7	SCLK	MPU	Serial Clock signal
8	SDIN	MPU	Serial Data Input signal
9	N.C.	-	No Connect
10-14	V _{SS}	Power Supply	Ground
15	N.C. (VCC)	-	No Connect by default. Can be configured for external VCC (+15V). (refer to On-Board Jumper Options section below)
16	/RES	MPU	Active LOW Reset signal
17	/CS	MPU	Active LOW Chip Select signal
18	/SHDN (N.C.)	MPU	Active LOW Shutdown control pin for boost converter (pulled HIGH via on-board 15kΩ resistor) Can be made a No Connect by removing resistor R1.
19	BS1	MPU	MPU Interface select signal
20	BS0	MPU	MPU Interface select signal



Capacitive Touch Panel:

Pin No.	Symbol	External Connection	Function Description
1	V _{DD}	Power Supply	Supply voltage for Logic (3.3V)
2	V _{SS}	Power Supply	Ground
3	SCL	MPU	Serial I2C Clock (Requires 4.7KΩ pull-up resistor)
4	SDA	MPU	Serial I2C Data (Requires 4.7kΩ pull-up resistor)
5	/INT	MPU	Interrupt signal from touch panel module to host
6	/RESET	MPU	Active LOW Reset signal

Recommended connector: 6pin, 1.0mm pitch, FFC connector. Molex P/N 52271-0679

Interface Selection

MPU Interface Pin Selections

Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	3-wire Serial Interface	4-wire Serial Interface
BS1	1	1	0	0
BS0	1	0	1	0

MPU Interface Pin Assignment Summary

Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	Tie LOW	/RES
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	D/C	/RES

On-Board Jumper Options

Default Jumper Setting

R4	R5	R7	Description
Close	Open	Open	(default) OLED controller and boost converter + OLED panel are powered from VDD (pin #2). This allows the full module to be powered by a single low-voltage supply.

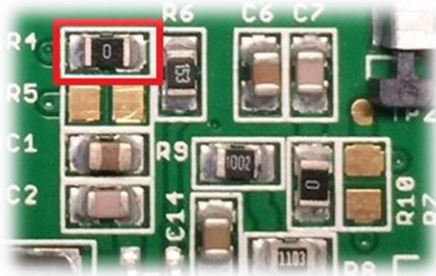
Jumper Option #1 - Independent Supply Voltage for Boost Converter (BC_VDD)

R4	R5	R7	Description
Open	Close	Open	Boost converter + OLED panel are powered from BC_VDD (pin #3). OLED controller is still powered from VDD (pin #2). This allows for increased efficiency through the boost converter, by allowing a supply voltage up to +12V at its input, BC_VDD (pin #3).

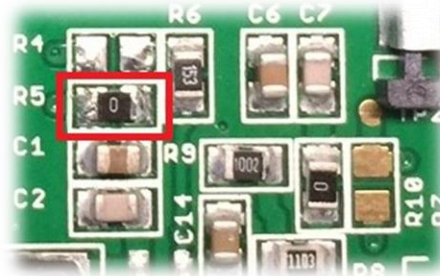
Jumper Option #2 – External Supply Voltage for OLED Panel (VCC)

R4	R5	R7	Description
Open	Open	Close	OLED panel is powered from VCC (pin #15) – boost converter is not used. OLED controller is still powered from VDD (pin #2). This allows for maximum module efficiency, and drastically reduced total current consumption.

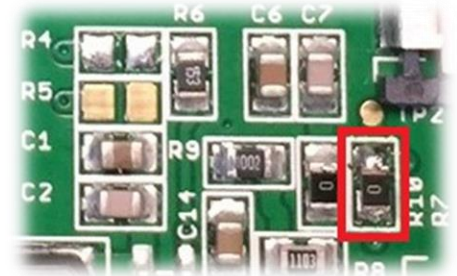
Default Jumper Setting



Jumper Option #1



Jumper Option #2



For detailed electrical information on each jumper option, please see the Electrical Characteristics table below.

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T _{OP}	Absolute Max	-40	-	+85	°C
Storage Temperature Range	T _{ST}	Absolute Max	-40	-	+85	°C
Default Jumper Setting						
Supply Voltage for Module	V_{DD}	-	2.8	3.3	3.5	V
Supply Current for Module	I_{DD}	VDD=3.3V, 100% ON	-	330	360	mA
Jumper Option #1						
Supply Voltage for Module	V _{DD}	-	2.8	3.3	3.5	V
Supply Current for Module	I _{DD}	VDD=3.3V	-	180	295	μA
Supply Voltage for Boost Converter	BC_V _{DD}	-	2.8	-	12	V
Supply Current for Boost Converter	BC_I _{DD}	BC_VDD=5.0V, 100% ON	-	190	205	mA
		BC_VDD=12.0V, 100% ON	-	70	80	mA
Jumper Option #2						
Supply Voltage for Module	V _{DD}	-	2.8	3.3	3.5	V
Supply Current for Module	I _{DD}	V _{DD} =3.3V	-	180	300	μA
Supply Voltage for OLED Panel	V _{CC}	-	14.5	15	15.5	V
Supply Current for OLED Panel	I _{CC}	V _{CC} =15V, 50% ON	-	35	40	mA
		V _{CC} =15V, 100% ON	-	50	60	mA
Sleep Mode Current	I _{DD_SLEEP}	-	-	25	120	μA
"H" Level input	V _{IH}	-	0.8 * V _{DD}	-	V _{DD}	V
"L" Level input	V _{IL}	-	V _{SS}	-	0.2 * V _{DD}	V
"H" Level output	V _{OH}	-	0.9 * V _{DD}	-	V _{DD}	V
"L" Level output	V _{OL}	-	V _{SS}	-	0.1 * V _{DD}	V

Note: The electrical characteristics shown above for Jumper Option #1 and Jumper Option #2 apply only when the on-board jumpers are configured accordingly. By default, only Default Jumper Setting supply voltage and current (in bold) need to be considered. For details, see On-Board Jumper Options section on previous page.

Capacitive Touch Panel:

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T _{OP}	Absolute Max	-40	-	+85	°C
Storage Temperature Range	T _{ST}	Absolute Max	-40	-	+85	°C
Supply Voltage	V _{DD}	-	2.8	-	3.3	V
Supply Current – Operating	I _{DD}	-	-	15	23	mA
"H" Level input	V _{IH}	-	0.7*V _{DD}	-	V _{DD}	V
"L" Level input	V _{IL}	-	V _{SS}	-	0.3*V _{DD}	V
"H" Level output	V _{OH}	-	0.7*V _{DD}	-	V _{DD}	V
"L" Level output	V _{OL}	-	V _{SS}	-	0.3*V _{DD}	V

Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	$\phi Y+$	-	-	85	-	°
	Bottom	$\phi Y-$		-	85	-	°
	Left	$\theta X-$		-	85	-	°
	Right	$\theta X+$		-	85	-	°
Contrast Ratio		C_r	-	>10,000:1	-	-	-
Response Time	Rise	T_R	-	-	15	-	ns
	Fall	T_F	-	-	15	-	ns
Brightness		L_V	50% Checkerboard	60	80	-	cd/m ²
Lifetime		-	$T_{OP}=25^{\circ}C, L_V=80cd/m^2$	60,000	-	-	hrs
		-	$T_{OP}=25^{\circ}C, L_V=60cd/m^2$	100,000	-	-	hrs

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. To extend the life of the display, lower values may be used for the contrast setting registers – see below table of commands for details.

Driver/Controller Information

Built-in SSD1322 Source Driver: <https://support.newhavendisplay.com/hc/en-us/articles/4414477846679-SSD1322>

Built-in FT5426-003 Controller: <https://support.newhavendisplay.com/hc/en-us/articles/4414392845079-FT5x26>

Table of Commands

Instruction	Code										Description	RESET value
	D/C	HEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Enable Grayscale Table	0	00	0	0	0	0	0	0	0	0	Enable the Grayscale table settings. (see command 0xB8)	
Set Column Address	0	15	0	0	0	1	0	1	0	1	Set column start and end address A[6:0]: Column start address. Range: 0-119d B[6:0]: Column end address. Range: 0-119d	0 119d
	1	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
	1	B[6:0]	*	B6	B5	B4	B3	B2	B1	B0		
Write RAM Command	0	5C	0	1	0	1	1	1	0	0	Enable MCU to write Data into RAM	
Read RAM Command	0	5D	0	1	0	1	1	1	0	1	Enable MCU to read Data from RAM	
Set Row Address	0	75	0	1	1	1	0	1	0	1	Set row start and end address A[6:0]: Row start address. Range: 0-127d B[6:0]: Row end address. Range: 0-127d	0 127d
	1	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
	1	B[6:0]	*	B6	B5	B4	B3	B2	B1	B0		
Set Re-map	0	A0	1	0	1	0	0	0	0	0	A[0] = 0; Horizontal Address Increment A[0] = 1; Vertical Address Increment A[1] = 0; Disable Column Address remap A[1] = 1; Enable Column Address remap A[2] = 0; Disable Nibble remap A[2] = 1; Enable Nibble remap A[4] = 0; Scan from COM0 to COM[N-1] A[4] = 1; Scan from COM[N-1] to COM0 A[5] = 0; Disable COM split Odd/Even A[5] = 1; Enable COM split Odd/Even B[4] = 0; Disable Dual COM mode B[4] = 1; Enable Dual COM mode Note: A[5] must be 0 if B[4] is 1.	0 0 0 0 0 0
	1	A[5:0]	0	0	A5	A4	0	A2	A1	A0		
	1	B[4]	*	*	0	B4	0	0	0	1		
Set Display Start Line	0	A1	1	0	1	0	0	0	0	1	Set display RAM display start line register from 0-127.	0
	1	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
Set Display Offset	0	A2	1	0	1	0	0	0	1	0	Set vertical shift by COM from 0~127.	0
	1	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
Display Mode	0	A4~A7	1	0	1	0	0	X2	X1	X0	0xA4 = Entire display OFF 0xA5 = Entire display ON, all pixels Grayscale level 15 0xA6 = Normal display 0xA7 = Inverse display	0xA6
Enable Partial Display	0	A8	1	0	1	0	1	0	0	0	Turns ON partial mode. A[6:0] = Address of start row B[6:0] = Address of end row (B[6:0] > A[6:0])	
	1	A[6:0]	0	A6	A5	A4	A3	A2	A1	A0		



	1	B[6:0]	0	B6	B5	B4	B3	B2	B1	B0		
Exit Partial Display	0	A9	1	0	1	0	1	0	0	1	Exit Partial Display mode	
Function Selection	0	AB	1	0	1	0	1	0	1	1	A[0] = 0; External VDD	1
	1	A[0]	0	0	0	0	0	0	0	A0	A[0] = 1; Internal VDD regulator	
Set Sleep Mode ON/OFF	0	AE~AF	1	0	1	0	1	1	1	X0	0xAE = Sleep Mode ON (display OFF) 0xAF = Sleep Mode OFF (display ON)	
Set Phase Length	0	B1	1	0	1	1	0	0	0	1	A[3:0] = P1. Phase 1 period of 5-31 DCLK clocks	9
	1	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0	A[7:4] = P2. Phase 2 period of 3-15 DCLK clocks	7
Set Display Clock Divide Ratio / Oscillator Frequency	0	B3	1	0	1	1	0	0	1	1	A[3:0] = 0000; divide by 1	0
	1	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0	A[3:0] = 0001; divide by 2	
											A[3:0] = 0010; divide by 4	
											A[3:0] = 0011; divide by 8	
											A[3:0] = 0100; divide by 16	
											A[3:0] = 0101; divide by 32	
											A[3:0] = 0110; divide by 64	
											A[3:0] = 0111; divide by 128	
											A[3:0] = 1000; divide by 256	
											A[3:0] = 1001; divide by 512	
											A[3:0] = 1010; divide by 1024	
											A[3:0] >= 1011; invalid	
											A[7:4] = Set the Oscillator Frequency. Frequency increases with the value of A[7:4]. Range 0000b~1111b.	
VSL / Display Enhancement	0	B4	1	0	1	1	0	1	0	0	A[1:0] = 00b; Enable external VSL	10b
	1	A[1:0]	1	0	1	0	0	0	A1	A0	A[1:0] = 10b; Internal VSL	
	1	B[7:3]	B7	B6	B5	B4	B3	1	0	1	B[7:3] = 11111b; Enhanced low GS display quality B[7:3] = 10110b; Normal	
Set GPIO	0	B5	1	0	1	1	0	1	0	1	A[1:0] = 00; GPIO0 input disabled	10b
	1	A[3:0]	*	*	*	*	A3	A2	A1	A0	A[1:0] = 01; GPIO0 input enabled	
											A[1:0] = 10; GPIO0 output LOW	10b
											A[1:0] = 11; GPIO0 output HIGH	
											A[3:2] = 00; GPIO1 input disabled	
											A[3:2] = 01; GPIO1 input enabled	
											A[3:2] = 10; GPIO1 output LOW	10b
											A[3:2] = 11; GPIO1 output HIGH	
Set Second Pre-charge Period	0	B6	1	0	1	1	0	1	1	0	Sets the second precharge period	1000b
	1	A[3:0]	*	*	*	*	A3	A2	A1	A0	A[3:0] = DCLKs	
Set Grayscale Table	0	B8	1	0	1	1	1	0	0	0	Sets the gray scale pulse width in units of DCLK. Range 0-180d.	
	1	A1[7:0]	A17	A16	A15	A14	A13	A12	A11	A10	A1[7:0] = Gamma Setting for GS1	
	1	A2[7:0]	A27	A26	A25	A24	A23	A22	A21	A20	A2[7:0] = Gamma Setting for GS2	
	1	
	1	

	1 1 1 1	. . A14[7:0] A15[7:0]	. . A14₇ A15₇	. . A14₆ A15₆	. . A14₅ A15₅	. . A14₄ A15₄	. . A14₃ A15₃	. . A14₂ A15₂	. . A14₁ A15₁	. . A14₀ A15₀	. . A14[7:0] = Gamma Setting for GS14 A15[7:0] = Gamma Setting for GS15 Note: 0 < GS1 < GS2 < GS3 ... < GS14 < GS15 The setting must be followed by command 0x00.	
Select Default Linear Gray Scale Table	0 1	B9 A[4:0]	1 *	0 *	1 *	1 A4	1 A3	0 A2	0 A1	1 A0	Sets Linear Grayscale table GS0 pulse width = 0 GS0 pulse width = 0 GS0 pulse width = 8 GS0 pulse width = 16 GS0 pulse width = 104 GS0 pulse width = 112	
Set Pre-charge Voltage	0 1	BB A[4:0]	1 *	0 *	1 *	1 A4	1 A3	0 A2	1 A1	1 A0	Set precharge voltage level. A[4:0] = 0x00; 0.20*VCC . . A[4:0] = 0x3E; 0.60*VCC	0x17
Set VCOMH Voltage	0 1	BE A[3:0]	1 *	0 *	1 *	1 *	1 A3	1 A2	1 A1	0 A0	Sets the VCOMH voltage level A[3:0] = 0x00; 0.72*VCC . . A[3:0] = 0x04; 0.8*VCC . . A[3:0] = 0x07; 0.86*VCC	0x04
Set Contrast Control	0 1	C1 A[7:0]	1 A7	1 A6	0 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases.	0x7F
Master Contrast Control	0 1	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A3	1 A2	1 A1	1 A0	A[3:0] = 0x00; Reduce output for all colors to 1/16 A[3:0] = 0x01; Reduce output for all colors to 2/16 . . A[3:0] = 0x0E; Reduce output for all colors to 15/16 A[3:0] = 0x0F; no change	0x0f
Set Multiplex Ratio	0 1	CA A[6:0]	1 *	1 A6	0 A5	0 A4	1 A3	0 A2	1 A1	0 A0	Set MUX ratio to N+1 MUX N=A[6:0]; from 16MUX to 128MUX (0 to 14 are invalid)	127d
Set Command Lock	0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A2	0 1	1 0	A[2] = 0; Unlock OLED to enable commands A[2] = 1; Lock OLED from entering commands	0x12

Capacitive Touch Panel Registers

Register No.	Access	Register Name	Bits	Value	Description
01h	RO	Gesture ID	[7:0]	1Ch	Swipe Up
				14h	Swipe Down
				10h	Swipe Left
				18h	Swipe Right
				49h	Zoom Out
				48h	Zoom In
				00	No gesture
02h	RO	Touch Points	[7:0]	0-Ah	0: No touch detected A: 10 touch points detected
03h	RO	TOUCH1_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
03h	RO	TOUCH1_XH	[3:0]	0-1	Upper 4 bits of X touch coordinate
04h	RO	TOUCH1_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
05h	RO	TOUCH1_YH	[3:0]	0-1	Upper 4 bits of Y touch coordinate
06h	RO	TOUCH1_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
07h	RO	TOUCH1_Weight	[7:0]		Touch Weight
08h	RO	TOUCH1_Misc	[3:0]	00-0Fh	Touch Area
09h	RO	TOUCH2_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
09h	RO	TOUCH1_XH	[3:0]	0-1	Upper 4 bits of X touch coordinate
0Ah	RO	TOUCH2_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
0Bh	RO	TOUCH2_YH	[3:0]	0-1	Upper 4 bits of Y touch coordinate
0Ch	RO	TOUCH2_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
0Dh	RO	TOUCH2_Weight	[7:0]		Touch Weight
0Eh	RO	TOUCH2_Misc	[3:0]	00-0Fh	Touch Area
0Fh	RO	TOUCH3_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
0Fh	RO	TOUCH3_XH	[3:0]	0-1	Upper 4 bits of X touch coordinate
10	RO	TOUCH3_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
11h	RO	TOUCH3_YH	[3:0]	0-1	Upper 4 bits of Y touch coordinate
12h	RO	TOUCH3_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
13h	RO	TOUCH3_Weight	[7:0]		Touch Weight
14h	RO	TOUCH3_Misc	[3:0]	00-0Fh	Touch Area
15h	RO	TOUCH4_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
15h	RO	TOUCH4_XH	[3:0]	0-1	Upper 4 bits of X touch coordinate
16h	RO	TOUCH4_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
17h	RO	TOUCH4_YH	[3:0]	0-1	Upper 4 bits of Y touch coordinate
18h	RO	TOUCH4_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
1Ah	RO	TOUCH4_Misc	[3:0]	00-0Fh	Touch Area
1Bh	RO	TOUCH5_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved

Register No.	Access	Register Name	Bits	Value	Description
1Bh	RO	TOUCH5_XH	[3:0]	0 - 1	Upper 4 bits of X touch coordinate
1Ch	RO	TOUCH5_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
1Dh	RO	TOUCH5_YH	[3:0]	0 - 1	Upper 4 bits of Y touch coordinate
1Eh	RO	TOUCH5_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
1Fh	RO	TOUCH5_Weight	[7:0]		Touch Weight
20	RO	TOUCH5_Misc	[3:0]	00-0Fh	Touch Area
21h	RO	TOUCH6_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
21h	RO	TOUCH6_XH	[3:0]	0 - 1	Upper 4 bits of X touch coordinate
22h	RO	TOUCH6_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
23h	RO	TOUCH6_YH	[3:0]	0 - 1	Upper 4 bits of Y touch coordinate
24h	RO	TOUCH6_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
25h	RO	TOUCH6_Weight	[7:0]		Touch Weight
26h	RO	TOUCH6_Misc	[3:0]	00-0Fh	Touch Area
27h	RO	TOUCH7_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
27h	RO	TOUCH7_XH	[3:0]	0 - 1	Upper 4 bits of X touch coordinate
28h	RO	TOUCH7_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
29h	RO	TOUCH7_YH	[3:0]	0 - 1	Upper 4 bits of Y touch coordinate
2Ah	RO	TOUCH7_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
2Bh	RO	TOUCH7_Weight	[7:0]		Touch Weight
2Ch	RO	TOUCH7_Misc	[3:0]	00-0Fh	Touch Area
2Dh	RO	TOUCH8_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
2Dh	RO	TOUCH8_XH	[3:0]	0 - 1	Upper 4 bits of X touch coordinate
2Eh	RO	TOUCH8_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
2Fh	RO	TOUCH8_YH	[3:0]	0 - 1	Upper 4 bits of Y touch coordinate
30	RO	TOUCH8_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
31h	RO	TOUCH8_Weight	[7:0]		Touch Weight
32h	RO	TOUCH8_Misc	[3:0]	00-0Fh	Touch Area
33h	RO	TOUCH9_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
33h	RO	TOUCH9_XH	[3:0]	0 - 1	Upper 4 bits of X touch coordinate
34h	RO	TOUCH9_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
35h	RO	TOUCH9_YH	[3:0]	0 - 1	Upper 4 bits of Y touch coordinate
36h	RO	TOUCH9_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate
37h	RO	TOUCH9_Weight	[7:0]		Touch Weight
38h	RO	TOUCH9_Misc	[3:0]	00 - 0Fh	Touch Area
39h	RO	TOUCH10_Event_Flag	[7:6]	0	Put Down
				1	Put Up
				2	Contact
				3	Reserved
39h	RO	TOUCH10_XH	[3:0]	0 - 1	Upper 4 bits of X touch coordinate
3Ah	RO	TOUCH10_XL	[7:0]	00 - FFh	Lower 8 bits of X touch coordinate
3Bh	RO	TOUCH10_YH	[3:0]	0 - 1	Upper 4 bits of Y touch coordinate
3Ch	RO	TOUCH10_YL	[7:0]	00 - FFh	Lower 8 bits of Y touch coordinate

Register No.	Access	Register Name	Bits	Value	Description
3Dh	RO	TOUCH10_Weight	[7:0]	00-FFh	Touch Weight
3Eh	RO	TOUCH10_Misc	[3:0]	00-0Fh	Touch Area
A1h	RO	ID_G_LIB_VERSION_H	[7:0]	00-FFh	App library version high-byte Default: 0
A2h	RO	ID_G_LIB_VERSION_L	[7:0]	00-FFh	App library version low-byte Default: 2h
A3h	RO	ID_G_CHIPER_HIGH	[7:0]	00-FFh	Chip Vendor ID Default: 54h
A6h	RO	ID_G_FIRMID	[7:0]	00-FFh	Firmware ID Number Default: 1
A8h	RO	ID_G_VENODRID	[7:0]	00-FFh	CTPM Vendor's Chip ID Default: 79h

MPU Interface

6800-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, R/W, D/C, E, and /CS.

A LOW on R/W indicates write operation, and HIGH on R/W indicates read operation.

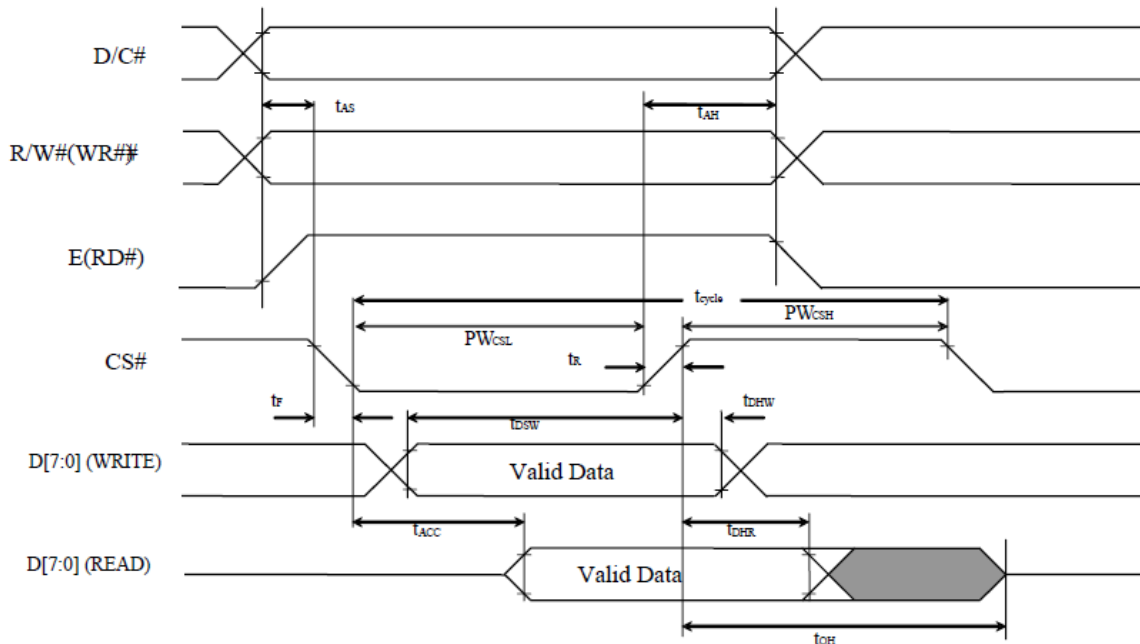
A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.

The E input serves as data latch signal, while /CS is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W	/CS	D/C
Write Command	↓	0	0	0
Read Status	↓	1	0	0
Write Data	↓	0	0	1
Read Data	↓	1	0	1

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, /RD, /WR, D/C, and /CS.

A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.

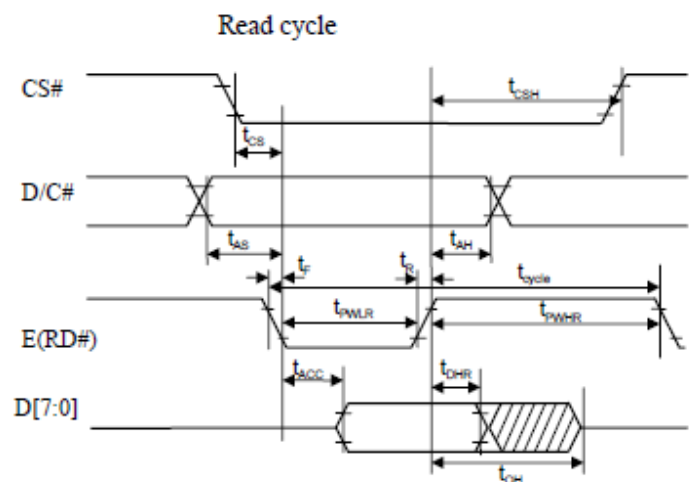
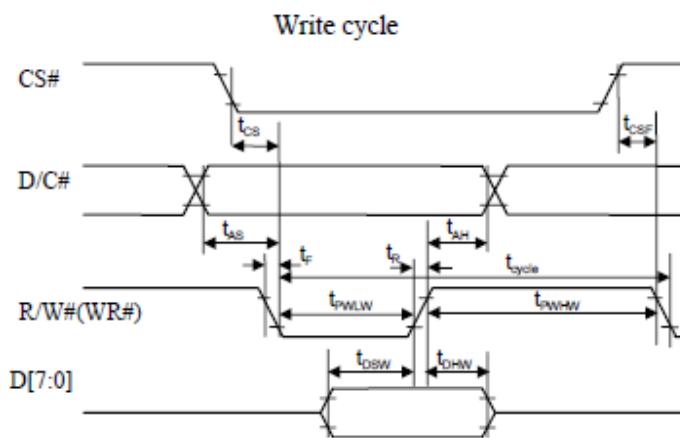
A rising edge of /RS input serves as a data read latch signal while /CS is LOW.

A rising edge of /WR input serves as a data/command write latch signal while /CS is LOW.

Function	/RD	/WR	/CS	D/C
Write Command	1	↑	0	0
Read Status	↑	1	0	0
Write Data	1	↑	0	1
Read Data	↑	1	0	1

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
$t_{PWL R}$	Read Low Time	150	-	-	ns
$t_{PWL W}$	Write Low Time	60	-	-	ns
$t_{PWH R}$	Read High Time	60	-	-	ns
$t_{PWH W}$	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns



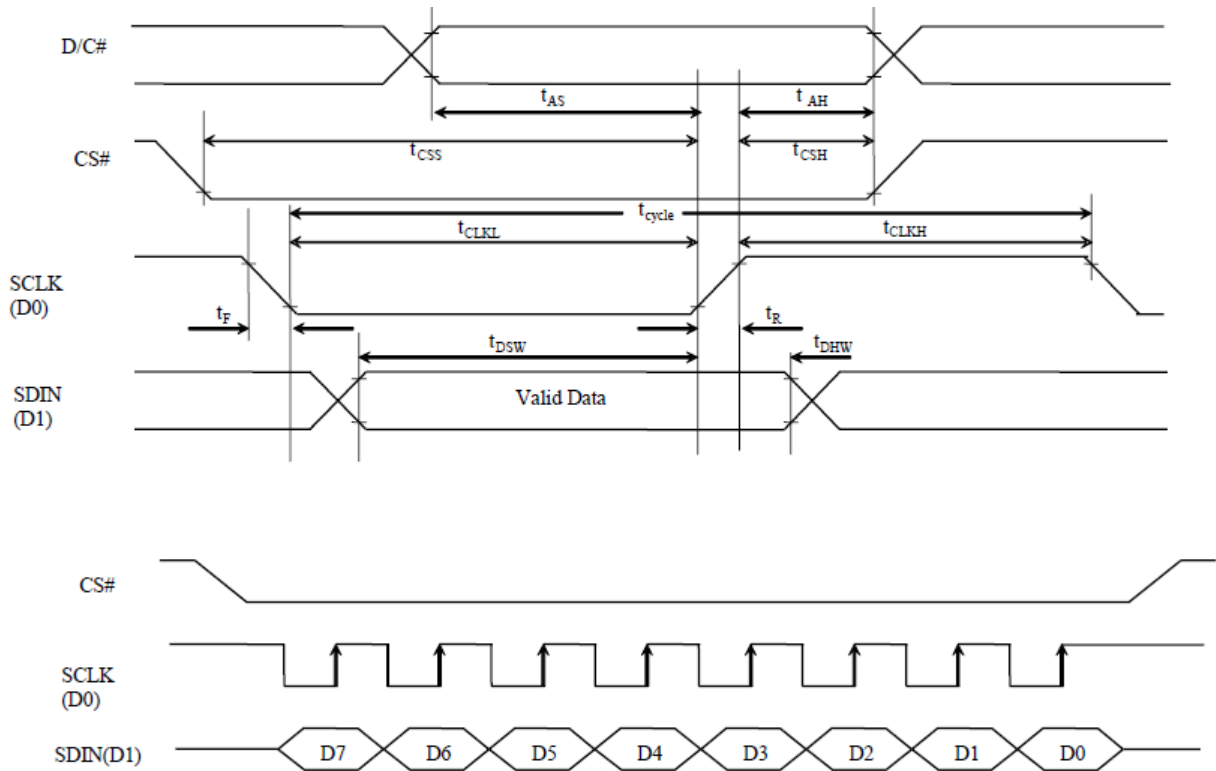
Serial Interface (4-wire)

The 4-wire serial interface consists of Serial Clock (SCLK), Serial Data (SDIN), Data/Command (D/C), and Chip Select (/CS). D0 acts as SCLK and D1 acts as SDIN. D2 must be left as a No Connect. D3~D7, E, and R/W should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	Tie LOW	Tie LOW	0	0	↑
Write Data	Tie LOW	Tie LOW	0	1	↑

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^{\circ}C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6...D0.

D/C is sampled on every eighth clock and the data byte in the shift register is written to the GDDRAM or command register in the same clock.

Note: Read functionality is not available in serial mode.

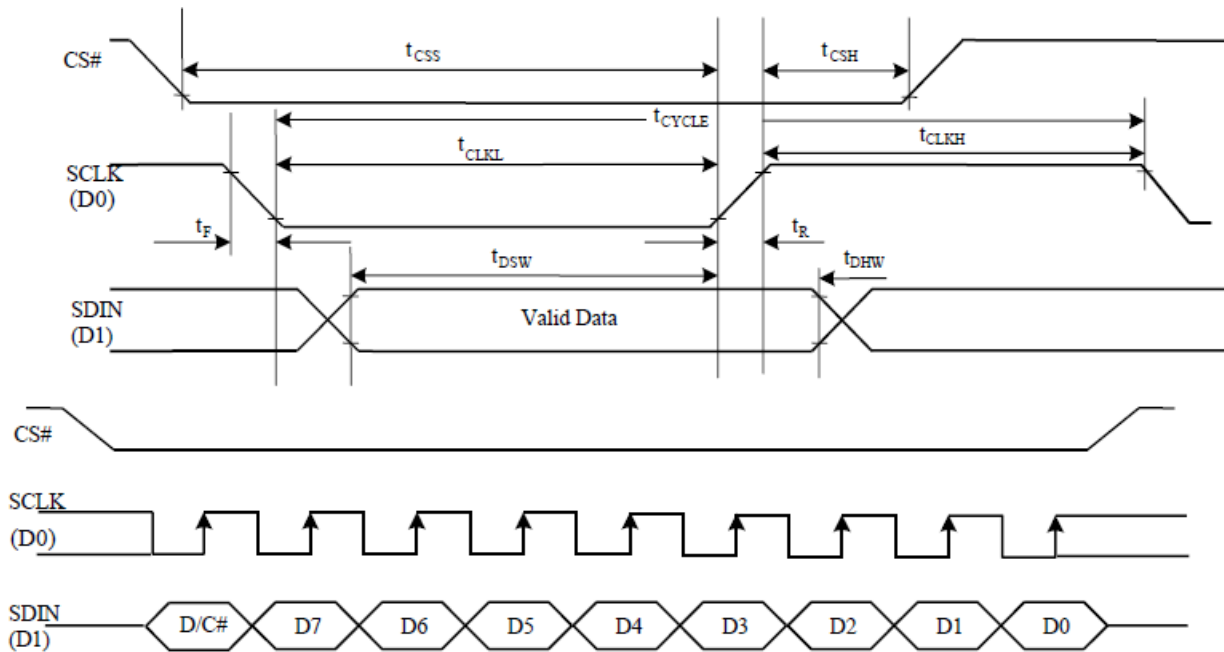
Serial Interface (3-wire)

The 3-wire serial interface consists of Serial Clock (SCLK), Serial Data In (SDIN), and Chip Select (/CS). D0 acts as SCLK and D1 acts as SDIN. D2 must be left as a No Connect. D3~D7, E, R/W, and D/C should be connected to Ground.

Function	/RD	/WR	/CS	D/C	D0
Write Command	Tie LOW	Tie LOW	0	Tie LOW	↑
Write Data	Tie LOW	Tie LOW	0	Tie LOW	↑

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

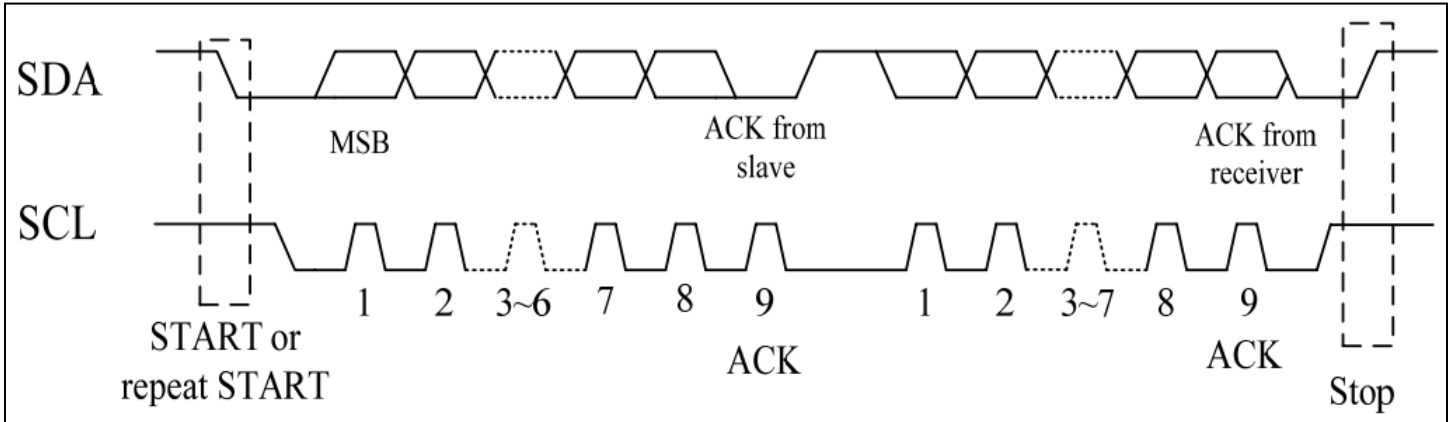


SDIN is shifted into an 9-bit shift register on every rising edge of SCLK in the order of D/C, D7, D6...D0. D/C (first bit of the sequential data) will determine if the following data byte is written to the Display Data RAM (D/C = 1) or the command register (D/C = 0).

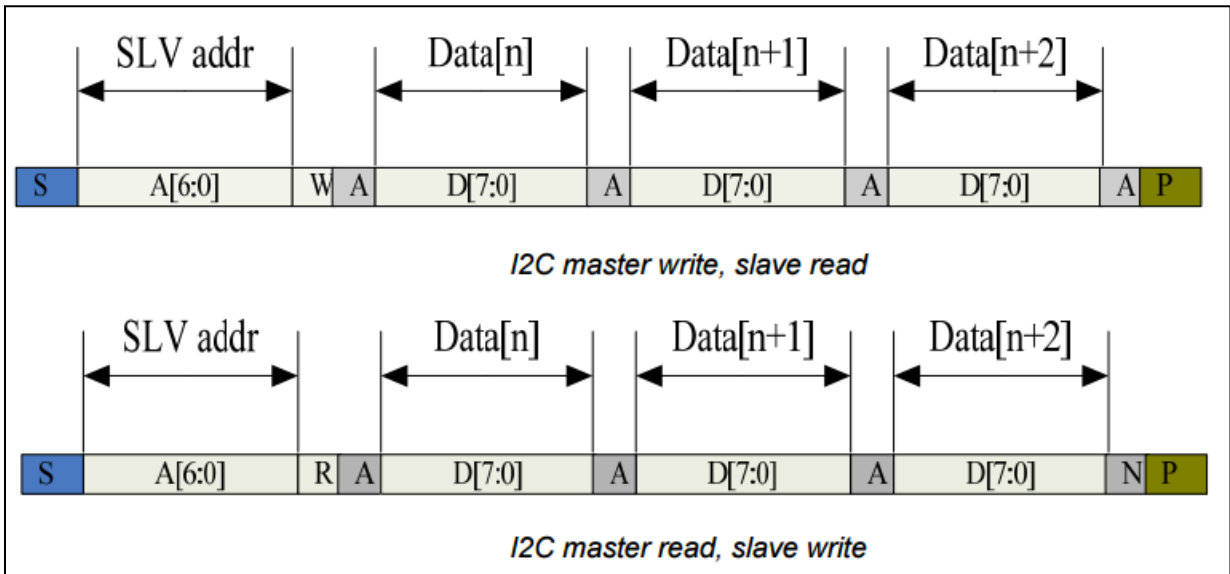
Note: Read functionality is not available in serial mode.

Timing Characteristics – Capacitive Touch Panel

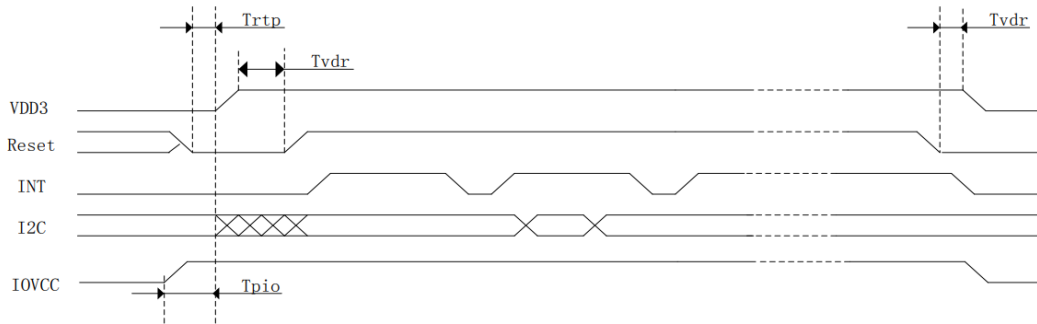
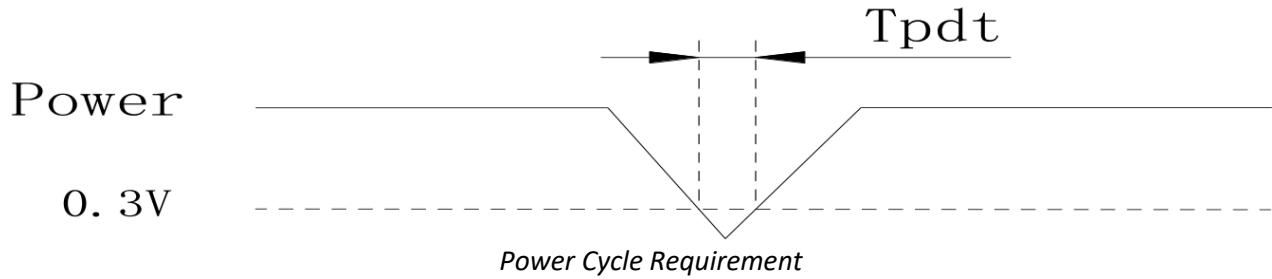
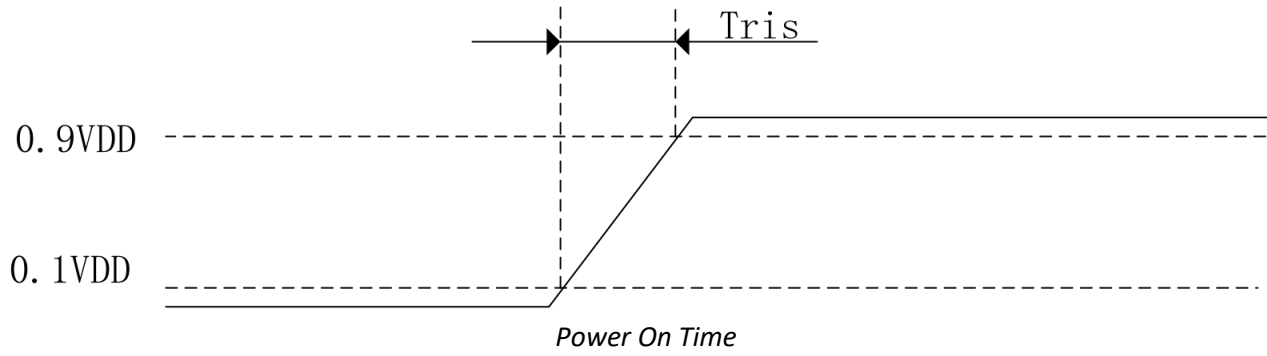
Data Transfer Format



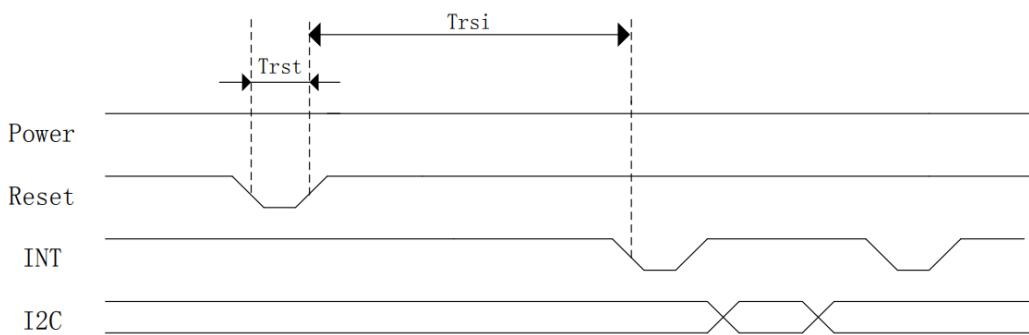
Parameter	Min	Max	Unit
SCL Frequency	0	400	KHz
Bus free time between a STOP & START condition	1.3	-	μs
Hold time Repeated START condition	0.6	-	μs
Data Setup Time	100	-	ns
Setup time for a repeated START condition	0.6	-	μs
Setup time for a STOP condition	0.6	-	μs



Power ON/Reset Sequence



Power ON Sequence

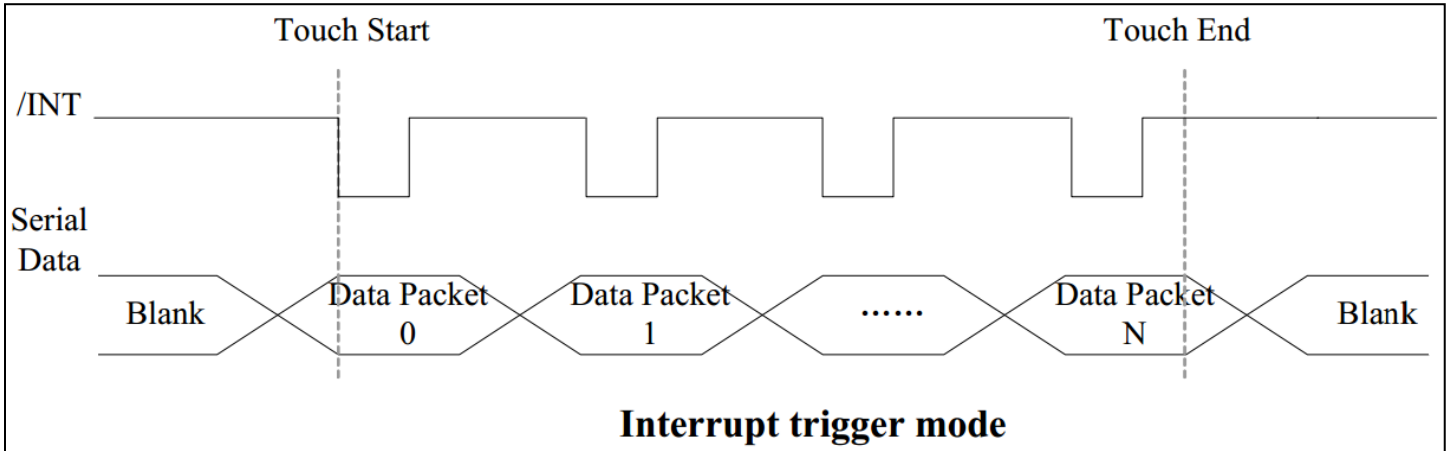


Reset sequence

Parameter	Description	Min	Max	Unit
Tris	Rise time from 0.1V _{DD} to 0.9V _{DD}	-	5	ms
T _{pdT}	Time of the voltage of supply being below 0.3V	5	-	ms
Trtp	Time of resetting to be low before powering on	100	-	μs
T _{pon}	Time to start reporting after power on	-	200	ms
Tvdr*	Reset time after applying V _{DD}	1	-	ms
Trsi	Time to start reporting after reset	-	200	ms
Trst*	Reset Time	1	-	ms

*Note: If Reset is tied to V_{DD} data corruption can occur





Sample code to read touch data:

```

i2c_start();
i2c_tx(0x70);           //Slave Address (Write)
i2c_tx(0x00);          //Start reading address
i2c_stop();

i2c_start();
i2c_tx(0x71);           //Slave Address (Read)
for(i=0x00;i<0x1F;i++)
{touchdata_buffer[i] = i2c_rx(1);}
i2c_stop();

```

Sample code to overwrite default register values:

```

i2c_start();
i2c_tx(0x70);           //Slave Address (Write)
i2c_tx(0xA4);           //ID_G_Mode
i2c_tx(0x01);           //Disable interrupt status to host
i2c_stop();

```

Recommended Initialization

```
void NHD12864WDY3_Init(void){
    digitalWrite(RESET, LOW);           //pull /RES (pin #16) low
    delayUS(200);                       //keep /RES low for minimum 200µs
    digitalWrite(RESET, HIGH);         //pull /RES high
    delayUS(200);                       //wait minimum 200µs before sending commands
    writeCommand(0xAE);                //display OFF
    writeCommand(0xB3);                //set CLK div. & OSC freq.
    writeData(0x91);
    writeCommand(0xCA);                //set MUX ratio
    writeData(0x3F);
    writeCommand(0xA2);                //set offset
    writeData(0x00);
    writeCommand(0xAB);                //function selection
    writeData(0x01);
    writeCommand(0xA0);                //set re-map
    writeData(0x16);
    writeData(0x11);
    writeCommand(0xC7);                //master contrast current
    writeData(0x0F);
    writeCommand(0xC1);                //set contrast current
    writeData(0x9F);
    writeCommand(0xB1);                //set phase length
    writeData(0xF2);
    writeCommand(0xBB);                //set pre-charge voltage
    writeData(0x1F);
    writeCommand(0xB4);                //set VSL
    writeData(0xA0);
    writeData(0xFD);
    writeCommand(0xBE);                //set VCOMH
    writeData(0x04);
    writeCommand(0xA6);                //set display mode
    writeCommand(0xAF);                //display ON
}
```

Example Software Routines

```

void setColumn(unsigned char xStart, unsigned char xEnd){
    writeCommand(0x15);    //set column (x-axis) start/end address
    writeData(xStart);    //column start; 28 is left-most column
    writeData(xEnd);      //column end; 91 is right-most column
}

void setRow(unsigned char yStart, unsigned char yEnd){
    writeCommand(0x75);    //set row (y-axis) start/end address
    writeData(yStart);    //row start; 0 is top row
    writeData(yEnd);      //row end; 63 is bottom row
}

void clearDisplay(void){
    unsigned int i;
    setColumn(28,91);     //set column (x-axis) start/end address
    setRow(0,63);        //set row (y-axis) start/end address
    writeRAM();          //single byte command (0x5C) to initiate pixel data write to GDDRAM;
    for(i=0;i<4096;i++){ // ((91-28)+1)*((63-0)+1)
        writeData(0x00);
        writeData(0x00);
    }
}

void write2Pixels(unsigned char xPos, unsigned char yPos, unsigned char pixel1, unsigned char pixel2){
    if(pixel1>=1) pixel1 = 0xFF;    //set 1st pixel value to ON
    else pixel1 = 0x00;            //set 1st pixel value to OFF
    if(pixel2>=1) pixel2 = 0xFF;    //set 2nd pixel value to ON
    else pixel2 = 0x00;            //set 2nd pixel value to OFF
    if(xPos>127) xPos = 127;       //boundary check (MIN xPos = 0, MAX xPos = 127)
    xPos = xPos/2;                //account for GDDRAM address mapping
    xPos+=28;                      //account for GDDRAM address mapping
    if(yPos>63) yPos = 63;        //boundary check (MIN yPos = 0, MAX yPos = 63)
    setColumn(xPos,xPos);         //set column (x-axis) start/end address
    setRow(yPos,yPos);            //set row (y-axis) start/end address
    writeRAM();                    //single byte command (0x5C) to initiate pixel data write to GDDRAM;
    writeData(pixel1);            //write 1st of 2 pixels to the display
    writeData(pixel2);            //write 2nd of 2 pixels to the display
}

void displayArray12864(const unsigned char arr[]){ //display 128x64 monochrome bitmap, horizontal pixel arrangement, 8-pixels per byte
    unsigned int i, j;
    setColumn(28,91);            //set column (x-axis) start/end address
    setRow(0,63);                //set row (y-axis) start/end address
    writeRAM();                  //single byte command (0x5C) to initiate pixel data write to GDDRAM;
    for(i=0;i<1024;i++){        //translate each byte/bit into pixel data
        for(j=0;j<8;j++){
            if(((arr[i]<<j)&0x80)==0x80){
                writeData(0xFF);
            }
            else{
                writeData(0x00);
            }
        }
    }
}

```


Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+85°C, 240hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-40°C, 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+85°C, 240hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-40°C, 240hrs	1,2
High Temperature / Humidity Storage	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+60°C, 90% RH, 240hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-40°C, 30min -> +25°C, 5min -> +85°C, 30min = 1 cycle 100 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-22Hz, 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X, Y, Z	3
Atmospheric Pressure Test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Endurance test applying electric static discharge.	Air: ±8KV; 300Ω, 150pF	
		Contact: ±4KV; 300Ω, 150pF	

Note 1: No condensation to be observed.

Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.

Evaluation Criteria:

- 1: Display is fully functional during operational tests and after all tests, at room temperature.
- 2: No observable defects.
- 3: Luminance >50% of initial value.
- 4: Current consumption within 50% of initial value

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