

# NHD-3.5-320240MF-22 Controller Board

## TFT Controller Evaluation Board

|         |   |
|---------|---|
| NHD-    | Newhaven Display  |
| 3.5-    | 3.5" Diagonal   |
| 320240- | 320xRGBx240 pixels                                      |
| MF-     | Model   |
| 22-     | 22-POS FFC interface (8-bit data)<br>SSD1963 Controller |

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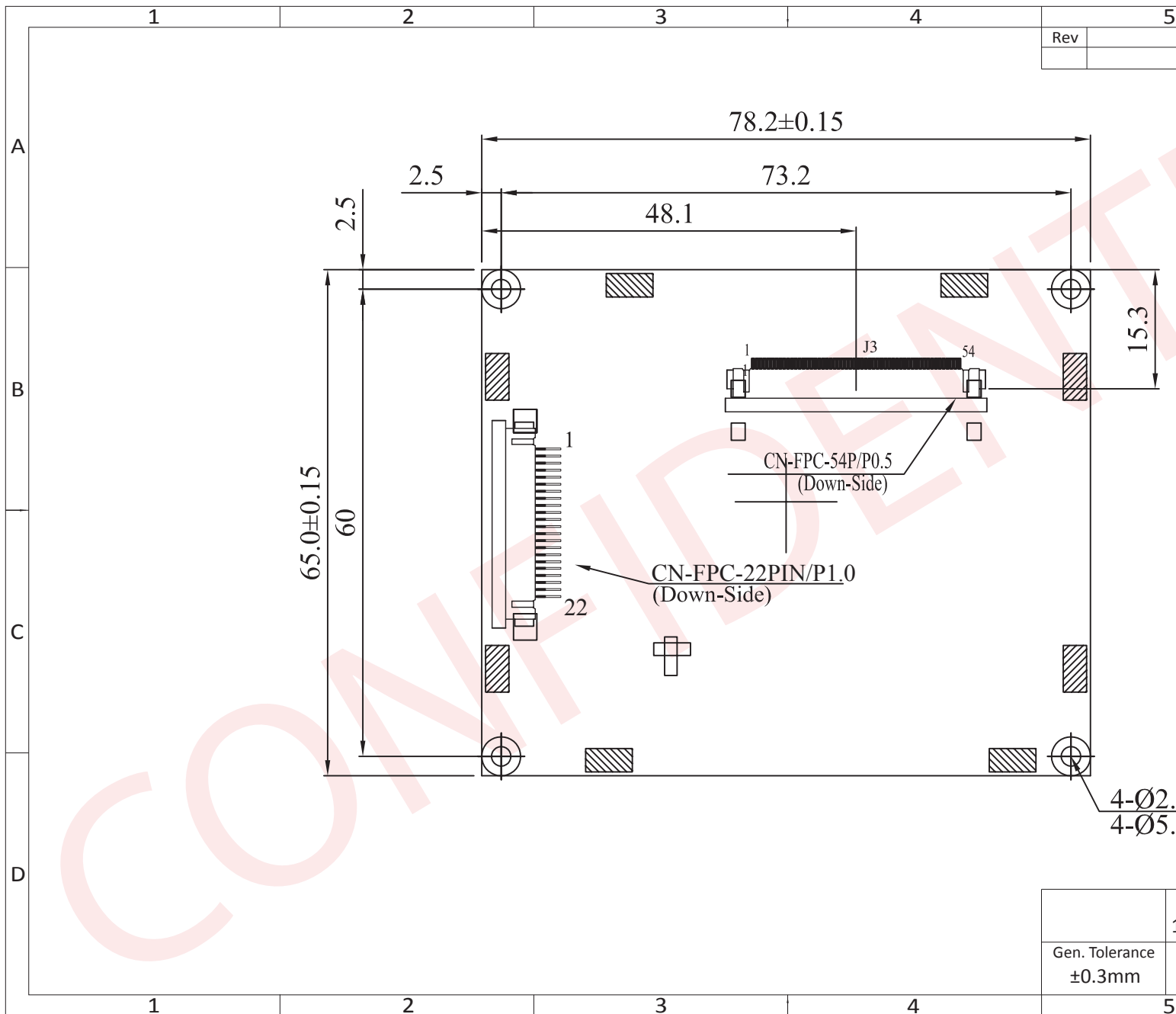
## Document Revision History

| Revision | Date       | Description                | Changed by |
|----------|------------|----------------------------|------------|
| 0        | 11/20/2012 | Initial Release            | AK         |
| 1        | 1/25/2013  | J2 Pin description updated | AK         |

## Functions and Features

- To use for testing, evaluating, or in final production with NHD-3.5-320240MF-A displays.

# Mechanical Drawing



|     |  |
|-----|--|
| Rev |  |
|-----|--|

|                |                    |
|----------------|--------------------|
| Gen. Tolerance | $\pm 0.3\text{mm}$ |
|----------------|--------------------|

## Pin Description

### J2 (SSD1963 input from user's MPU):

| Pin No. | Symbol     | External Connection | Function Description                       |
|---------|------------|---------------------|--|
| 1       | VSS        | Power Supply        | Ground                                     |
| 2       | VDD        | Power Supply        | Power supply for LCD and logic (3.3V)      |
| 3       | B/L Enable | Power Supply        | Backlight Enable                           |
| 4       | RS         | MPU                 | Register Select. RS=0: Command, RS=1: Data |
| 5       | /WR        | MPU                 | 8080 mode: Active LOW Write                |
| 6       | /RD        | MPU                 | 8080 mode: Active LOW Read                 |
| 7-14    | DB0-DB7    | MPU                 | 8-bit bidirectional data bus               |
| 15      | /CS        | MPU                 | Active LOW Chip Select                     |
| 16      | /RST       | MPU                 | Active LOW Reset                           |
| 17      | NC         | -                   | No Connect                                 |
| 18      | NC         | -                   | No Connect                                 |
| 19      | NC         | -                   | No Connect                                 |
| 20      | NC         | -                   | No Connect                                 |
| 21      | NC         | -                   | No Connect                                 |
| 22      | NC         | -                   | No Connect                                 |

### J3, J4 (SSD1963 output to display panel):

| Pin No. | Symbol  | External Connection | Function Description                       |
|---------|---------|---------------------|--|
| 1       | LED-    | LED Power Supply    | Ground for backlight                       |
| 2       | LED-    | LED Power Supply    | Ground for backlight                       |
| 3       | LED+    | LED Power Supply    | Power for backlight                        |
| 4       | LED+    | LED Power Supply    | Power for backlight                        |
| 5-7     | NC      | -                   | No Connect                                 |
| 8       | /RST    | MPU                 | Active LOW Reset                           |
| 9       | /CS     | -                   | Active LOW Serial Chip Select (No Connect) |
| 10      | SCL     | -                   | Serial Clock (No Connect)                  |
| 11      | SDA     | -                   | Serial Data (No Connect)                   |
| 12-19   | [B0-B7] | MPU                 | Blue Data                                  |
| 20-27   | [G0-G7] | MPU                 | Green Data                                 |
| 28-35   | [R0-R7] | MPU                 | Red Data                                   |
| 36      | HSYNC   | MPU                 | Horizontal (Line) Sync                     |
| 37      | VSYNC   | MPU                 | Vertical (Frame) Sync                      |
| 38      | DCLK    | MPU                 | Dot Clock                                  |
| 39-40   | NC      | -                   | No Connect                                 |
| 41      | VDD     | Power Supply        | Power supply for LCD and logic (3.3V)      |
| 42      | VDD     | Power Supply        | Power supply for LCD and logic (3.3V)      |
| 43-51   | NC      | -                   | No Connect                                 |
| 52      | DE      | -                   | Data Enable (No Connect)                   |
| 53      | VSS     | Power Supply        | Ground                                     |
| 54      | VSS     | Power Supply        | Ground                                     |

## Electrical Characteristics

| Item                        | Symbol | Condition    | Min.    | Typ. | Max.    | Unit |
|-----------------------------|--------|--------------|---------|------|---------|------|
| Operating Temperature Range | Top    | Absolute Max | -20     | -    | +70     | °C   |
| Storage Temperature Range   | Tst    | Absolute Max | -30     | -    | +80     | °C   |
| Supply Voltage              | VDD    |              | 3.0     | 3.3  | 3.6     | V    |
| Supply Current              | IDD    |              | -       | 25   | -       | mA   |
| Input High Voltage          | VIH    |              | 0.8*VDD | -    | VDD     | V    |
| Input Low Voltage           | VIL    |              | VSS     | -    | 0.2*VDD | V    |
| Backlight Voltage           | VLED   | ILED=20mA    | 18      | 19.2 | 20.4    | V    |
| Backlight Current           | ILED   |              | -       | 18   | 20      | mA   |

## Controller Information

Built-in SSD1963 controller

Please download specification at [http://www.newhavendisplay.com/app\\_notes/SSD1963.pdf](http://www.newhavendisplay.com/app_notes/SSD1963.pdf)

## MCU Interface

The controller board operates in 8080 mode. This interface uses /WR to define a write cycle and /RD for read cycle. If /WR goes low when the /CS signal is low, the data or command will be latched into the system at the rising edge of /WR. Similarly, the read cycle will start when /RD goes low and end at the rising edge of /RD.

### Pixel Data Format

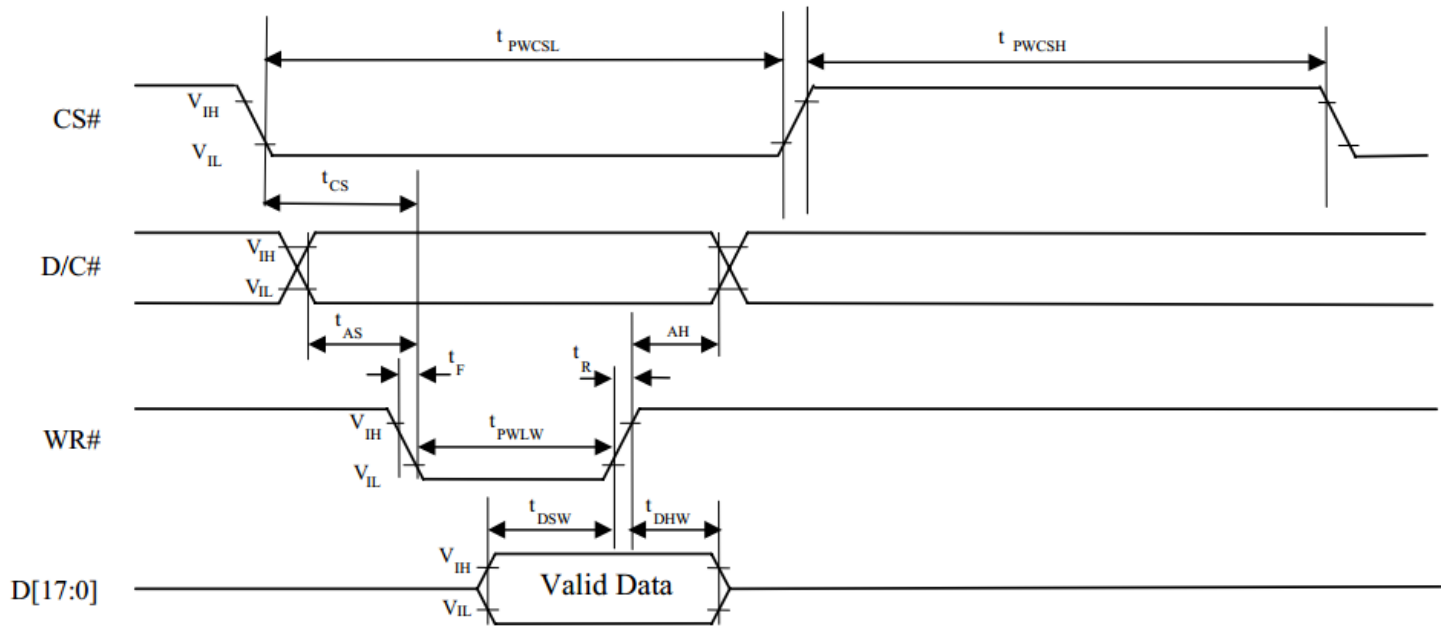
| Interface            | Cycle           | D[23] | D[22] | D[21] | D[20] | D[19] | D[18] | D[17] | D[16] | D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|----------------------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| 24 bits              | 1 <sup>st</sup> | R7    | R6    | R5    | R4    | R3    | R2    | R1    | R0    | G7    | G6    | G5    | G4    | G3    | G2    | G1   | G0   | B7   | B6   | B5   | B4   | B3   | B2   | B1   | B0   |
| 18 bits              | 1 <sup>st</sup> |       |       |       |       |       |       | R5    | R4    | R3    | R2    | R1    | R0    | G5    | G4    | G3   | G2   | G1   | G0   | B5   | B4   | B3   | B2   | B1   | B0   |
| 16 bits (565 format) | 1 <sup>st</sup> |       |       |       |       |       |       |       |       | R5    | R4    | R3    | R2    | R1    | G5    | G4   | G3   | G2   | G1   | G0   | B5   | B4   | B3   | B2   | B1   |
| 16 bits              | 1 <sup>st</sup> |       |       |       |       |       |       |       |       | R7    | R6    | R5    | R4    | R3    | R2    | R1   | R0   | G7   | G6   | G5   | G4   | G3   | G2   | G1   | G0   |
|                      | 2 <sup>nd</sup> |       |       |       |       |       |       |       |       | B7    | B6    | B5    | B4    | B3    | B2    | B1   | B0   | R7   | R6   | R5   | R4   | R3   | R2   | R1   | R0   |
|                      | 3 <sup>rd</sup> |       |       |       |       |       |       |       |       | G7    | G6    | G5    | G4    | G3    | G2    | G1   | G0   | B7   | B6   | B5   | B4   | B3   | B2   | B1   | B0   |
| 12 bits              | 1 <sup>st</sup> |       |       |       |       |       |       |       |       |       |       |       |       | R7    | R6    | R5   | R4   | R3   | R2   | R1   | R0   | G7   | G6   | G5   | G4   |
|                      | 2 <sup>nd</sup> |       |       |       |       |       |       |       |       |       |       |       |       | G3    | G2    | G1   | G0   | B7   | B6   | B5   | B4   | B3   | B2   | B1   | B0   |
| 9 bits               | 1 <sup>st</sup> |       |       |       |       |       |       |       |       |       |       |       |       |       |       |      | R5   | R4   | R3   | R2   | R1   | R0   | G5   | G4   | G3   |
|                      | 2 <sup>nd</sup> |       |       |       |       |       |       |       |       |       |       |       |       |       |       |      | G2   | G1   | G0   | B5   | B4   | B3   | B2   | B1   | B0   |
| 8 bits               | 1 <sup>st</sup> |       |       |       |       |       |       |       |       |       |       |       |       |       |       |      |      | R7   | R6   | R5   | R4   | R3   | R2   | R1   | R0   |
|                      | 2 <sup>nd</sup> |       |       |       |       |       |       |       |       |       |       |       |       |       |       |      |      | G7   | G6   | G5   | G4   | G3   | G2   | G1   | G0   |
|                      | 3 <sup>rd</sup> |       |       |       |       |       |       |       |       |       |       |       |       |       |       |      |      | B7   | B6   | B5   | B4   | B3   | B2   | B1   | B0   |

# Timing Characteristics

## Parallel 8080-series Interface Timing

| Symbol      | Parameter  | Min            | Typ  | Max | Unit |
|-------------|--|----------------|--|-----|------|
| $f_{MCLK}$  | System Clock Frequency*  | 1              | -  | 110 | MHz  |
| $t_{MCLK}$  | System Clock Period*   | $1/f_{MCLK}$   | -  | -   | ns   |
| $t_{PWCSL}$ | Control Pulse High Width<br>Write<br>Read  | 13<br>30       | $1.5 * t_{MCLK}$<br>$3.5 * t_{MCLK}$                 | -   | ns   |
| $t_{PWCSH}$ | Control Pulse Low Width<br>Write (next write cycle)<br>Write (next read cycle)<br>Read | 13<br>80<br>80 | $1.5 * t_{MCLK}$<br>$9 * t_{MCLK}$<br>$9 * t_{MCLK}$ | -   | ns   |
| $t_{AS}$    | Address Setup Time   | 1              | -  | -   | ns   |
| $t_{AH}$    | Address Hold Time  | 2              | -  | -   | ns   |
| $t_{DSW}$   | Write Data Setup Time  | 4              | -  | -   | ns   |
| $t_{DHW}$   | Write Data Hold Time   | 1              | -  | -   | ns   |
| $t_{PWLW}$  | Write Low Time   | 12             | -  | -   | ns   |
| $t_{DHR}$   | Read Data Hold Time  | 1              | -  | -   | ns   |
| $t_{ACC}$   | Access Time  | 32             | -  | -   | ns   |
| $t_{PWLR}$  | Read Low Time  | 36             | -  | -   | ns   |
| $t_R$       | Rise Time  | -              | -  | 0.5 | ns   |
| $t_F$       | Fall Time  | -              | -  | 0.5 | ns   |
| $t_{CS}$    | Chip select setup time   | 2              | -  | -   | ns   |
| $t_{CSH}$   | Chip select hold time to read signal   | 3              | -  | -   | ns   |

\* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)



## Quality Information

| Test Item                             | Content of Test   | Test Condition  | Note |
|---------------------------------------|---|---|------|
| High Temperature storage              | Endurance test applying the high storage temperature for a long time.   | +80°C , 200hrs  | 2    |
| Low Temperature storage               | Endurance test applying the low storage temperature for a long time.  | -30°C , 200hrs  | 1,2  |
| High Temperature Operation            | Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.                    | +70°C 200hrs  | 2    |
| Low Temperature Operation             | Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.                     | -20°C , 200hrs  | 1,2  |
| High Temperature / Humidity Operation | Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time. | +60°C , 90% RH , 96hrs  | 1,2  |
| Thermal Shock resistance              | Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.                  | -20°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle<br>10 cycles                       |      |
| Vibration test                        | Endurance test applying vibration to simulate transportation and use.   | 10-55Hz , 15mm amplitude.<br>60 sec in each of 3 directions X,Y,Z<br>For 15 minutes | 3    |
| Static electricity test               | Endurance test applying electric static discharge.  | VS=800V, RS=1.5kΩ, CS=100pF<br>One time   |      |

**Note 1:** No condensation to be observed.

**Note 2:** Conducted after 4 hours of storage at 25°C, 0%RH.

**Note 3:** Test performed on product itself, not inside a container.

## Precautions for using LCDs/LCMs

See Precautions at [www.newhavendisplay.com/specs/precautions.pdf](http://www.newhavendisplay.com/specs/precautions.pdf)

## Warranty Information and Terms & Conditions

[http://www.newhavendisplay.com/index.php?main\\_page=terms](http://www.newhavendisplay.com/index.php?main_page=terms)

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