

74ABT20

Dual 4-input NAND gate

Rev. 3 — 12 August 2016

Product data sheet

1. General description

The 74ABT20 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT20 is a dual 4-input NAND gate.

2. Features and benefits

- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT20D	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ABT20DB	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74ABT20PW	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

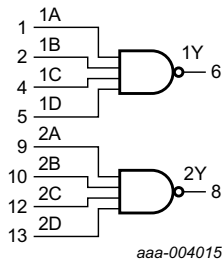


Fig 1. Logic symbol

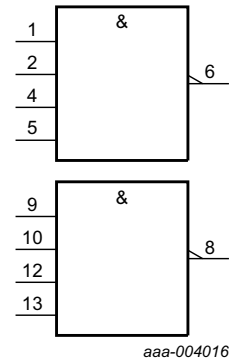


Fig 2. IEC Logic symbol

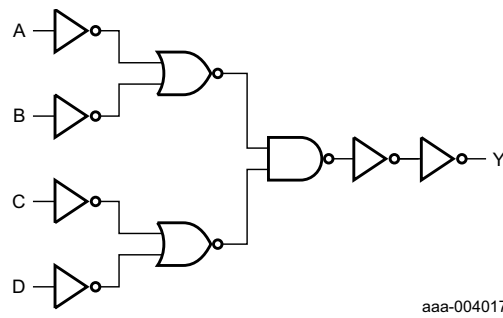


Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

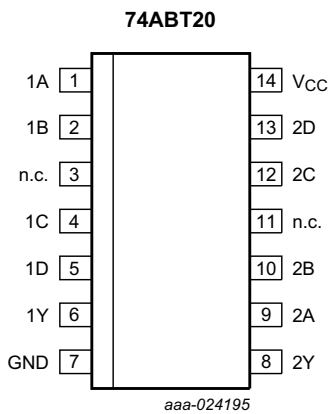


Fig 4. Pin configuration for SO14

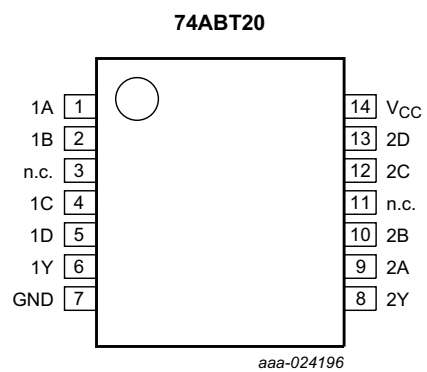


Fig 5. Pin configuration for SSOP14 and TSSOP14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 1B, 1C, 1D	1, 2, 4, 5	data input
n.c.	3, 11	not connected
1Y	6	data output
GND	7	ground (0 V)
2Y	8	data output
2A, 2B, 2C, 2D	9, 10, 12, 13	data input
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input				Output
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		^[1] -1.2	+7.0	V
V _O	output voltage	output HIGH or LOW	^[1] -0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	40	mA
T _j	junction temperature		^[2] -	150	°C
T _{stg}	storage temperature		-65	+150	°C

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-15	-	-	mA
I_{OL}	LOW-level output current		-	-	20	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}$; $I_{IK} = -18 \text{ mA}$	-1.2	-0.9	-	-1.2	-	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 4.5 \text{ V}$; $I_{OH} = -15 \text{ mA}$; $V_I = V_{IL}$ or V_{IH}	2.5	2.9	-	2.5	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}$; $I_{OL} = 20 \text{ mA}$; $V_I = V_{IL}$ or V_{IH}	-	0.35	0.5	-	0.5	V
I_I	input leakage current	$V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or 5.5 V	-	± 0.01	± 1.0	-	± 1.0	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}$; V_I or $V_O \leq 4.5 \text{ V}$	-	± 5.0	± 100	-	± 100	μA
I_{CEX}	output high leakage current	HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC}	-	5.0	50	-	50	μA
I_O	output current	$V_{CC} = 5.5 \text{ V}$; $V_O = 2.5 \text{ V}$ [1]	-50	-75	-180	-50	-180	mA
I_{CC}	supply current	$V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC}	-	2	50	-	50	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V}$; one input at 3.4 V ; other inputs at V_{CC} or GND [2]	-	0.25	500	-	500	μA
C_I	input capacitance	$V_I = 0 \text{ V}$ or V_{CC}	-	3	-	-	-	pF

[1] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[2] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

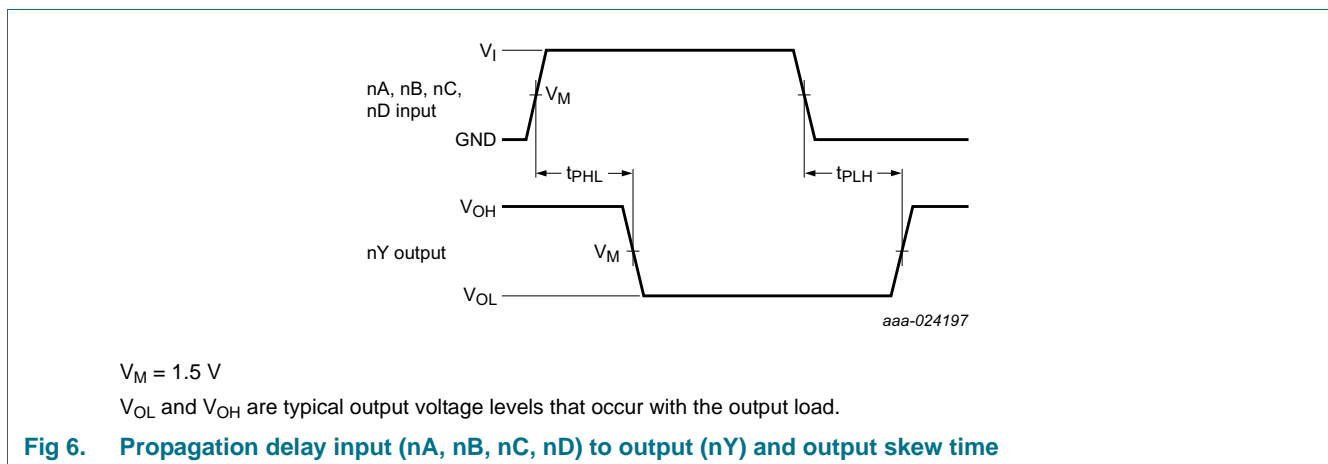
Table 7. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0\text{ V}$			-40 °C to +85 °C; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	nA, nB, nC, nD to nY; see Figure 6	1.0	2.7	3.9	1.0	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	nA, nB, nC, nD to nY; see Figure 6	1.0	2.2	3.4	1.0	3.8	ns
$t_{sk(o)}$	output skew time	[1]	-	0.3	0.5	-	0.5	ns

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

11. Waveforms



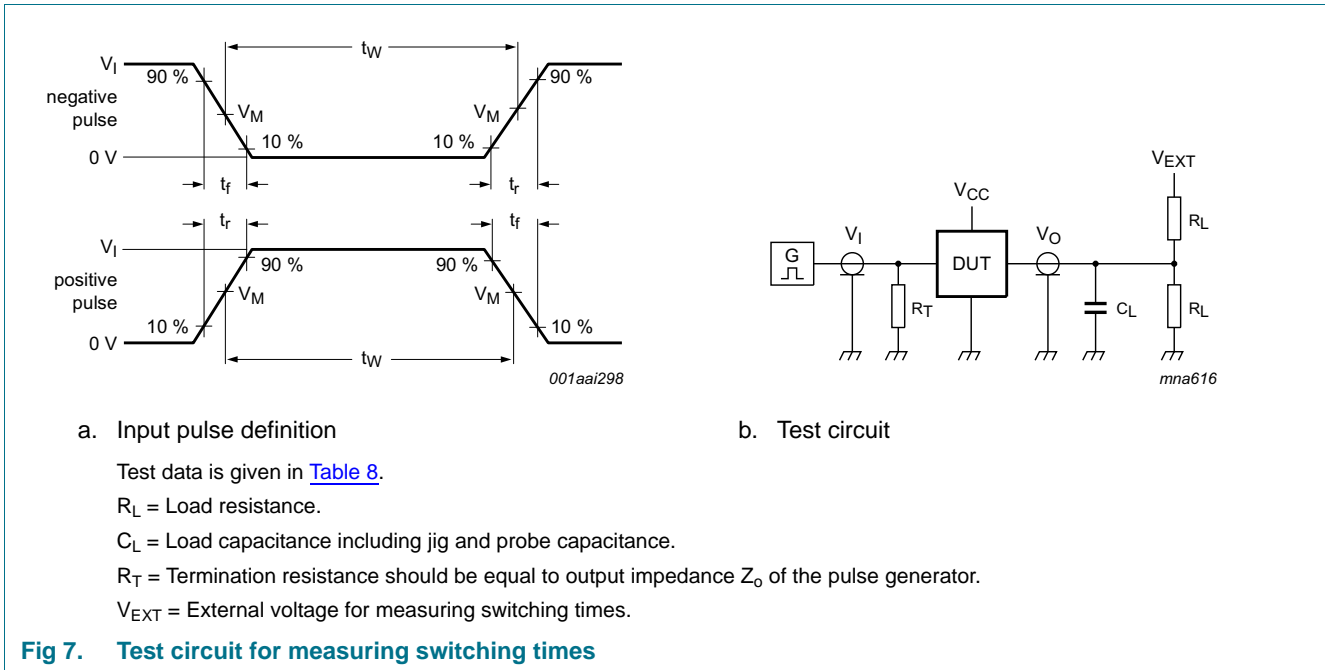


Fig 7. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

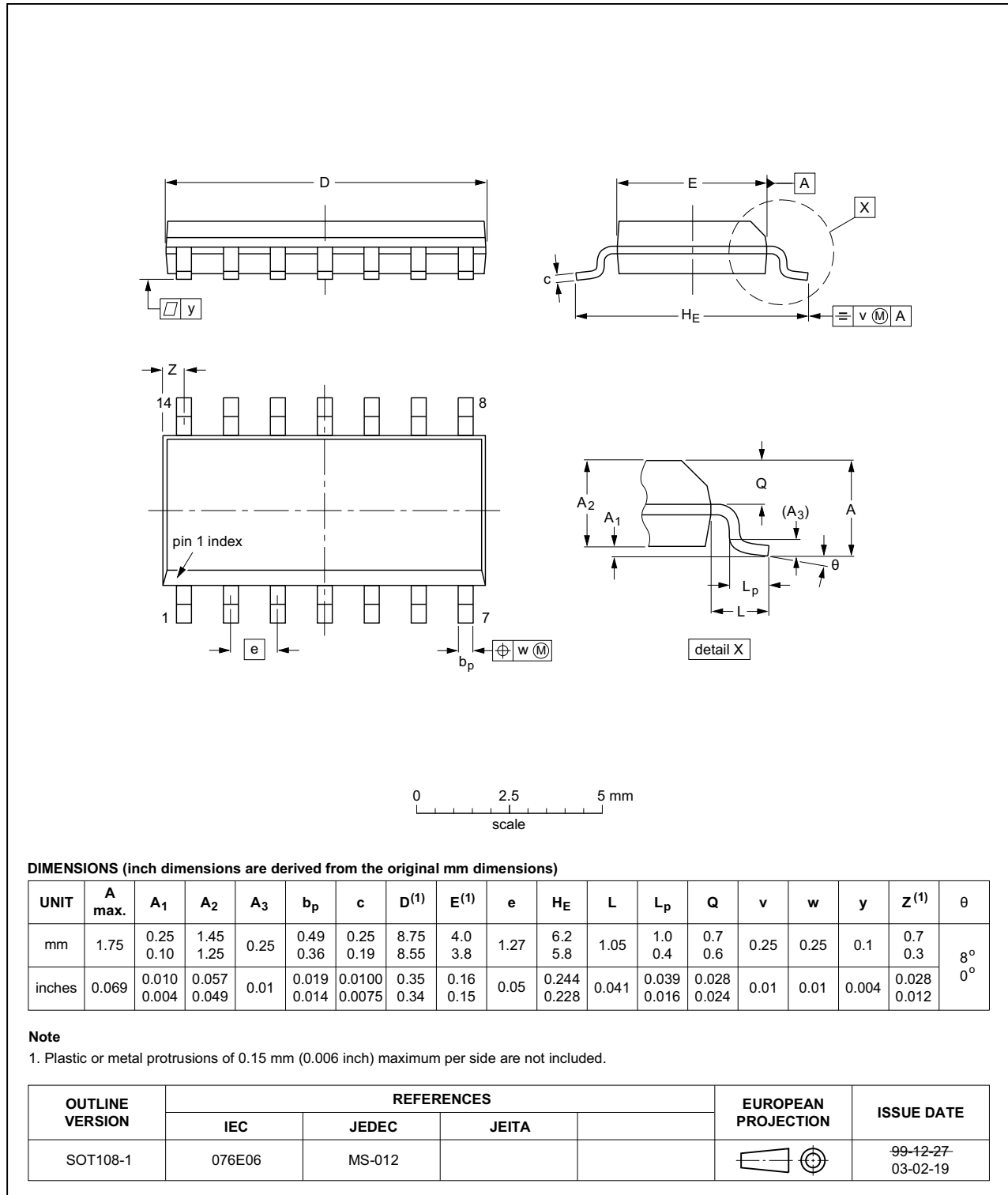


Fig 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

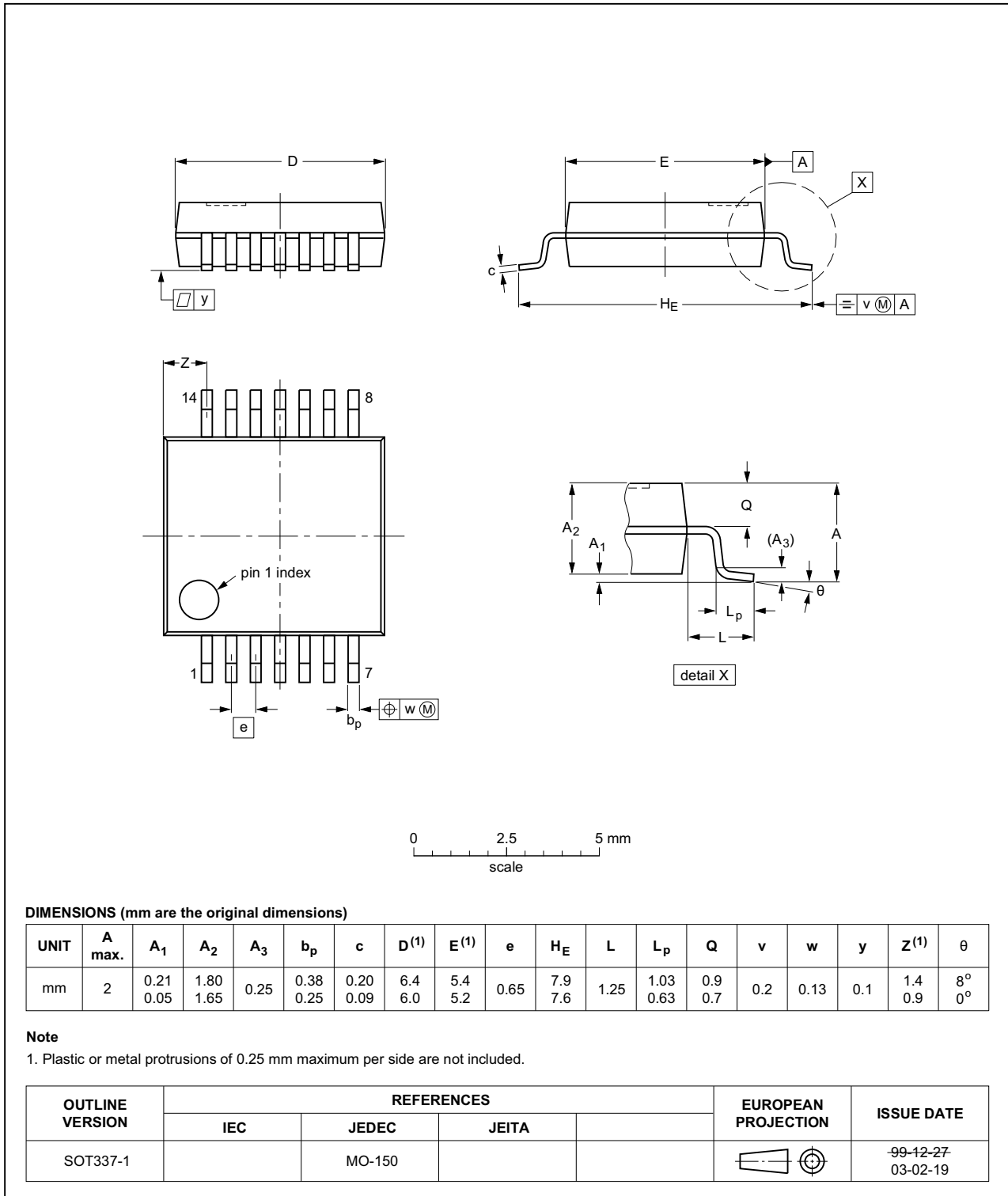


Fig 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

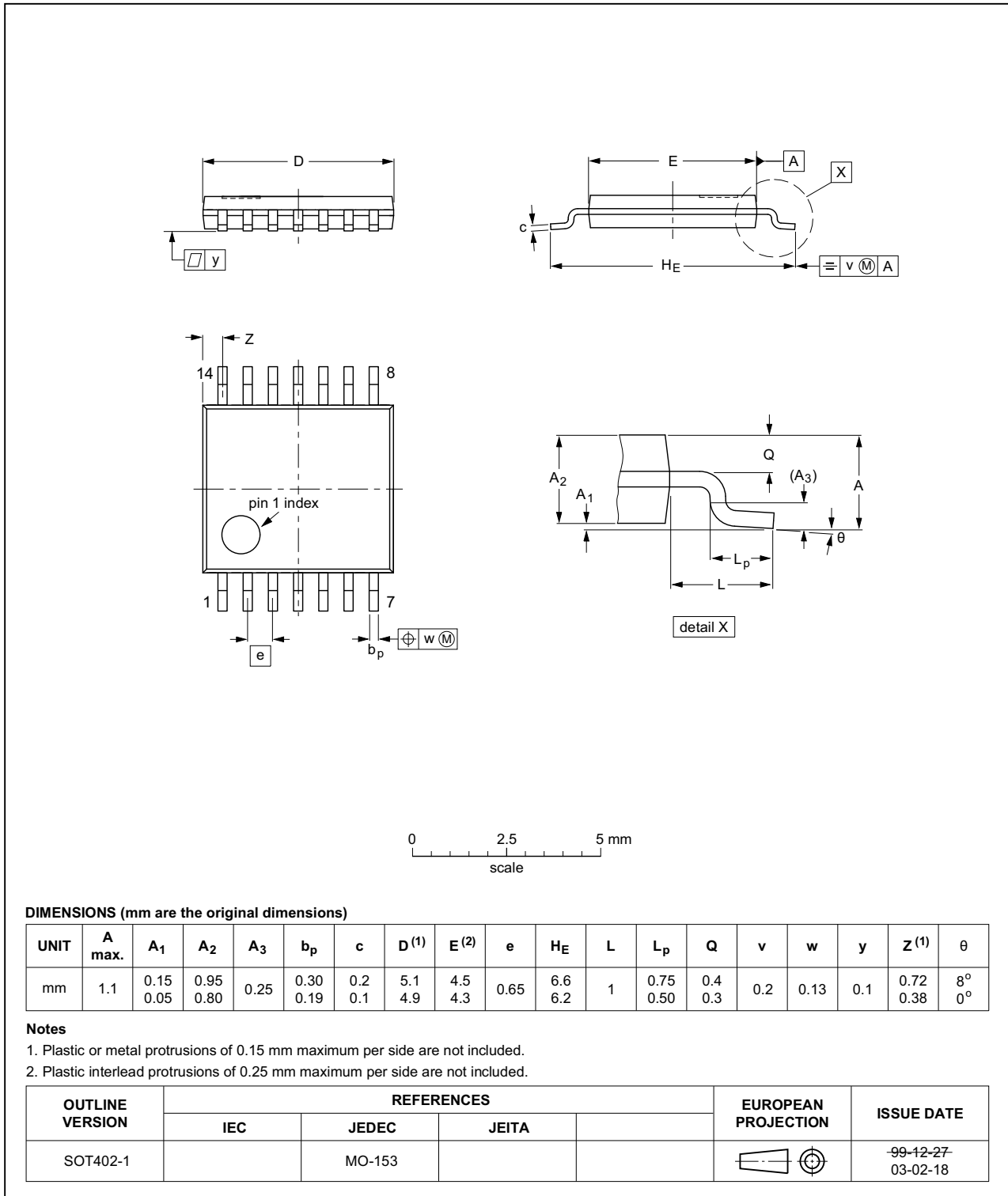


Fig 10. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT20 v.3	20160812	Product data sheet	-	74ABT20 v.2
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate.			
74ABT20 v.2	19950918	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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