

74AHC3G14; 74AHCT3G14

Triple inverting Schmitt trigger

Rev. 9 — 4 December 2018

Product data sheet

1. General description

74AHC3G14 and 74AHCT3G14 are high-speed Si-gate CMOS devices. They provide three inverting buffers with Schmitt trigger action. These devices are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101D exceeds 1000 V
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Wave and pulse shaper for highly noisy environment
- Astable multivibrator
- Monostable multivibrator

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC3G14DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHCT3G14DP				
74AHC3G14DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AHCT3G14DC				
74AHC3G14GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
74AHCT3G14GT				

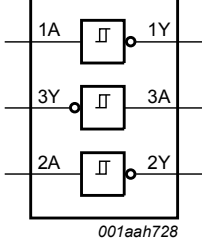
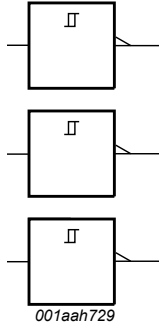
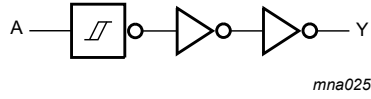
5. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AHC3G14DP	A14
74AHCT3G14DP	C14
74AHC3G14DC	A14
74AHCT3G14DC	C14
74AHC3G14GT	A14
74AHCT3G14GT	C14

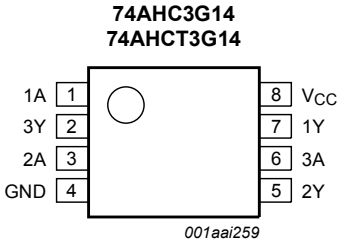
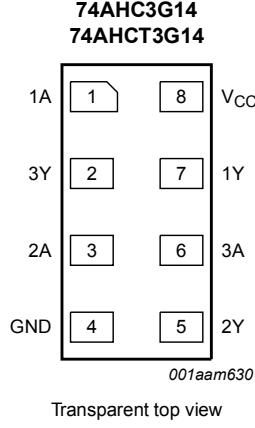
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

 <p>Fig. 1. Logic symbol</p>	 <p>Fig. 2. IEC logic symbol</p>	 <p>Fig. 3. Logic diagram (one Schmitt trigger)</p>
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7. Pinning information

7.1. Pinning

 <p>Fig. 4. Pin configuration SOT505-2 and SOT765-1</p>	 <p>Fig. 5. Pin configuration SOT833-1</p>
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7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V _{CC}	8	supply voltage

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input nA	Output nY
L	H
H	L

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V	-20	-	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly at 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly at 8 mW/K.

For XSON8 package: above 118 °C the value of P_{tot} derates linearly at 7.8 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC3G14			74AHCT3G14			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

11. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC3G14										
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}								
		I _O = -50 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}								
		I _O = 50 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF
74AHCT3G14										
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = 3.4 V; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF

11.1. Transfer characteristics

Table 8. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). See Fig. 8 and Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC3G14										
V _{T+}	positive-going threshold voltage	V _{CC} = 3.0 V	-	-	2.2	-	2.2	-	2.2	V
		V _{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
		V _{CC} = 5.5 V	-	-	3.85	-	3.85	-	3.85	V
V _{T-}	negative-going threshold voltage	V _{CC} = 3.0 V	0.9	-	-	0.9	-	0.9	-	V
		V _{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
		V _{CC} = 5.5 V	1.65	-	-	1.65	-	1.65	-	V
V _H	hysteresis voltage	V _{CC} = 3.0 V	0.3	-	1.2	0.3	1.2	0.25	1.2	V
		V _{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.35	1.4	V
		V _{CC} = 5.5 V	0.5	-	1.6	0.5	1.6	0.45	1.6	V
74AHCT3G14										
V _{T+}	positive-going threshold voltage	V _{CC} = 4.5 V	-	-	2.0	-	2.0	-	2.0	V
		V _{CC} = 5.5 V	-	-	2.0	-	2.0	-	2.0	V
V _{T-}	negative-going threshold voltage	V _{CC} = 4.5 V	0.5	-	-	0.5	-	0.5	-	V
		V _{CC} = 5.5 V	0.6	-	-	0.6	-	0.6	-	V
V _H	hysteresis voltage	V _{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.35	1.4	V
		V _{CC} = 5.5 V	0.4	-	1.6	0.4	1.6	0.35	1.6	V

12. Dynamic characteristics

Table 9. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f \leq 3.0\text{ ns}$; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC3G14										
t_{pd}	propagation delay	nA to nY; see Fig. 6 [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]								
		$C_L = 15\text{ pF}$	-	4.2	12.8	1.0	15.0	1.0	16.5	ns
		$C_L = 50\text{ pF}$	-	6.0	16.3	1.0	18.5	1.0	20.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]								
		$C_L = 15\text{ pF}$	-	3.2	8.6	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	$C_L = 50\text{ pF}$	-	4.6	10.6	1.0	12.0	1.0	13.5	ns
		per buffer; $C_L = 50\text{ pF}$; $f_i = 1\text{ MHz}$; $V_i = GND\text{ to }V_{CC}$ [4]	-	10	-	-	-	-	-	pF
74AHCT3G14										
t_{pd}	propagation delay	nA to nY; see Fig. 6 [1]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]								
		$C_L = 15\text{ pF}$	-	4.1	7.0	1.0	8.0	1.0	9.0	ns
		$C_L = 50\text{ pF}$	-	5.9	8.5	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}$; $f_i = 1\text{ MHz}$; $V_i = GND\text{ to }V_{CC}$ [4]	-	12	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] Typical values are measured at $V_{CC} = 3.3\text{ V}$.

[3] Typical values are measured at $V_{CC} = 5.0\text{ V}$.

[4] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12.1. Waveform and test circuit

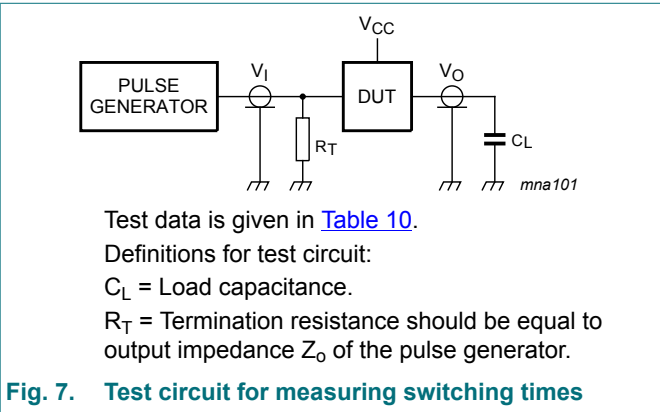
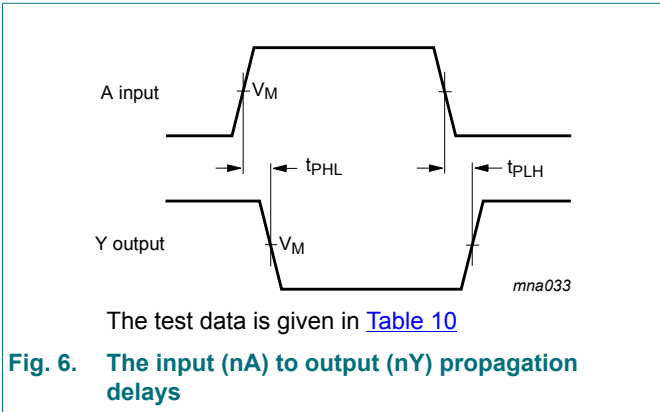
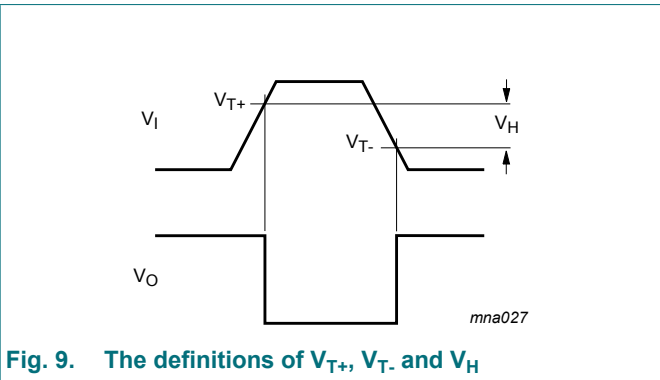
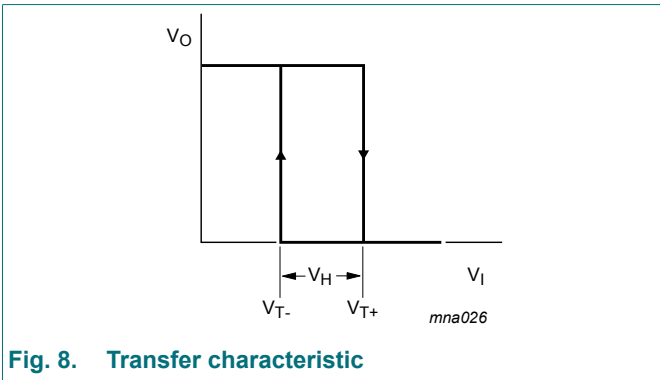


Table 10. Test data

Type number	Input		Output
	V_I	V_M	V_M
74AHC3G14	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT3G14	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$

12.2. Transfer characteristic waveforms



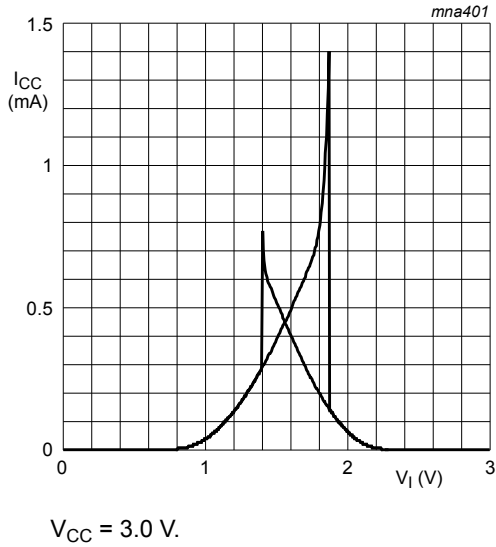


Fig. 10. Typical 74AHC3G14 transfer characteristics

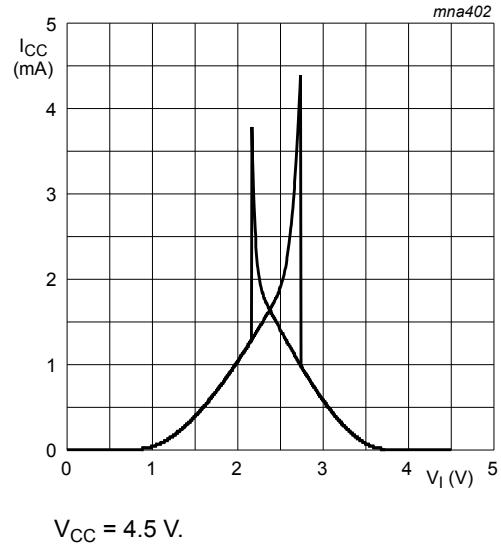


Fig. 11. Typical 74AHC3G14 transfer characteristics

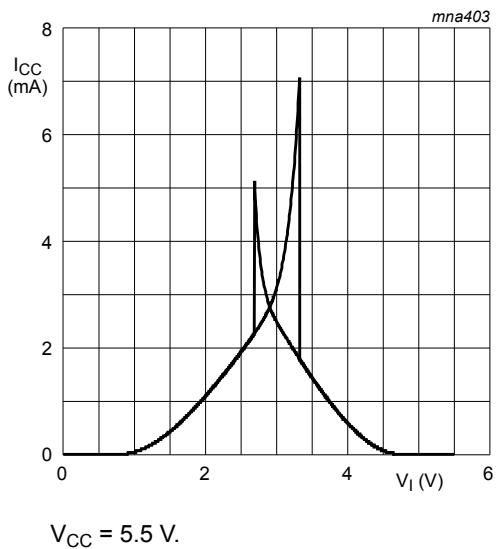


Fig. 12. Typical 74AHC3G14 transfer characteristics

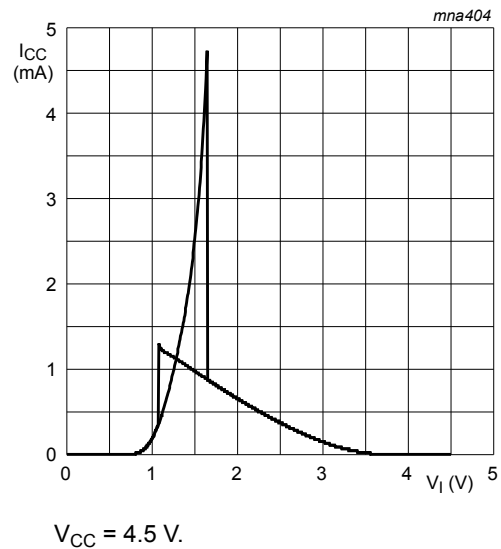


Fig. 13. Typical 74AHCT3G14 transfer characteristics

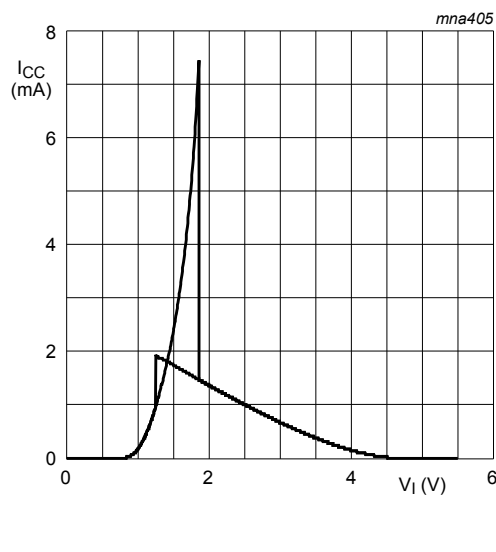


Fig. 14. Typical 74AHCT3G14 transfer characteristics

13. Application information

The slow input rise and fall times cause additional power dissipation, which can be calculated using the following formula:

$$P_{\text{add}} = f_i \times (t_r \times \Delta I_{\text{CC(AV)}} + t_f \times \Delta I_{\text{CC(AV)}}) \times V_{\text{CC}}$$

where:

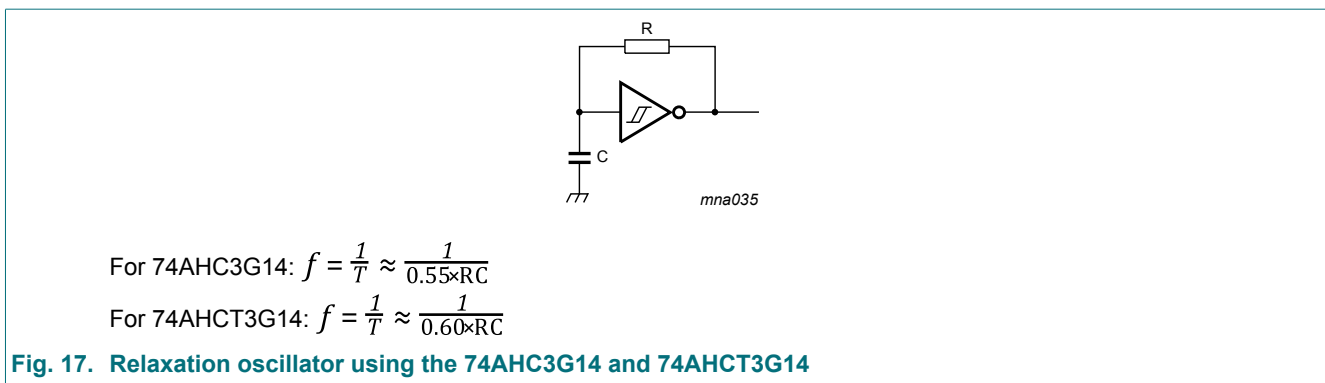
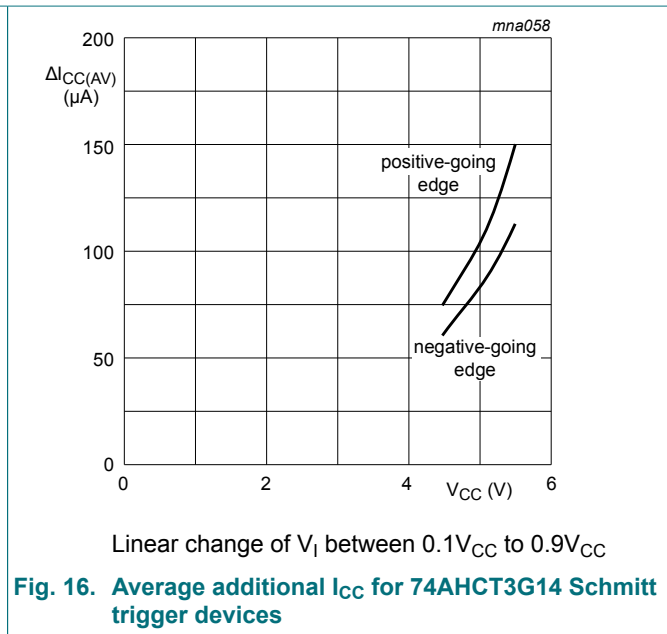
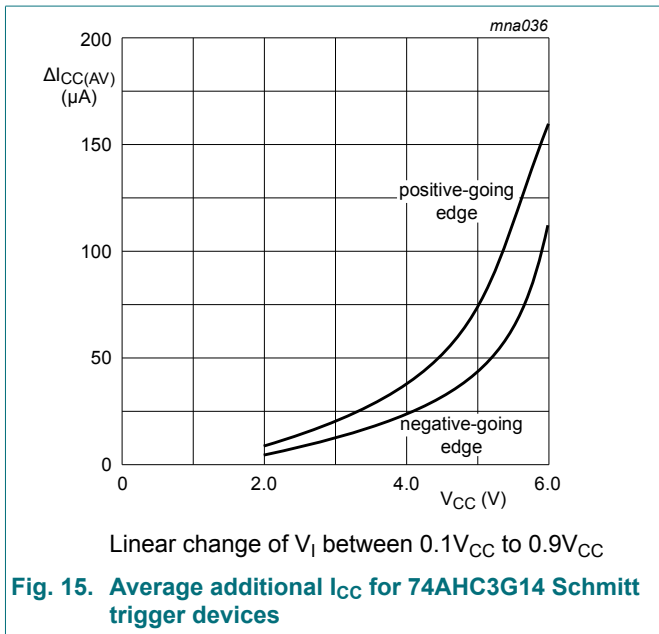
- P_{add} = additional power dissipation (μW);
- f_i = input frequency (MHz);
- t_r = input rise time (ns); 10 % to 90 %;
- t_f = input fall time (ns); 90 % to 10 %;
- $\Delta I_{\text{CC(AV)}}$ = average additional supply current (μA).

$\Delta I_{\text{CC(AV)}}$ differs with positive or negative input transitions, as shown in [Fig. 15](#) and [Fig. 16](#).

For 74AHC3G14 and 74AHCT3G14 used in relaxation oscillator circuit, see [Fig. 17](#).

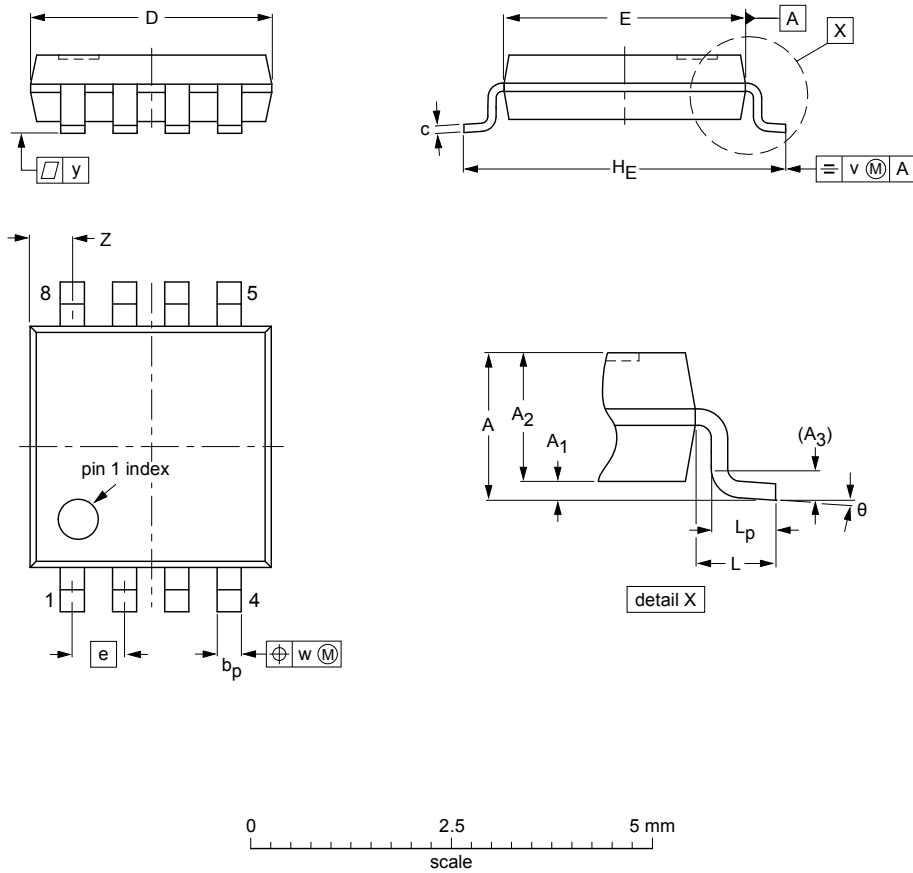
Note to the application information:

1. All values given are typical unless otherwise specified.



14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

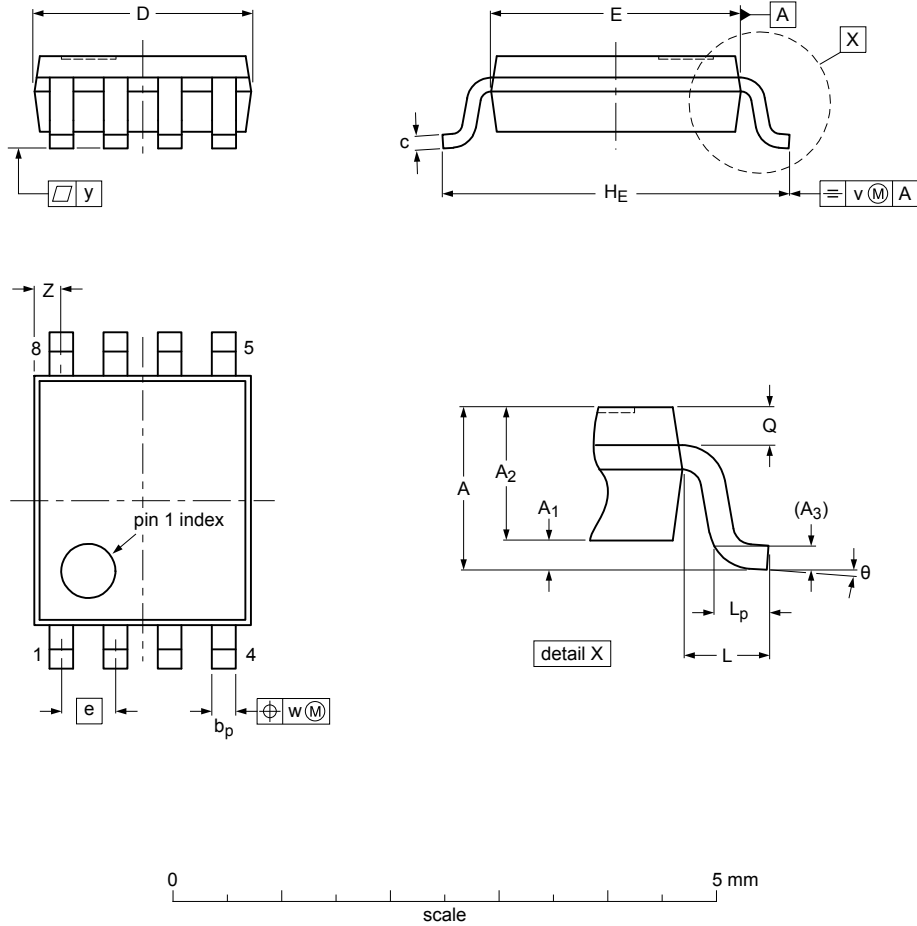
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Fig. 18. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A ^A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	max	0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
	nom	1		0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60	0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

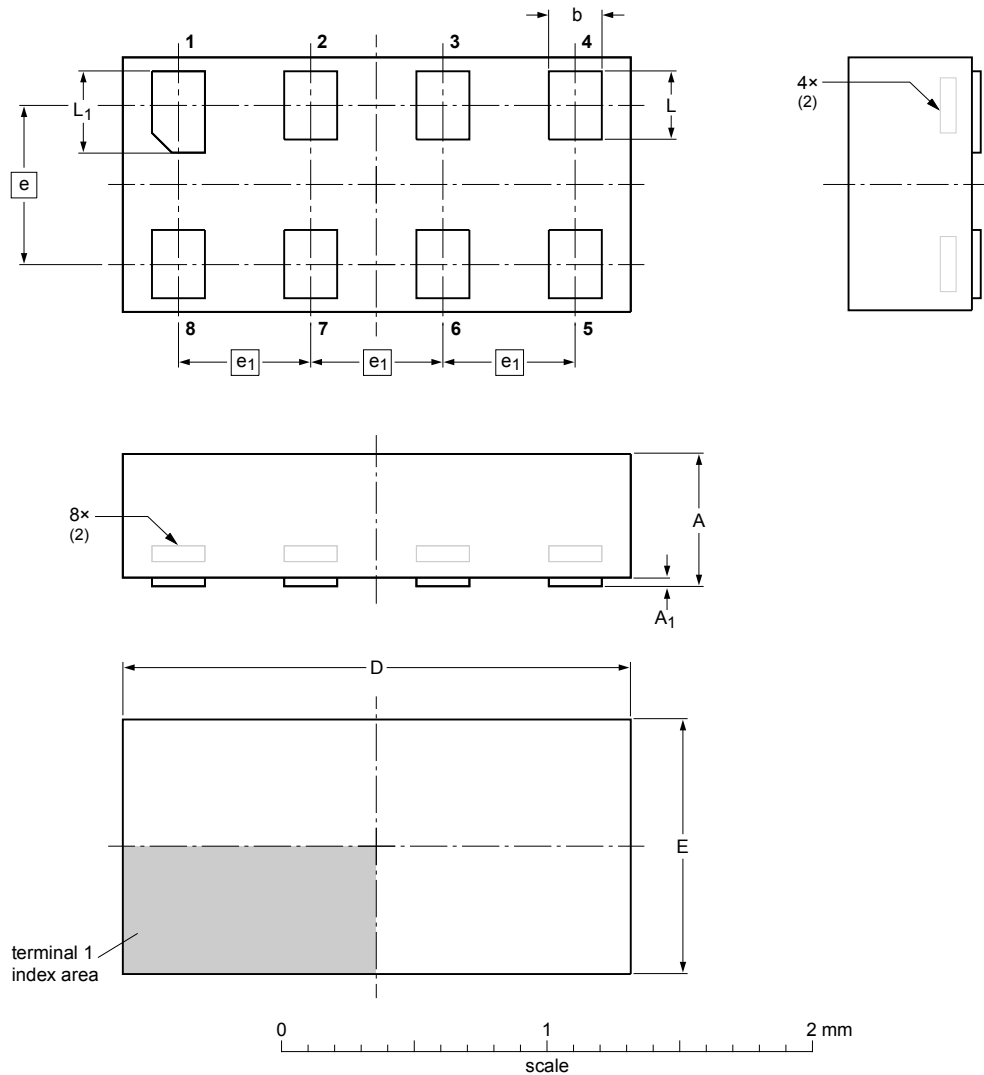
sot765-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT765-1		MO-187			-07-06-02- 16-05-31

Fig. 19. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

- Including plating thickness.
- Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT833-1	---	MO-252	---		-07-11-14- 07-12-07

Fig. 20. Package outline SOT833-1 (XSON8)

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT3G14 v.9	20181204	Product data sheet	-	74AHC_AHCT3G14 v.8
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74AHC3G14GD and 74AHCT3G14GD (SOT996-2/XSON8) removed. 			
74AHC_AHCT3G14 v.8	20130513	Product data sheet	-	74AHC_AHCT3G14 v.7
Modifications:	<ul style="list-style-type: none"> For type number 74AHC3G14GD and 74AHCT3G14GD XSON8U has changed to XSON8. 			
74AHC_AHCT3G14 v.7	20111108	Product data sheet	-	74AHC_AHCT3G14 v.6
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74AHC_AHCT3G14 v.6	20101118	Product data sheet	-	74AHC_AHCT3G14 v.5
74AHC_AHCT3G14 v.5	20100923	Product data sheet	-	74AHC_AHCT3G14 v.4
74AHC_AHCT3G14 v.4	20090505	Product data sheet	-	74AHC_AHCT3G14 v.3
74AHC_AHCT3G14 v.3	20080617	Product data sheet	-	74AHC_AHCT3G14 v.2
74AHC_AHCT3G14 v.2	20041018	Product specification	-	74AHC_AHCT3G14 v.1
74AHC_AHCT3G14 v.1	20031127	Product specification	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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