

74AHC2G00; 74AHCT2G00

Dual 2-input NAND gate

Rev. 5 — 7 March 2019

Product data sheet

1. General description

The 74AHC2G00; 74AHCT2G00 are high-speed Si-gate CMOS devices. They provide two 2-input NAND gates.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101C exceeds 1000 V
- Low power dissipation
- Balanced propagation delays
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC2G00DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHC2G00DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AHCT2G00DC				

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74AHC2G00DP	A00
74AHC2G00DC	A00
74AHCT2G00DC	C00

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

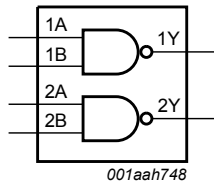


Fig. 1. Logic symbol

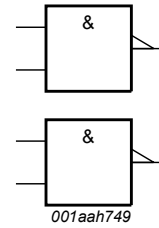


Fig. 2. IEC logic symbol

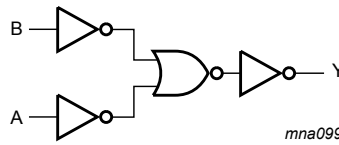


Fig. 3. Logic diagram (one gate)

6. Pinning information

6.1. Pinning

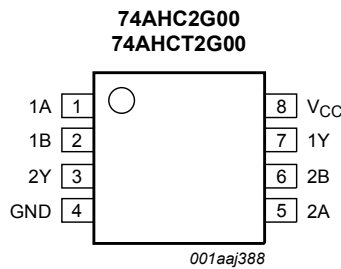


Fig. 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	-0.5 V < V_O < $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC2G00			74AHCT2G00			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC2G00										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
		I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	-	10	-
C _I	input capacitance		-	1.5	10	-	10	-	10	pF
74AHCT2G00										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
V _{OL}	LOW-level output voltage	I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
		V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
I _I	input leakage current	I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; $V_I = 3.4\text{ V}$; other inputs at V_{CC} or GND; $I_O = 0\text{ A}$; $V_{CC} = 5.5\text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC2G00										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 5 [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$; [2]								
		$C_L = 15\text{ pF}$	-	4.5	7.9	1.0	9.5	1.0	10.5	ns
		$C_L = 50\text{ pF}$	-	6.5	11.4	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$; [3]								
		$C_L = 15\text{ pF}$	-	3.5	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50\text{ pF}$	-	4.9	7.5	1.0	8.5	1.0	9.5	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}$; $f_i = 1\text{ MHz}$; $V_I = GND\text{ to }V_{CC}$ [4]	-	17	-	-	-	-	-	pF
74AHCT2G00										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 5 [1]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$; [3]								
		$C_L = 15\text{ pF}$	1.0	3.6	6.2	1.0	7.1	1.0	8.0	ns
		$C_L = 50\text{ pF}$	1.0	5.0	7.9	1.0	9.0	1.0	10.0	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}$; $f_i = 1\text{ MHz}$; $V_I = GND\text{ to }V_{CC}$ [4]	-	18	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] Typical values are measured at $V_{CC} = 3.3\text{ V}$.

[3] Typical values are measured at $V_{CC} = 5.0\text{ V}$.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

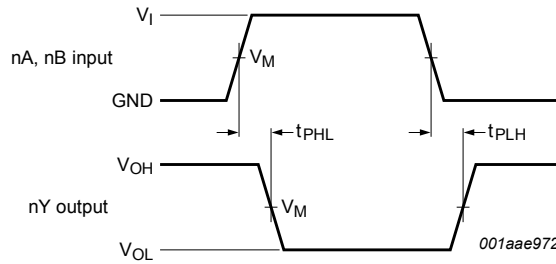
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit



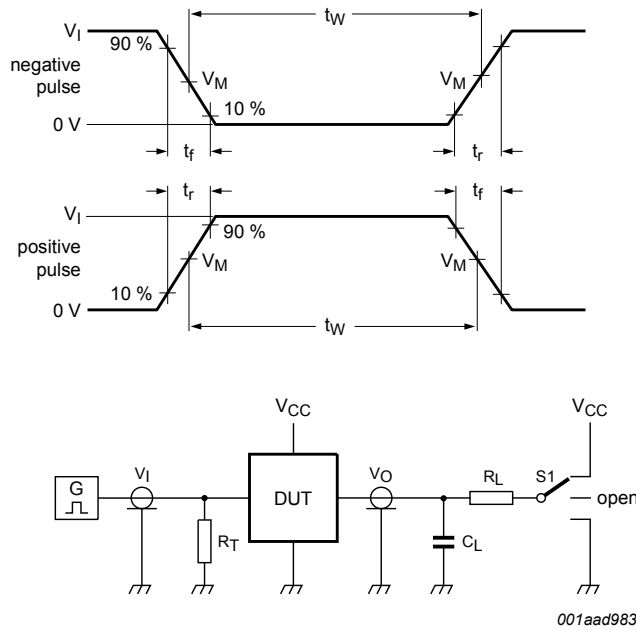
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The input (nA and nB) to output (nY) propagation delays

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74AHC2G00	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT2G00	1.5 V	$0.5V_{CC}$



Test data is given in [Table 10](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance; S1 = Test selection switch.

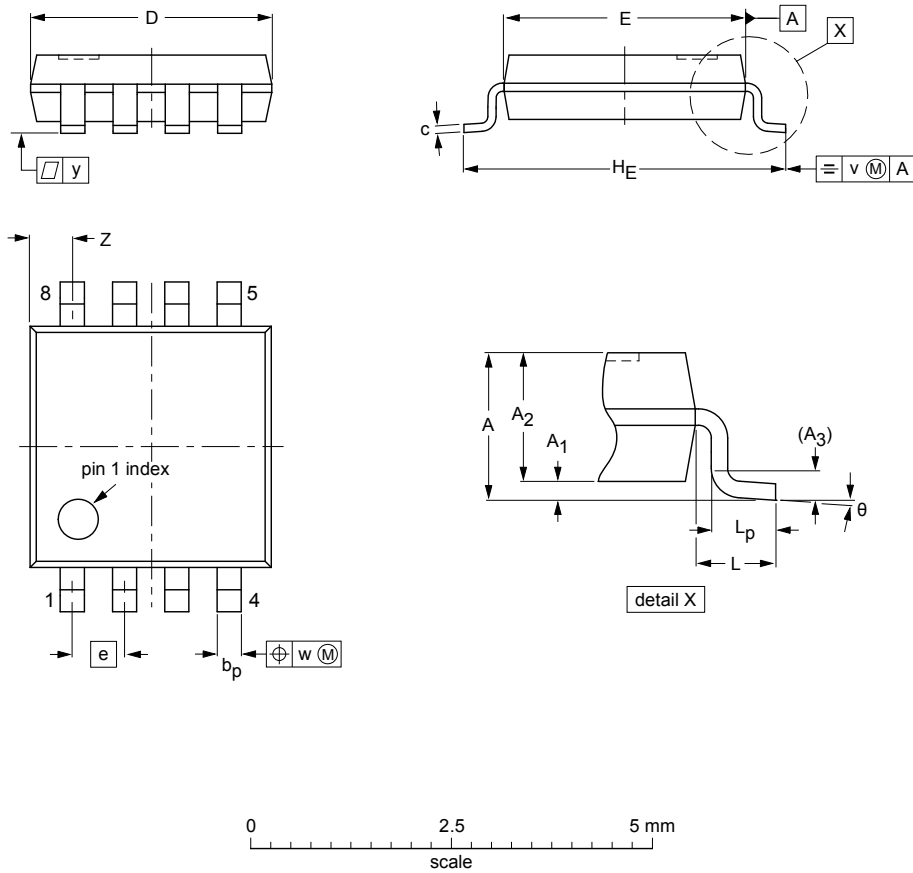
Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_i	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74AHC2G00	V_{CC}	≤ 3 ns	15 pF, 50 pF	1 k Ω	open
74AHCT2G00	3 V	≤ 3 ns	15 pF, 50 pF	1 k Ω	open

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

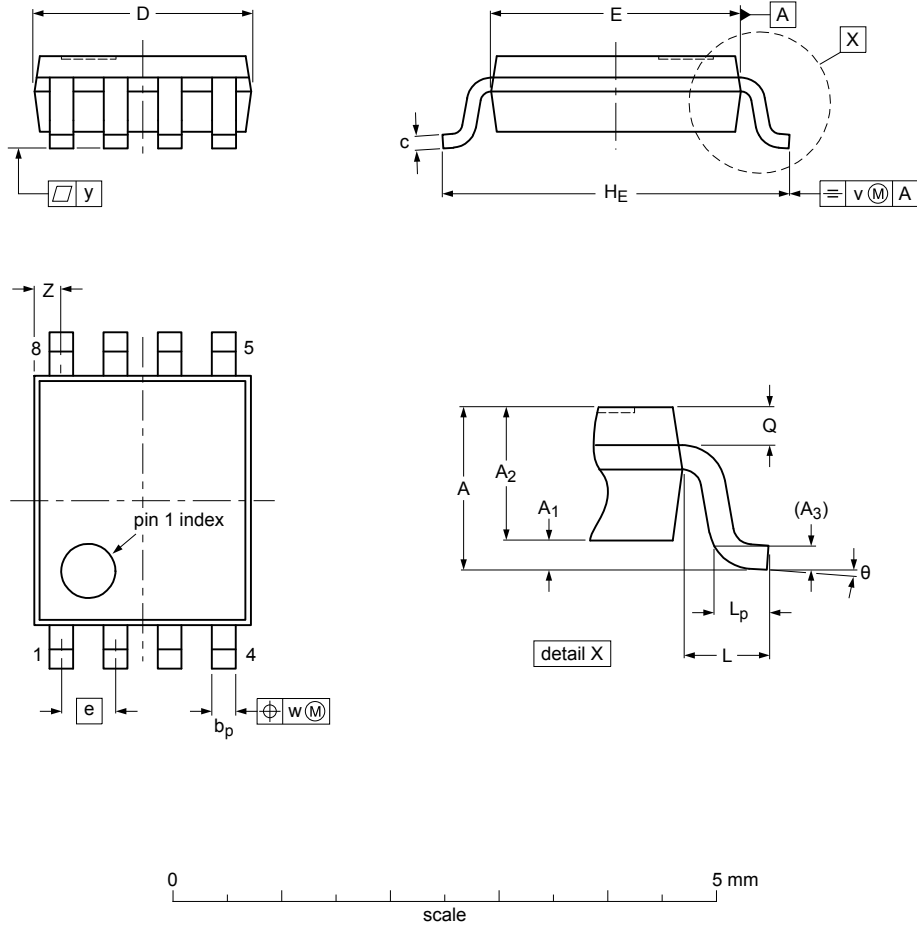
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Fig. 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A ^A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	max	0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
	nom	1		0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60	0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				07-06-02-16-05-31

Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT2G00 v.5	20190307	Product data sheet	-	74AHC_AHCT2G00 v.4
Modifications:	<ul style="list-style-type: none"> Type number 74AHCT2G00DP (SOT505-2/TSSOP8) removed. 			
74AHC_AHCT2G00 v.4	20181115	Product data sheet	-	74AHC_AHCT2G00 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74AHC2G00GD and 74AHCT2G00GD (SOT996-2/XSON8) removed. 			
74AHC_AHCT2G00 v.3	20130327	Product data sheet	-	74AHC_AHCT2G00 v.2
Modifications:	<ul style="list-style-type: none"> For type numbers 74AHC2G00GD and 74AHCT2G00GD XSON8U has changed to XSON8. 			
74AHC_AHCT2G00 v.2	20090112	Product data sheet	-	74AHC_AHCT2G00 v.1
74AHC_AHCT2G00 v.1	20040101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Marking	1
5. Functional diagram	2
6. Pinning information	2
6.1. Pinning.....	2
6.2. Pin description.....	2
7. Functional description	3
8. Limiting values	3
9. Recommended operating conditions	3
10. Static characteristics	4
11. Dynamic characteristics	5
11.1. Waveforms and test circuit.....	6
12. Package outline	7
13. Abbreviations	9
14. Revision history	9
15. Legal information	10

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[NLX1G11AMUTCG](#) [NLX1G97MUTCG](#) [74LS38](#) [74LVC32ADTR2G](#) [MC74HCT20ADTR2G](#) [NLV17SZ00DFT2G](#) [NLV17SZ02DFT2G](#)
[NLV74HC02ADR2G](#) [74HC32S14-13](#) [74LS133](#) [M38510/30402BDA](#) [74LVC1G86Z-7](#) [74LVC2G08RA3-7](#) [NLV74HC08ADTR2G](#)
[NLV74HC14ADR2G](#) [NLV74HC20ADR2G](#) [NLX2G86MUTCG](#) [5962-8973601DA](#) [74LVC2G02HD4-7](#) [NLU1G00AMUTCG](#)
[74LVC2G32RA3-7](#) [74LVC2G00HD4-7](#) [NL17SG02P5T5G](#) [74LVC2G00HK3-7](#) [74LVC2G86HK3-7](#) [NLX1G99DMUTWG](#)
[NLVVHC1G00DFT2G](#) [NLVHC1G08DFT2G](#) [NLV7SZ57DFT2G](#) [NLV74VHC04DTR2G](#) [NLV27WZ86USG](#) [NLV27WZ00USG](#)
[NLU1G86CMUTCG](#) [NLU1G08CMUTCG](#) [NL17SZ32P5T5G](#) [NL17SZ00P5T5G](#) [NL17SH02P5T5G](#) [74AUP2G00RA3-7](#)
[NLV74HC02ADTR2G](#) [NLX1G332CMUTCG](#) [NL17SG86P5T5G](#) [NL17SZ05P5T5G](#) [NLV74VHC00DTR2G](#)