74AHC595-Q100; 74AHCT595-Q100

8-bit serial-in/serial-out or parallel-out shift register with output latches

Rev. 2 — 26 May 2020

Product data sheet

1. General description

The 74AHC595-Q100; 74AHCT595-Q100 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{\text{MR}}$ input. A LOW on $\overline{\text{MR}}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{\text{OE}}$) is LOW. A HIGH on $\overline{\text{OE}}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the registers. The 74AHCT595-Q100 features TTL compatible inputs. Both 74AHC595-Q100 and 74AHCT595-Q100 inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 5.5 V
- · Balanced propagation delays
- All inputs have Schmitt trigger action
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Input levels:
 - The 74AHC595-Q100 operates with CMOS input levels
 - The 74AHCT595-Q100 operates with TTL input levels
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0 Ω)
- · Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Serial-to-parallel data conversion
- · Remote control holding register

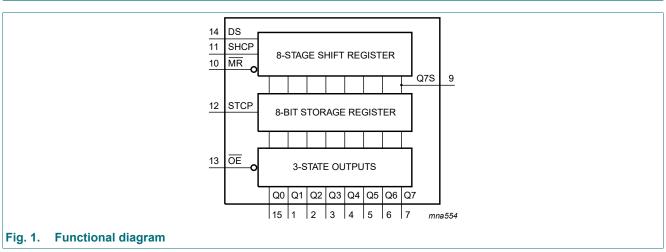


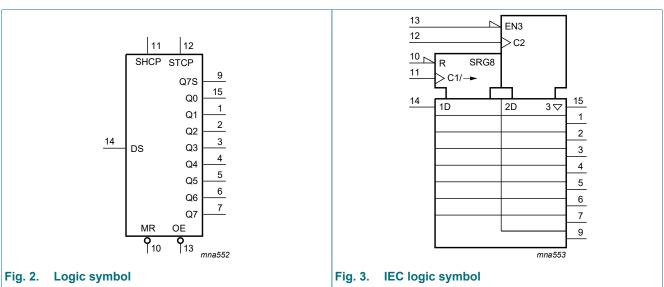
4. Ordering information

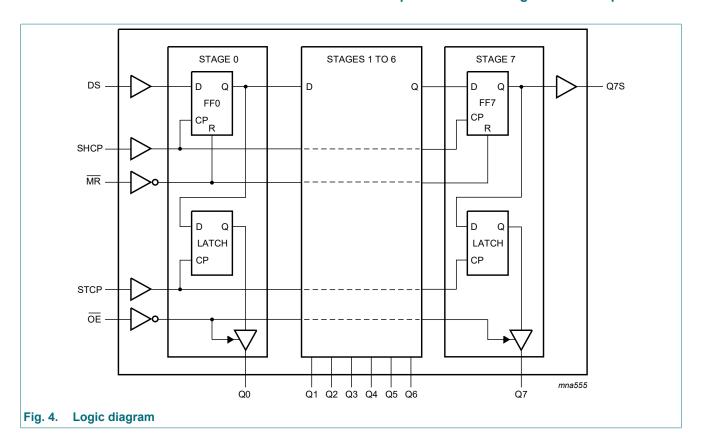
Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74AHC595D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1					
74AHCT595D-Q100			body width 3.9 mm						
74AHC595PW-Q100 -40 °C to +125 °C		TSSOP16	plastic thin shrink small outline package;	SOT403-1					
74AHCT595PW-Q100			16 leads; body width 4.4 mm						
74AHC595BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible	SOT763-1					
74AHCT595BQ-Q100			thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm						

5. Functional diagram

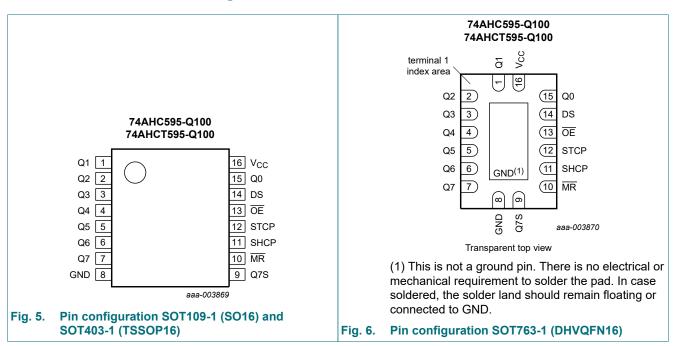






6. Pinning information

6.1. Pinning



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6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
ŌE	13	output enable input (active LOW)
DS	14	serial data input
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage state;

L = LOW voltage state;

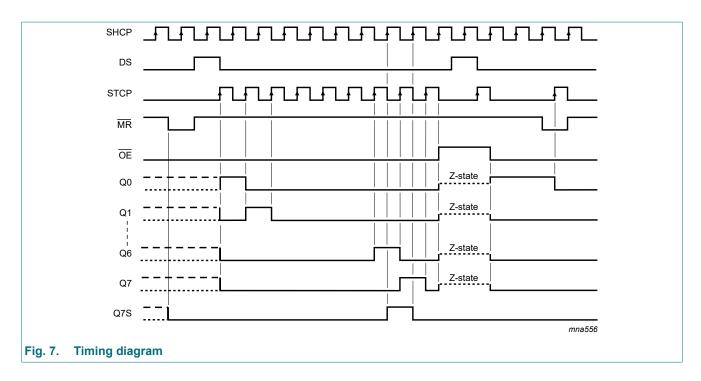
↑ = LOW-to-HIGH transition;

X = don't care;

NC = no change;

Z = high-impedance OFF-state.

Contro	I			Input	Output	:	Function
SHCP	STCP	OE	MR	DS	Q7S	Qn	
X	Χ	L	L	Χ	L	NC	a LOW-level on $\overline{\text{MR}}$ only affects the shift registers
X	1	L	L	Х	L	L	empty shift register loaded into storage register
Χ	Х	Н	L	Х	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
1	Х	L	Н	Н	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	1	L	Н	Х	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	Н	Х	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages



8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V}$ [1]	-20	-	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-20	+20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C. For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C. For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	74A	HC595-0	2100	74AH	Unit		
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.0 V to 3.6 V	-	-	100	-	-	-	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC5	95-Q100									
V_{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
l _l	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.25	-	±2.5	-	±10	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
C _I	input capacitance		-	3	10	-	10	-	10	pF

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHCT	595-Q100									
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	I _O = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.25	-	±2.5	-	±10	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μA
Δl _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance		-	3	10	-	10	-	10	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 13.

Symbol	Parameter	Conditions	25 °C				°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHC5	95-Q100								•	
t _{pd}	propagation	SHCP to Q7S; see Fig. 8 [2]								
	delay	V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	5.7	13.0	1.0	15.0	1.0	16.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	7.7	16.5	1.0	18.5	1.0	20.1	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.0	8.2	1.0	9.4	1.0	10.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.4	10.0	1.0	11.4	1.0	12.5	ns
		STCP to Qn; see Fig. 9 [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	5.9	11.9	1.0	13.5	1.0	15.0	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	7.7	15.4	1.0	17.0	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.2	7.4	1.0	8.5	1.0	9.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.5	9.0	1.0	10.5	1.0	11.5	ns

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t _{PHL}	HIGH	MR to Q7S; see Fig. 11								
	to LOW	V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.9	12.8	1.0	13.7	1.0	15.0	ns
	propagation delay	V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	7.4	16.3	1.0	17.2	1.0	18.7	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.4	8.0	1.0	9.1	1.0	10.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.6	10.0	1.0	11.1	1.0	12.0	ns
t _{en}	enable time	OE to Qn; see Fig. 12 [3]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.6	11.5	1.0	13.5	1.0	15.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	7.4	15.0	1.0	17.0	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.0	8.6	1.0	10.0	1.0	11.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.3	10.6	1.0	12.0	1.0	13.0	ns
t _{dis}	disable time	OE to Qn; see Fig. 12 [4]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.4	11.0	1.0	13.0	1.0	14.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	8.7	15.7	1.0	16.2	1.0	17.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	3.8	8.0	1.0	9.5	1.0	10.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f _{max}	maximum	SHCP or STCP; see Fig. 8 and Fig. 9								
	frequency	V _{CC} = 3.0 V to 3.6 V	80	125	-	60	-	40	-	MHz
		V _{CC} = 4.5 V to 5.5 V	130	170	-	110	-	90	-	MHz
t _W	pulse width	SHCP HIGH or LOW; see Fig. 8								
ι _W		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Fig. 9								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; see Fig. 11								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t _{su}	set-up time	DS to SHCP; see Fig. 10								
		V _{CC} = 3.0 V to 3.6 V	3.5	-	-	3.5	-	3.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Fig. 9								
		V _{CC} = 3.0 V to 3.6 V	8.5	-	-	8.5	-	8.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t _h	hold time	DS to SHCP; see Fig. 10								
		V _{CC} = 3.0 V to 3.6 V	1.5	-	-	1.5	-	1.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	ns
t _{rec}	recovery	MR to SHCP; see Fig. 11								
	time	V _{CC} = 3.0 V to 3.6 V	3.0	-	-	3.0	-	3.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	2.5	-	-	2.5	-	2.5	-	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ [5] [6]	-	180	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	_	°C to 5 °C	Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHCT	595-Q100							•		
t _{pd}	propagation	SHCP to Q7S; see Fig. 8 [2]								
	delay	V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.8	8.2	1.0	9.0	1.0	10.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.2	10.0	1.0	11.0	1.0	12.0	ns
		STCP to Qn; see Fig. 9 [2]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.0	7.4	1.0	8.5	1.0	9.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.3	9.0	1.0	10.5	1.0	11.5	ns
t _{PHL}	HIGH	MR to Q7S; see Fig. 11								
	to LOW	V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.6	8.2	1.0	9.5	1.0	10.5	ns
	propagation delay	V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.8	10.5	1.0	11.5	1.0	12.5	ns
t _{en}	enable time	OE to Qn; see Fig. 12 [3]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.8	9.0	1.0	11.0	1.0	12.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	6.2	11.6	1.0	13.0	1.0	14.5	ns
t _{dis}	disable time	OE to Qn; see Fig. 12 [4]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.6	6.9	1.0	8.0	1.0	9.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f _{max}	maximum frequency	SHCP and STCP; V_{CC} = 4.5 V to 5.5 V; see Fig. 8 and Fig. 9	130	170	-	110	-	90	-	MHz
t _W	pulse width	SHCP HIGH or LOW; V _{CC} = 4.5 V to 5.5 V; see Fig. 8	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; V _{CC} = 4.5 V to 5.5 V; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
		\overline{MR} LOW; V_{CC} = 4.5 V to 5.5 V; see Fig. 11	5.0	-	-	5.0	-	5.0	-	ns
t _{su}	set-up time	DS to SHCP; V_{CC} = 4.5 V to 5.5 V; see Fig. 10	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
t _h	hold time	DS to SHCP; V_{CC} = 4.5 V to 5.5 V; see Fig. 10	2.0	-	-	2.0	-	2.0	-	ns
t _{rec}	recovery time	\overline{MR} to SHCP; V_{CC} = 4.5 V to 5.5 V; see $\overline{Fig. 11}$	3.0	-	-	3.0	-	3.0	-	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ [5]		190	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage.
- t_{pd} is the same as t_{PHL} and t_{PLH} . [2] [3]
- t_{en} is the same as t_{PZL} and t_{PZH}.
- [4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
 [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

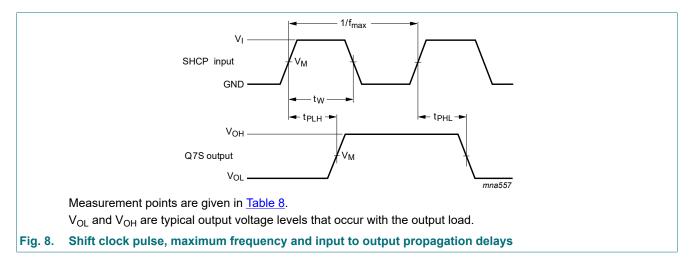
C_L = output load capacitance in pF;

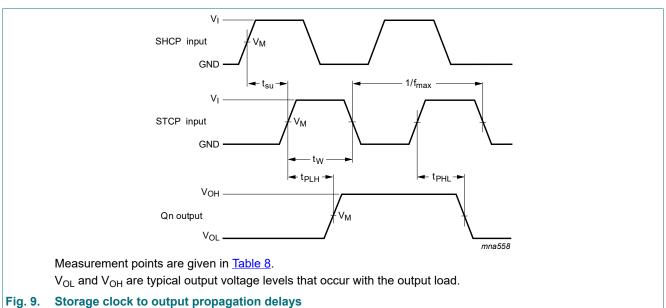
V_{CC} = supply voltage in V.

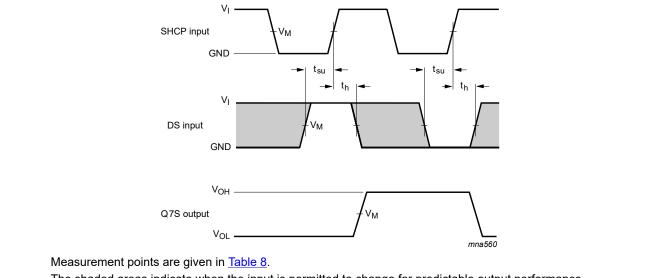
[6] All 9 outputs switching.

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11.1. Waveforms and test circuit



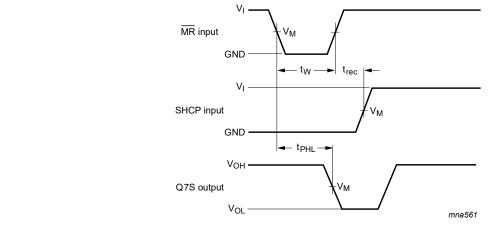




The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 10. Data set-up and hold times



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 11. Master reset to output propagation delays

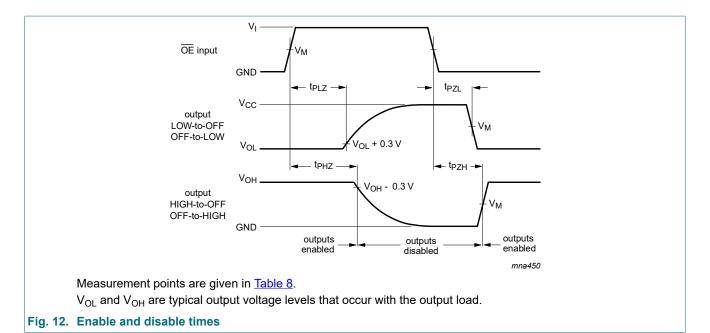
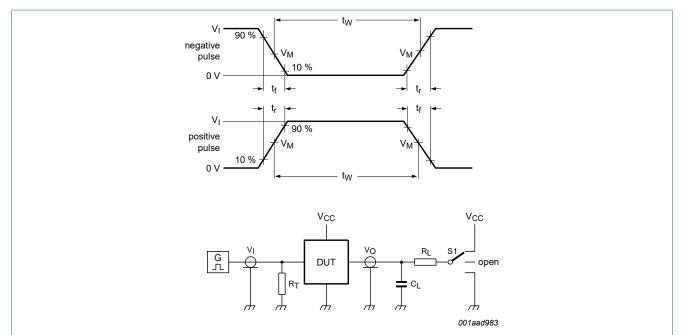


Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74AHC595-Q100	0.5V _{CC}	0.5V _{CC}
74AHCT595-Q100	1.5 V	0.5V _{CC}



Test data is given in Table 9.

Definitions for test circuit:

 C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1 = test selection switch.

Fig. 13. Test circuit for measuring switching times

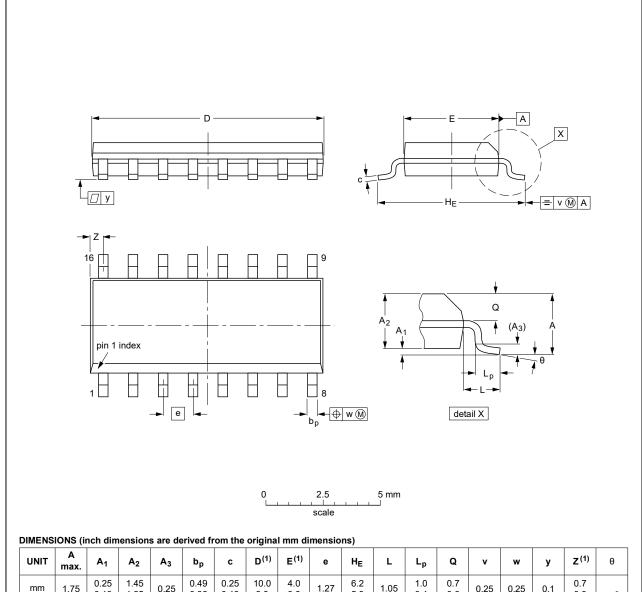
Table 9. Test data

Туре	Input		Load		S1 position			
	V _I	t _r , t _f	C _L R _L t _P		t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
74AHC595-Q100	V _{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	
74AHCT595-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

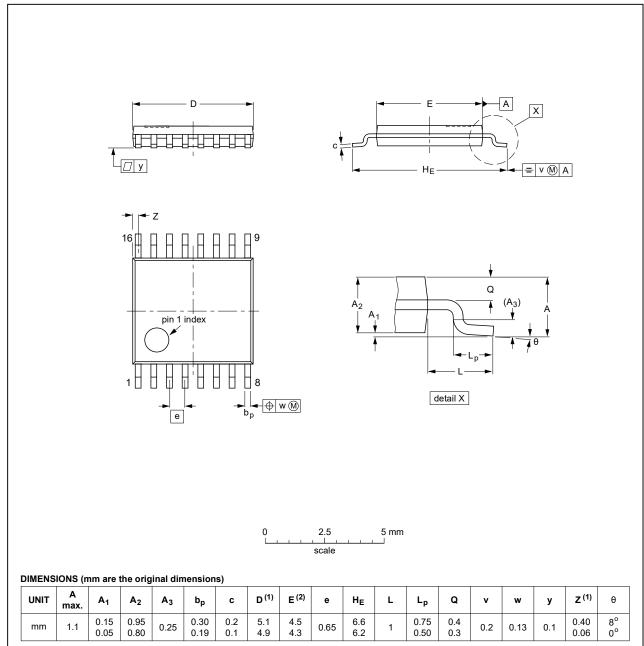
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	1330E DATE	
SOT109-1	076E07	MS-012				99-12-27 03-02-19	

Fig. 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

	OUTLINE		REFER	EUROPEAN	ISSUE DATE		
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT403-1		MO-153				99-12-27 03-02-18

Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

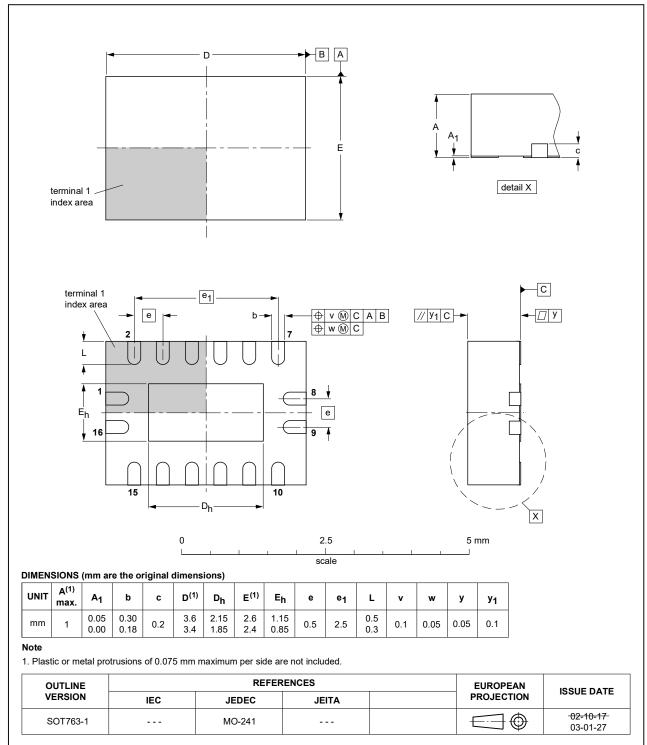


Fig. 16. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT595_Q100 v.2	20200526	Product data sheet	-	74AHC_AHCT595_Q100 v.1
Modifications:	guidelines o Legal texts I Section 1 ar Fig. 7: Timin Table 4: Der	of this data sheet has been f Nexperia. In ave been adapted to the rand Section 2 updated. In diagram updated with SI rating values for P _{tot} total pagation delay symbol and	new company nan HCP waveform. ower dissipation ι	ne where appropriate. updated.
74AHC_AHCT595_Q100 v.1	20120712	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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