

74AHCV05A

Hex inverter Schmitt trigger with open-drain outputs

Rev. 1 — 24 June 2019

Product data sheet

1. General description

The 74AHCV05A is a hex inverter with Schmitt trigger inputs and open-drain outputs. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

The data (nA) inputs include Schmitt trigger inputs capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

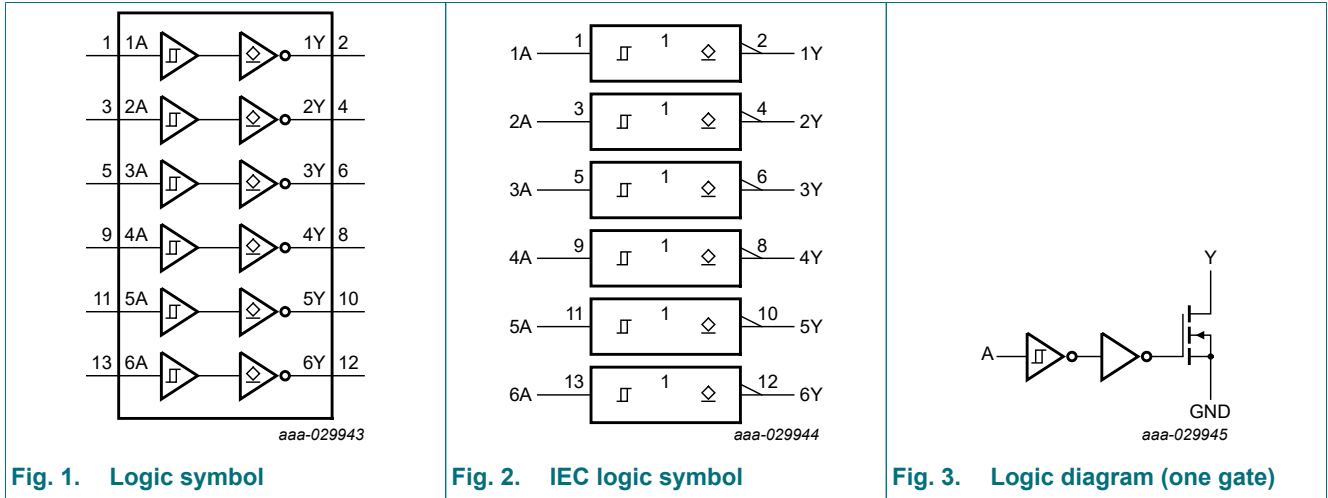
- Wide supply voltage range from 1.8 V to 5.5 V
- Typical t_{PZL} of 3.6 ns at 5 V
- Typical $V_{OL(p)} < 0.8$ V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3 kV
 - MM: JESD22-A115-A exceeds 150 V
 - CDM: ANSI/ESDA/JEDEC JS-002 Class C3, exceeds 2 kV
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

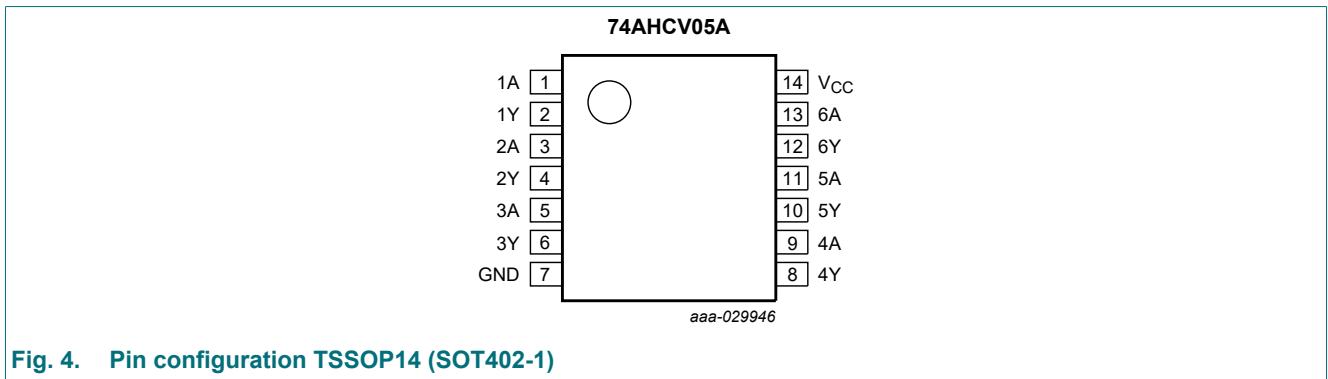
Type number	Package			
	Temperature range	Name	Description	Version
74AHCV05APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
nA	nY
L	Z
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output LOW state, 3-state or power-down [2]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0\text{ V}$	-50	-	mA
I_{OK}	output clamping current	$V_O < 0\text{ V}$	-50	-	mA
I_O	output current	$V_O = 0\text{ V to }V_{CC}$	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$ [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For TSSOP14 packages: above 75 °C the value of P_{tot} derates linearly at 7 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.8	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output LOW state, 3-state or power-down	0	-	5.5	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	50	ms/V
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	20	ms/V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	1	ms/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	positive-going threshold voltage	V _{CC} = 1.8 V	-	-	1.65	-	1.65	-	1.65	V
		V _{CC} = 2.3 V	-	-	1.85	-	1.85	-	1.85	V
		V _{CC} = 3.0 V	-	-	2.2	-	2.2	-	2.2	V
		V _{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
		V _{CC} = 5.5 V	-	-	3.85	-	3.85	-	3.85	V
V _{T-}	negative-going threshold voltage	V _{CC} = 1.8 V	0.15	-	-	0.15	-	0.15	-	V
		V _{CC} = 2.3 V	0.45	-	-	0.45	-	0.45	-	V
		V _{CC} = 3.0 V	0.9	-	-	0.9	-	0.9	-	V
		V _{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
		V _{CC} = 5.5 V	1.65	-	-	1.65	-	1.65	-	V
V _H	hysteresis voltage	V _{CC} = 1.8 V	0.15	-	1.05	0.15	1.05	0.15	1.05	V
		V _{CC} = 2.3 V	0.2	-	1.1	0.2	1.1	0.2	1.1	V
		V _{CC} = 3.0 V	0.3	-	1.2	0.3	1.2	0.3	1.2	V
		V _{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.4	1.4	V
		V _{CC} = 5.5 V	0.5	-	1.6	0.5	1.6	0.5	1.6	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}								
		I _O = 50 μA; V _{CC} = 1.8 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.44	V
I _O = 16 mA; V _{CC} = 4.5 V	-	-	0.44	-	0.55	-	0.55	V		
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _O = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	μA
I _{OFF}	power-off leakage current	V _I or V _O = GND to 5.5 V; V _{CC} = 0 V	-	-	0.5	-	5	-	5	μA
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2	-	20	-	20	μA

9.1. Transfer characteristics waveforms

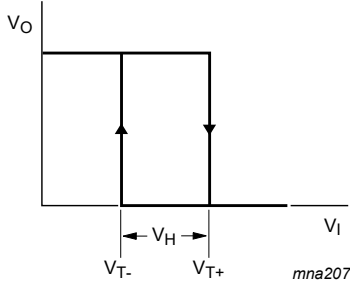


Fig. 5. Transfer characteristics

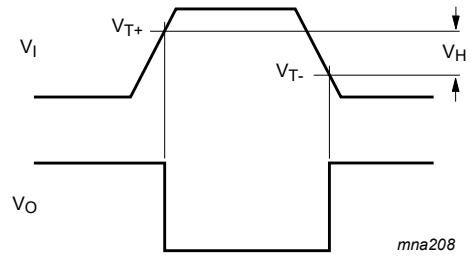
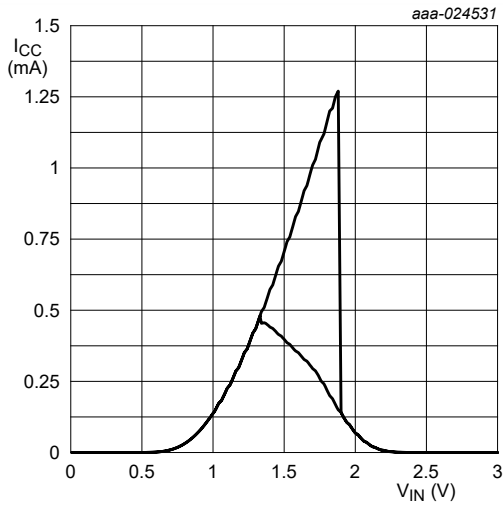
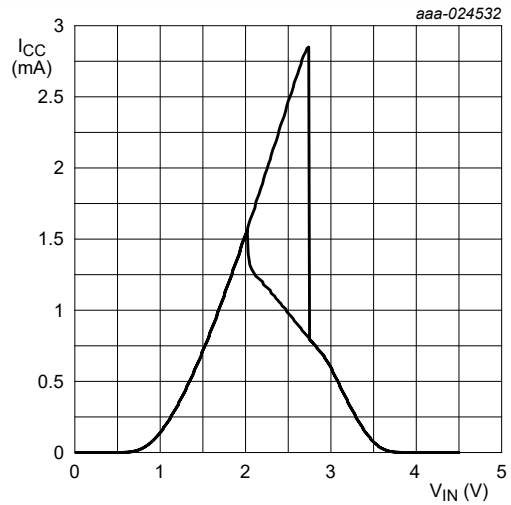


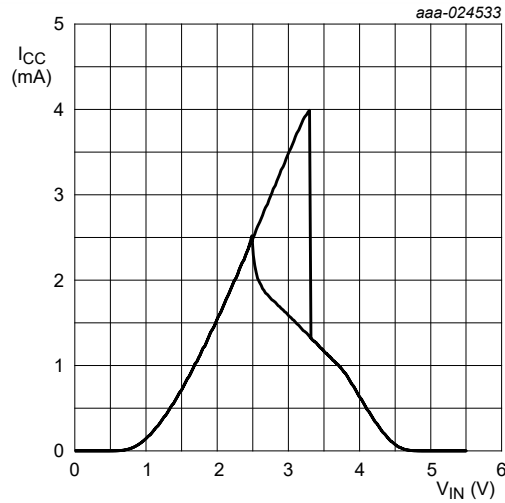
Fig. 6. Transfer characteristics definitions



a. $V_{CC} = 3.0\text{ V}$



b. $V_{CC} = 4.5\text{ V}$



c. $V_{CC} = 5.5\text{ V}$

Fig. 7. Typical transfer characteristics

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$. For test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 8								
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.8	12.2	1	15	1	17	ns
		$C_L = 50\text{ pF}$	-	8.2	16.6	1	19.5	1	21.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	4.6	7.1	1	8.5	1	10.0	ns
		$C_L = 50\text{ pF}$	-	6.5	10.6	1	12	1	13.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.6	5.5	1	6.5	1	7.5	ns
		$C_L = 50\text{ pF}$	-	5.3	7.5	1	8.5	1	9.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 8								
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.4	10.5	1	12.0	1	14.0	ns
		$C_L = 50\text{ pF}$	-	10.0	15.2	1	18	1	20.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	4.3	7.2	1	9.0	1	10.5	ns
		$C_L = 50\text{ pF}$	-	7.7	10.6	1	12	1	13.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.4	5.5	1	6.5	1	7.5	ns
		$C_L = 50\text{ pF}$	-	5.6	7.5	1	8.5	1	9.5	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 3.3\text{ V}$	-	2	6	-	6	-	6	pF
C_O	output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 3.3\text{ V}$	-	5	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per buffer; $C_L = 0\text{ pF}$; [2] $f = 10\text{ MHz}$; $V_{CC} = 5\text{ V}$; $V_I = \text{GND to }V_{CC}$	-	3	-	-	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 2.5\text{ V}$, 3.3 V , and 5 V respectively, unless otherwise specified.

[2] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

Table 8. Noise characteristics

$GND = 0\text{ V}$. For test circuit see [Fig. 9](#).

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			Unit
			Min	Typ	Max	
$V_{CC} = 3.3\text{ V}$; $C_L = 50\text{ pF}$						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.3	0.8	V
$V_{OL(v)}$	LOW-level output voltage (valley)		-0.8	-0.1	-	V
$V_{IH(AC)}$	AC HIGH-level input voltage (dynamic)		2.31	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage (dynamic)		-	-	0.99	V
$V_{CC} = 5.0\text{ V}$; $C_L = 50\text{ pF}$						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.6	-	V
$V_{OL(v)}$	LOW-level output voltage (valley)		-	-0.4	-	V
$V_{IH(AC)}$	AC HIGH-level input voltage (dynamic)		3.5	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage (dynamic)		-	-	1.5	V

10.1. Waveforms and test circuit

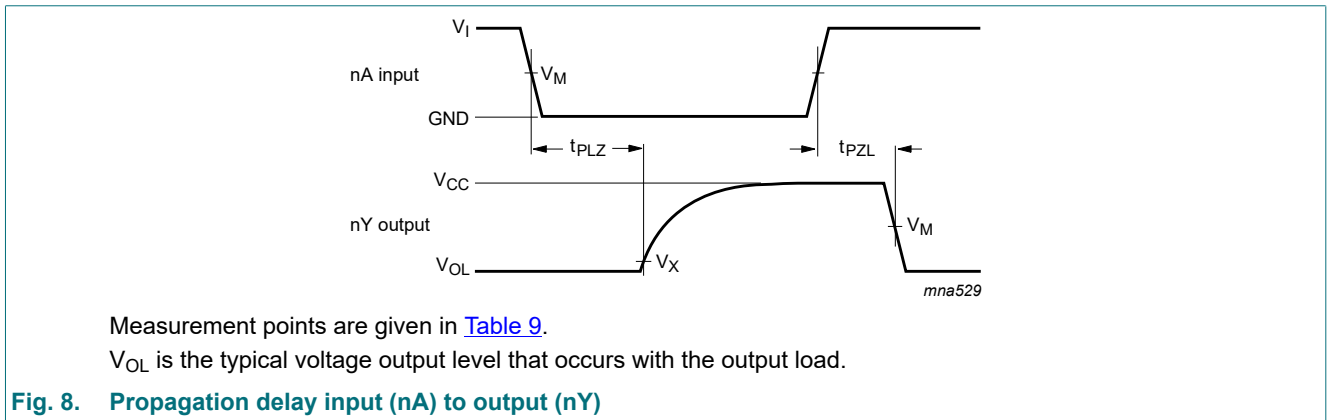


Table 9. Measurement points

Input	Output	
V_M	V_M	V_X
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3\text{ V}$

Hex inverter Schmitt trigger with open-drain outputs

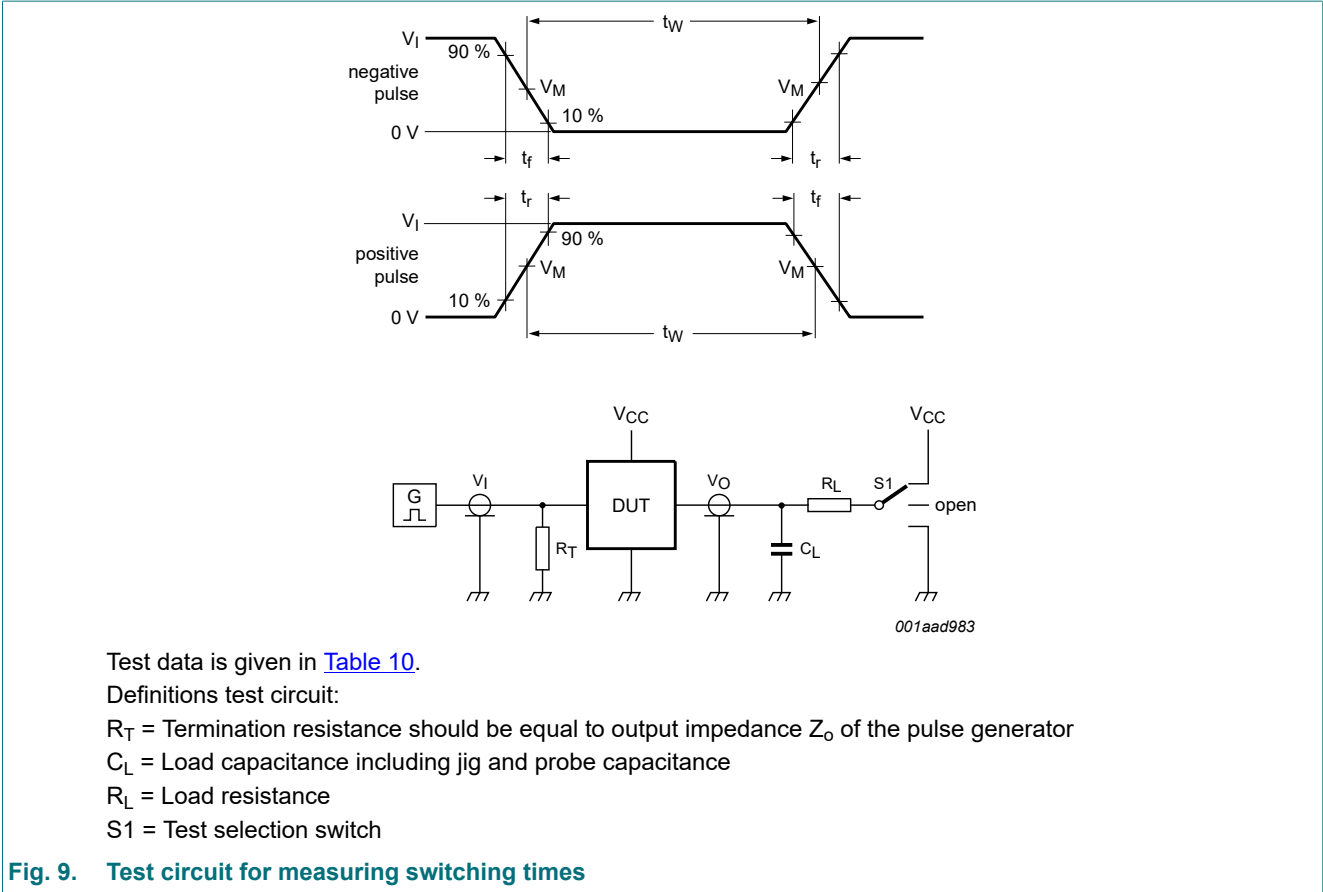


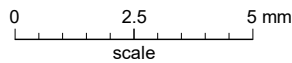
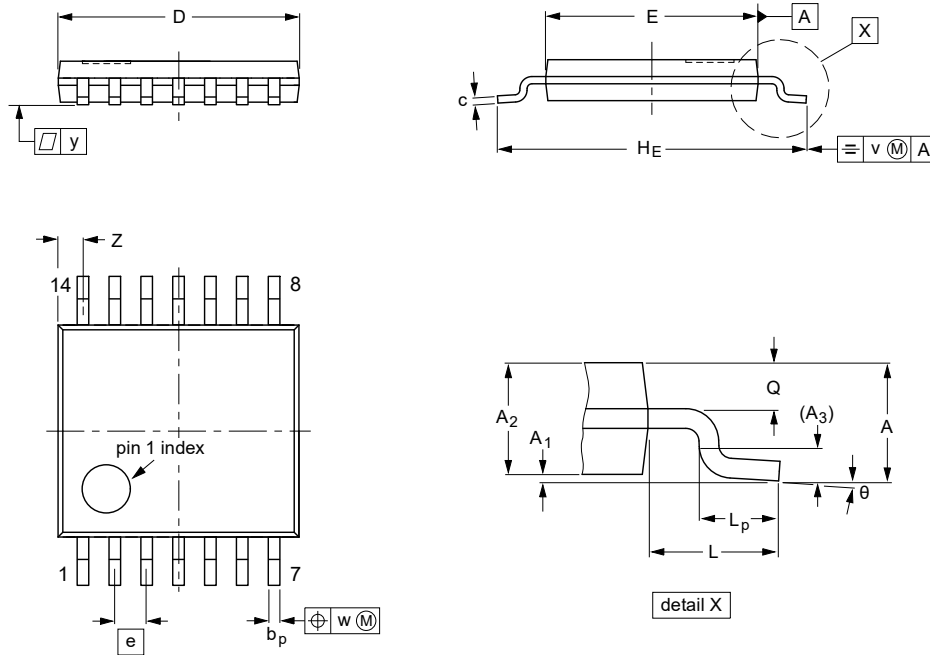
Table 10. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PLZ}, t_{PZL}
GND to V_{CC}	3.0 ns	15 pF, 50 pF	1 k Ω	V_{CC}

11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

Fig. 10. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCV05A v.1	20190624	Product data sheet	-	-

Hex inverter Schmitt trigger with open-drain outputs

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[NLV27WZU04DFT2G](#) [NLV17SG14DFT2G](#) [74ACT14SC](#) [BU4069UBF-E2](#) [EMPP008Z](#) [NLV14106BDTR2G](#) [NLV74AC14DTR2G](#)
[SN74HCT04DE4](#) [ODE-3-120023-1F12](#) [74VHCT04AM](#) [TC74HC04APF](#) [TC7SH04F,LJ\(CT](#) [CD74HC14M96](#) [TC7W14FK,LF](#)
[74VHC14MTCX](#) [74LCX14MTC](#) [SN74LVC1GU04DBVR](#) [SN74LVC14APWR](#) [NLU1G14BMX1TCG](#) [NLU2G04AMX1TCG](#)
[NLU3G14AMX1TCG](#) [NLVVHC1G04DFT2G](#) [NLX2G04CMX1TCG](#) [NLX3G14AMX1TCG](#)