

74ALVC125

Quad buffer/line driver; 3-state

Rev. 4 — 30 April 2021

Product data sheet

1. General description

The 74ALVC125 is a quad non-inverting buffer/line driver with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A HIGH on the nOE pin causes the outputs to assume a high-impedance OFF-state.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B (2.7 V to 3.6 V)
- ESD protection:
 - MM JESD22-A115-A exceeds 200 V
 - HBM JESD22-A114E exceeds 2000 V
- Multiple package options
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC125D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC125PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC125BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

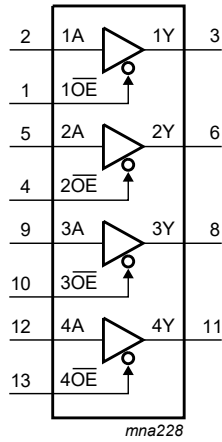


Fig. 1. Logic symbol

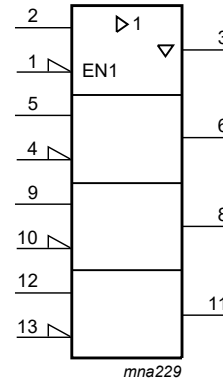


Fig. 2. IEC logic symbol

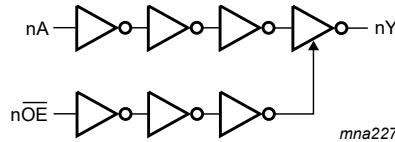


Fig. 3. Logic diagram (one buffer)

5. Pinning information

5.1. Pinning

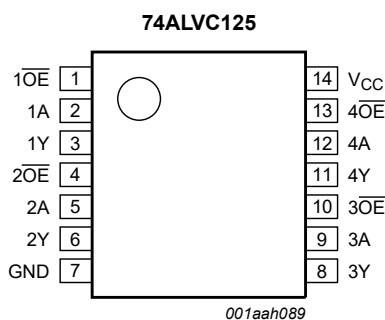
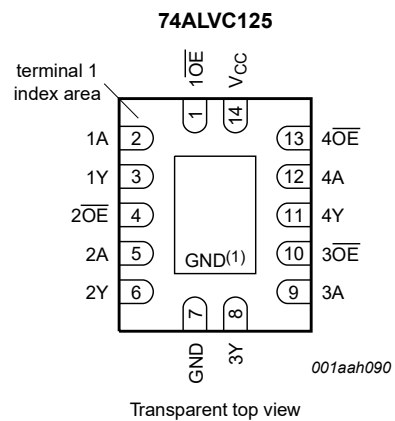


Fig. 4. Pin configuration SOT108-1 (SO14) and SOT402-1 (TSSOP14)



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	2, 5, 9, 12	data input
nY	3, 6, 8, 11	bus output
n $\overline{\text{OE}}$	1, 4, 10, 13	output enable (active LOW)
V _{CC}	14	supply voltage
GND	7	ground (0 V)

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
n $\overline{\text{OE}}$	nA	nY
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{CC}	supply voltage		-0.5	+4.6	V	
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA	
V _I	input voltage	[1]	-0.5	+4.6	V	
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA	
V _O	output voltage	output HIGH or LOW state	[1]	-0.5	V _{CC} + 0.5	V
		output 3-state		-0.5	+4.6	V
		Power-down mode; V _{CC} = 0 V		-0.5	+4.6	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA	
I _{CC}	supply current		-	100	mA	
I _{GND}	ground current		-100	-	mA	
T _{stg}	storage temperature		-65	+150	°C	
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	[2]	500	mW	

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	3.6	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100$ μ A; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6$ mA; $V_{CC} = 1.65$ V	1.25	1.51	-	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	1.8	2.10	-	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	1.7	2.01	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.53	-	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	2.4	2.76	-	V
$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.2	2.68	-	V		
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100$ μ A; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 1.65$ V	-	0.11	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	-	0.17	0.4	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	-	0.25	0.6	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.16	0.4	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	-	0.23	0.4	V
$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	0.30	0.55	V		
I_I	input leakage current	$V_{CC} = 3.6$ V; $V_I = 3.6$ V or GND	-	± 0.1	± 5	μ A
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 1.65$ V to 3.6 V; $V_O = 3.6$ V or GND;	-	± 0.1	± 10	μ A
I_{OFF}	power-off leakage current	$V_{CC} = 0$ V; V_I or $V_O = 0$ V to 3.6 V	-	± 0.1	± 10	μ A

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	10	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	750	μA
C _I	input capacitance		-	3.5	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 6 [2]				
		V _{CC} = 1.65 V to 1.95 V	1.3	2.4	5.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	1.7	3.2	ns
		V _{CC} = 2.7 V	-	2.0	3.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	1.8	2.8	ns
t _{en}	enable time	nOE to nY; see Fig. 7 [2]				
		V _{CC} = 1.65 V to 1.95 V	1.4	3.9	6.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.2	4.1	ns
		V _{CC} = 2.7 V	-	2.7	4.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	1.9	3.5	ns
t _{dis}	disable time	nOE to nY; see Fig. 7 [2]				
		V _{CC} = 1.65 V to 1.95 V	1.8	3.9	5.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.1	3.4	ns
		V _{CC} = 2.7 V	-	2.9	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.4	2.7	4.0	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3]				
		outputs HIGH or LOW state	-	27	-	pF
		outputs 3-state	-	5	-	pF

[1] Typical values are measured at T_{amb} = 25 °C

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

t_{en} is the same as t_{PZH} and t_{PZL}.

t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

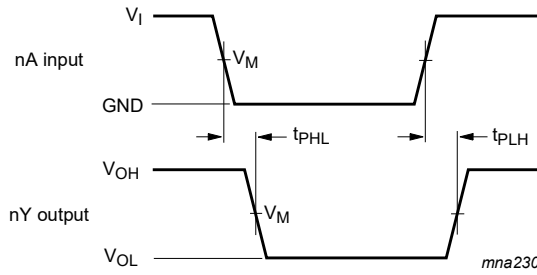
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

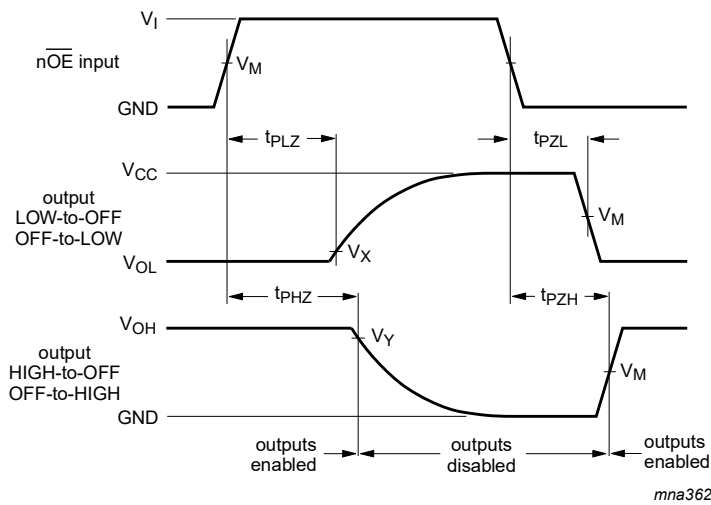
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig. 6. Input nA to output nY propagation delay times



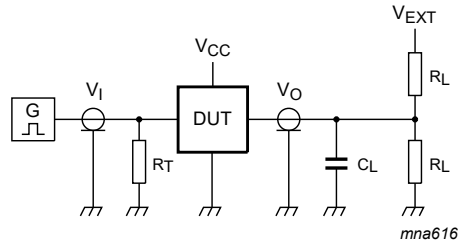
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig. 7. Enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	2 x V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 x V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

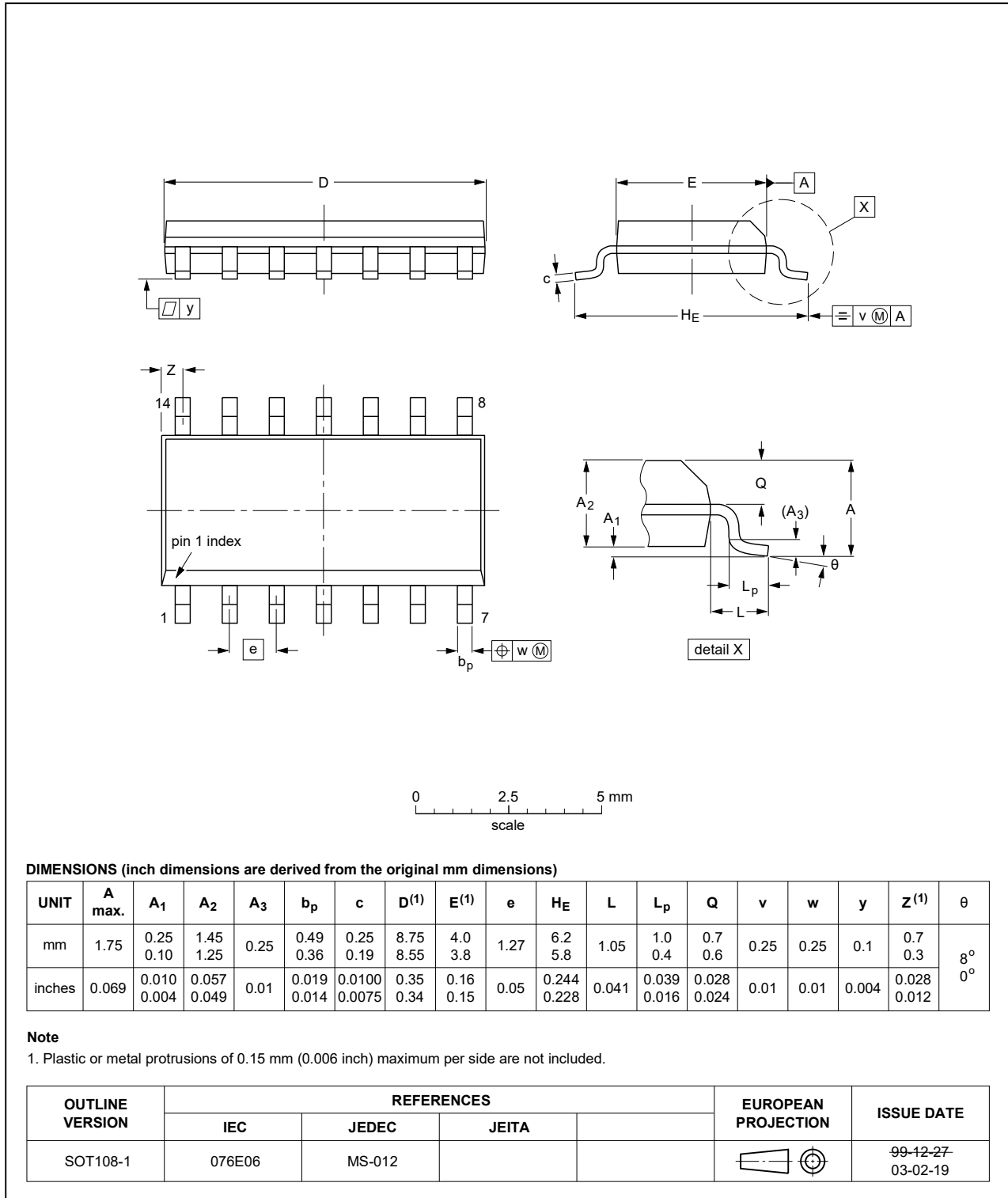


Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

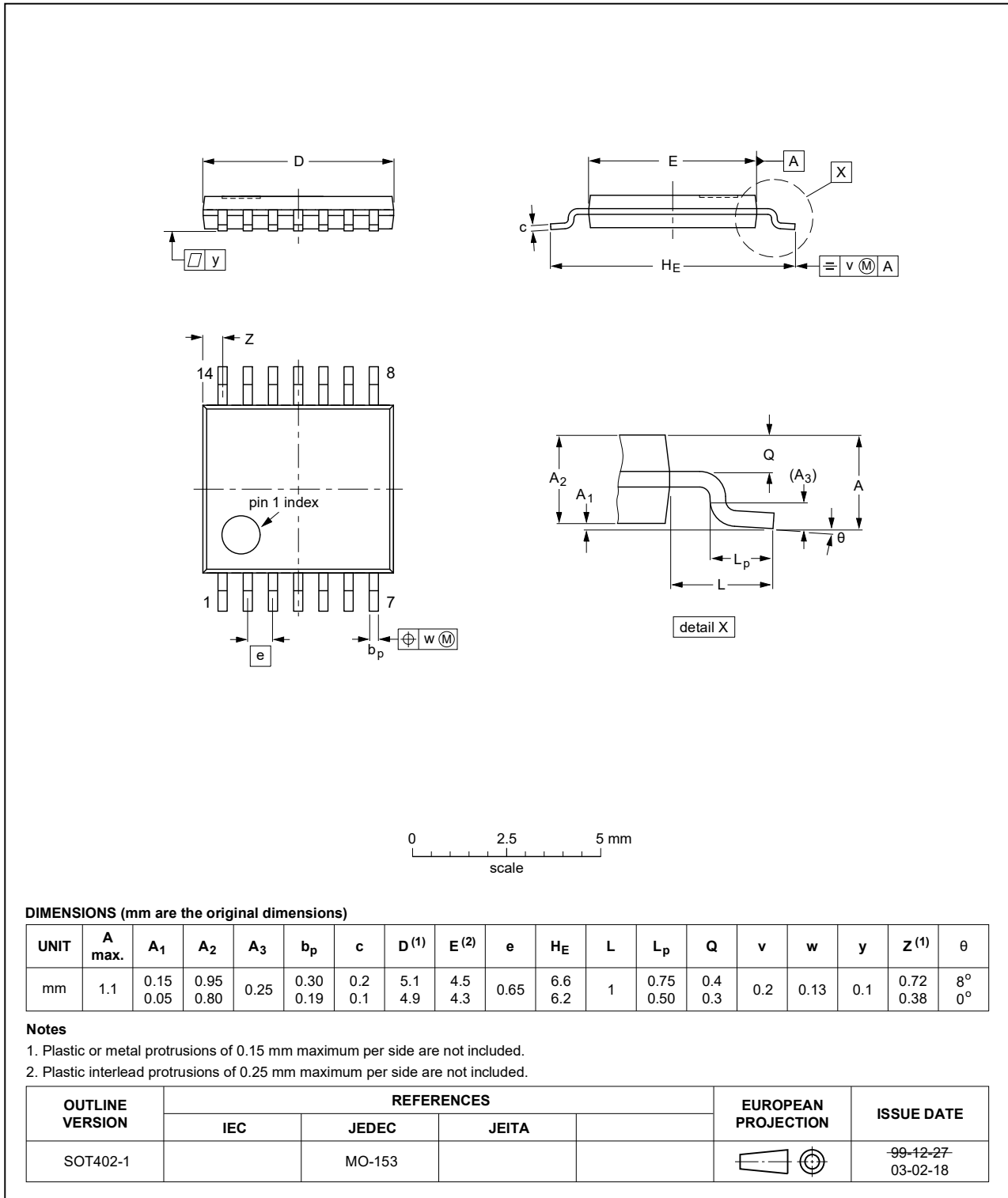


Fig. 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

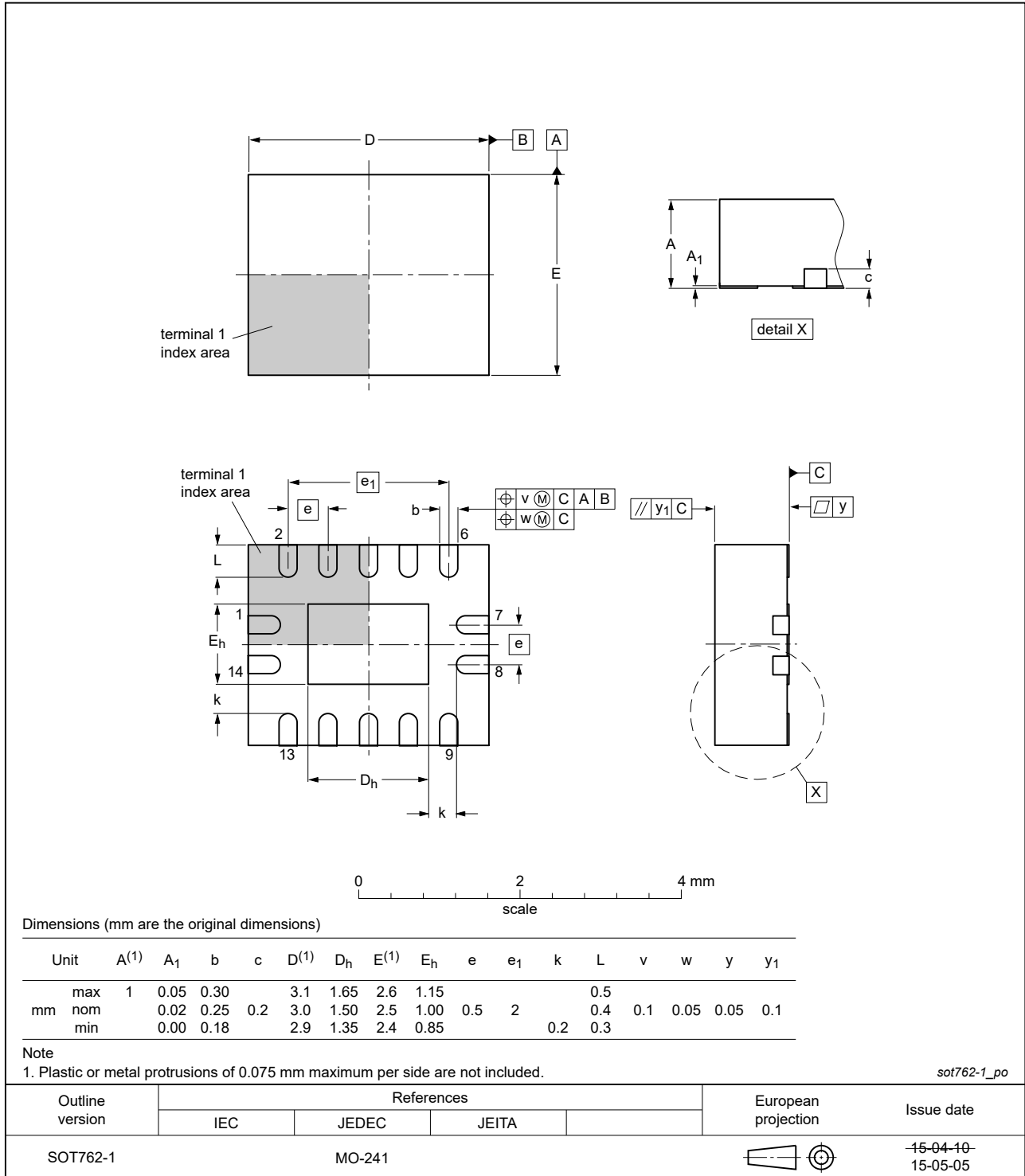


Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC125 v.4	20210430	Product data sheet	-	74ALVC125 v.3
Modifications:	<ul style="list-style-type: none"> • Section 2: Reference to JESD36 removed. • Table 4: Derating values for P_{tot} total power dissipation updated (errata). 			
74ALVC125 v.3	20200924	Product data sheet	-	74ALVC125 v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 4: Derating values for P_{tot} total power dissipation have been updated. • Package outline drawing of SOT762-1 (Fig. 11) updated. 			
74ALVC125 v.2	20080110	Product data sheet	-	74ALVC125 v.1
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: DHVQFN14 package added. • Section 7: derating values added for DHVQFN14 package. • Section 11: outline drawing added for DHVQFN14 package. 			
74ALVC125 v.1	20021118	Product specification	-	-

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[NLV37WZ07USG](#) [RHRXH162244K1](#) [74AUP1G34FW5-7](#) [74AUP1G07FW5-7](#) [74LVC2G126RA3-7](#) [NLX2G17CMUTCG](#)
[74LVCE1G125FZ4-7](#) [Le87501NQC](#) [74AUP1G126FW5-7](#) [TC74HC4050AP\(F\)](#) [74LVCE1G07FZ4-7](#) [NLX3G16DMUTCG](#)
[NLX2G06AMUTCG](#) [NLU2G17AMUTCG](#) [LE87100NQC](#) [LE87100NQCT](#) [LE87285NQC](#) [LE87285NQCT](#) [LE87290YQC](#) [LE87290YQCT](#)
[LE87511NQC](#) [LE87511NQCT](#) [LE87557NQC](#) [LE87557NQCT](#) [LE87614MQC](#) [LE87614MQCT](#) [LE87286NQCT](#)