

74ALVC541

Octal buffer/line driver; 3-state

Rev. 5 — 30 April 2021

Product data sheet

1. General description

The 74ALVC541 is an octal non-inverting buffer/line drivers with 3-state bus compatible outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}0$ and $\overline{OE}1$. A HIGH on $\overline{OE}n$ causes the outputs to assume a high-impedance OFF-state.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.5 V)
 - JESD8B (2.7 V to 3.6 V)
- 3.6 V tolerant inputs/outputs
- CMOS LOW power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC541D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC541PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC541BQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

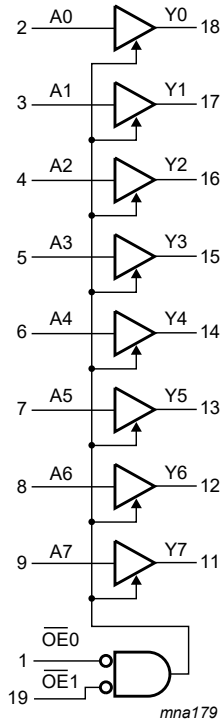


Fig. 1. Logic symbol

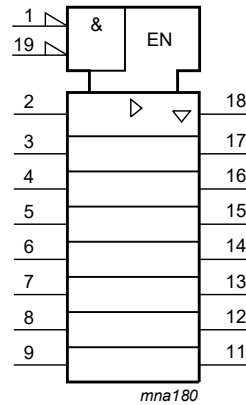


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning

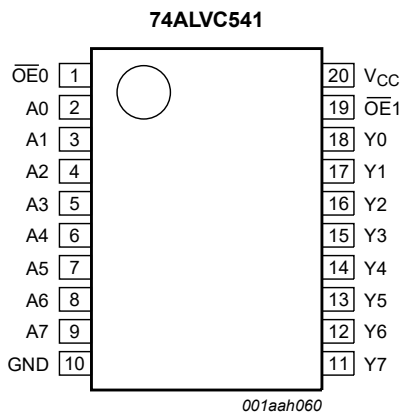
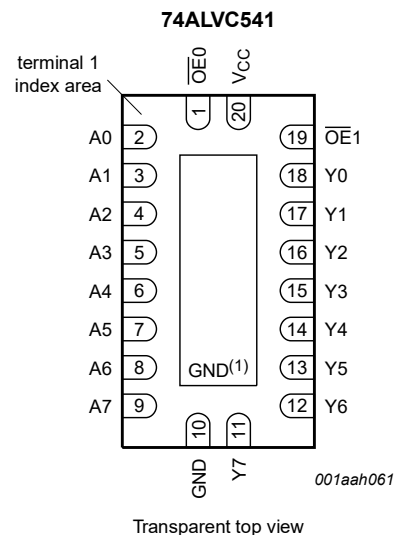


Fig. 3. Pin configuration SOT163-1 (SO20) and SOT360-1 (TSSOP20)



Transparent top view
 (1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 4. Pin configuration SOT764-1 (DHVQFN20)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}0$	1	output enable input (active LOW)
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	18, 17, 16, 15, 14, 13, 12, 11	data output
$\overline{OE}1$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Functional table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control		Input	Output
$\overline{OE}0$	$\overline{OE}1$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	output HIGH or LOW state [2]	-0.5	$V_{CC} + 0.5$	V
		output 3-state [2]	-0.5	+4.6	V
		power-down mode; $V_{CC} = 0$ V	-0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	3.6	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40$ °C to +85 °C			Unit
			Min	Typ[1]	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100$ μ A; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = 6$ mA; $V_{CC} = 1.65$ V	1.25	-	-	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	1.8	-	-	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	1.7	-	-	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	2.2	-	-	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	2.4	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100$ μ A; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = -6$ mA; $V_{CC} = 1.65$ V	-	-	0.3	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	-	-	0.4	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	-	-	0.6	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	-	-	0.4	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	-	-	0.4	V
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 3.6$ V	-	± 0.1	± 10.0	μ A
		$V_I = V_{CC}$ or GND; $V_{CC} = 3.6$ V	-	± 0.1	± 5.0	μ A
I_{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	± 0.1	± 10.0	μ A

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V	-	0.2	10	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	750	μA
C _I	input capacitance		-	3.5	-	pF

[1] All typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V and 3.3 V.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t _{pd}	propagation delay	An to Yn; see Fig. 5 [2]				
		V _{CC} = 1.65V to 1.95 V	1.0	3.0	4.6	ns
		V _{CC} = 2.3V to 2.7 V	1.0	2.2	3.3	ns
		V _{CC} = 2.7 V	1.0	2.5	3.3	ns
t _{en}	enable time	OE _n to Yn; see Fig. 6 [2]				
		V _{CC} = 1.65V to 1.95 V	1.0	4.2	7.5	ns
		V _{CC} = 2.3V to 2.7 V	1.0	3.3	5.4	ns
		V _{CC} = 2.7 V	1.0	3.7	5.8	ns
t _{dis}	disable time	OE _n to Yn; see Fig. 6 [2]				
		V _{CC} = 1.65V to 1.95 V	1.0	4.8	7.5	ns
		V _{CC} = 2.3V to 2.7 V	1.0	3.1	4.5	ns
		V _{CC} = 2.7 V	1.0	3.1	4.8	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3]				
		outputs enabled	-	25	-	pF
		outputs disabled	-	0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V and 3.3 V.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

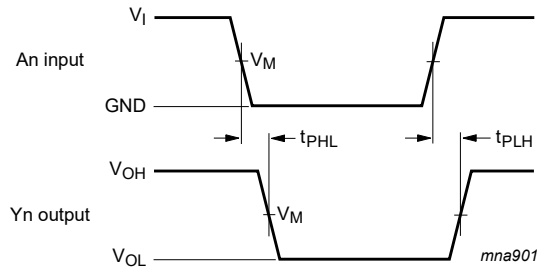
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

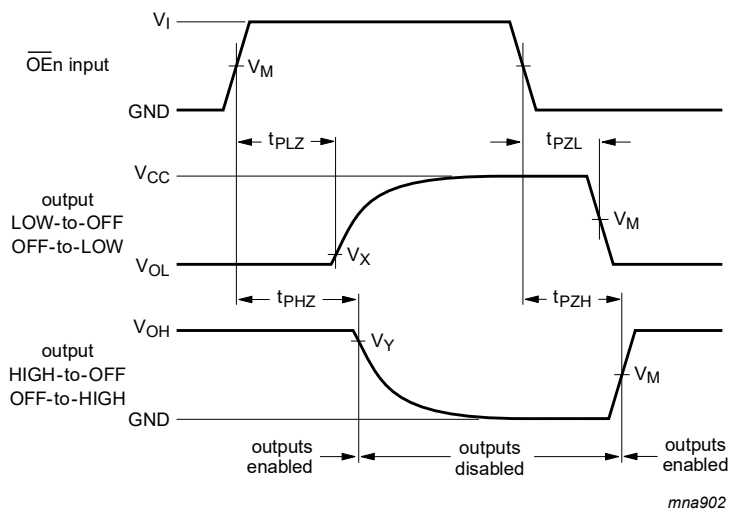
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Propagation delay input (An) to output (Yn)



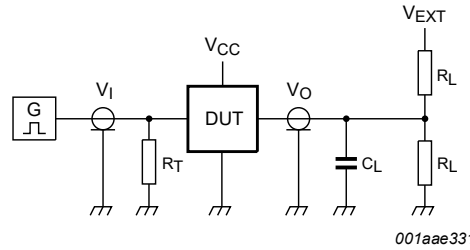
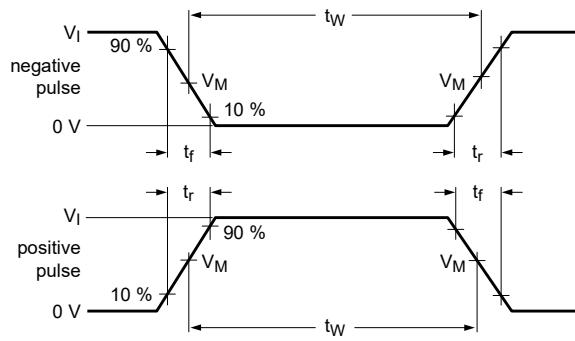
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.65 V to 1.65V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



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Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

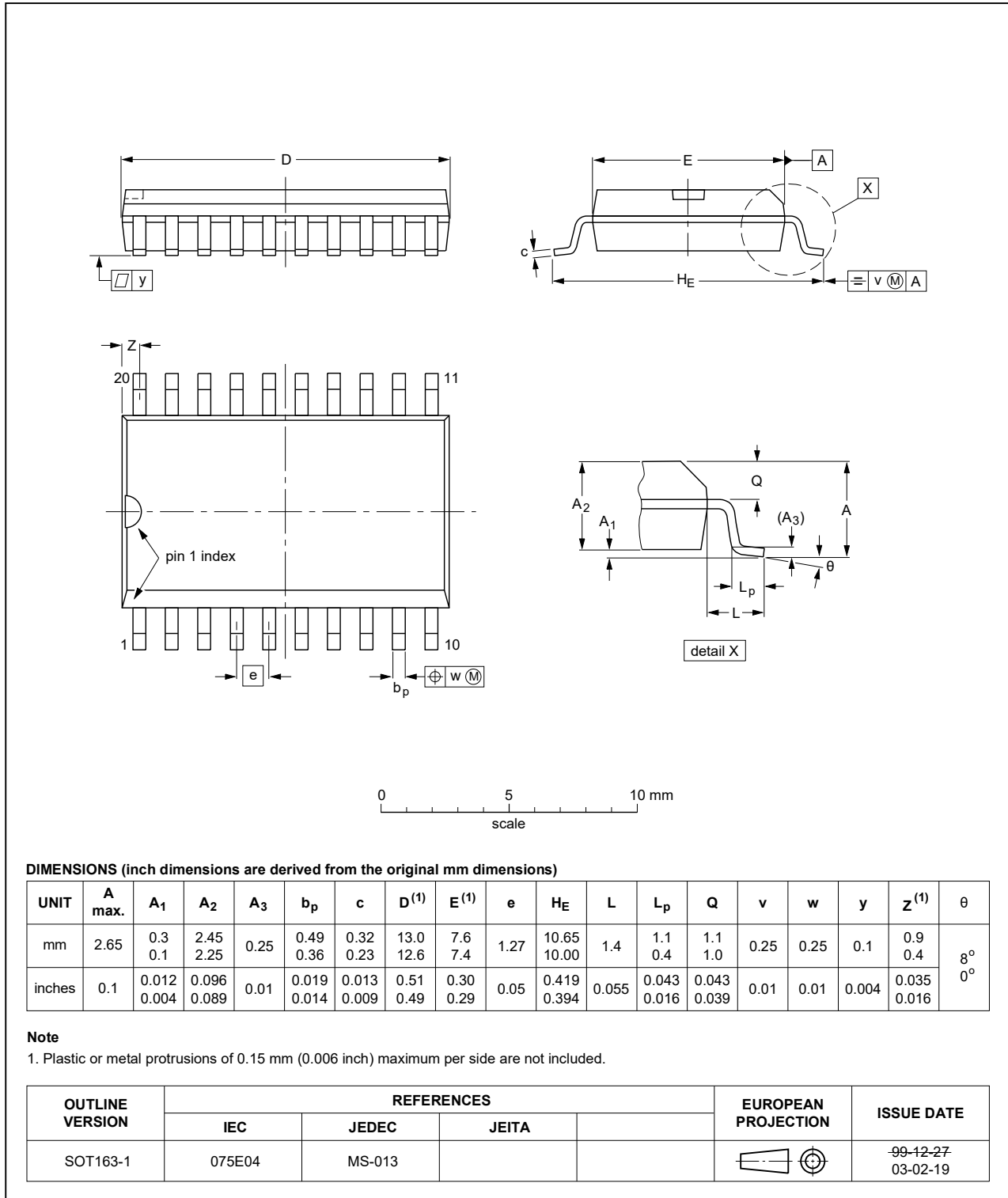


Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

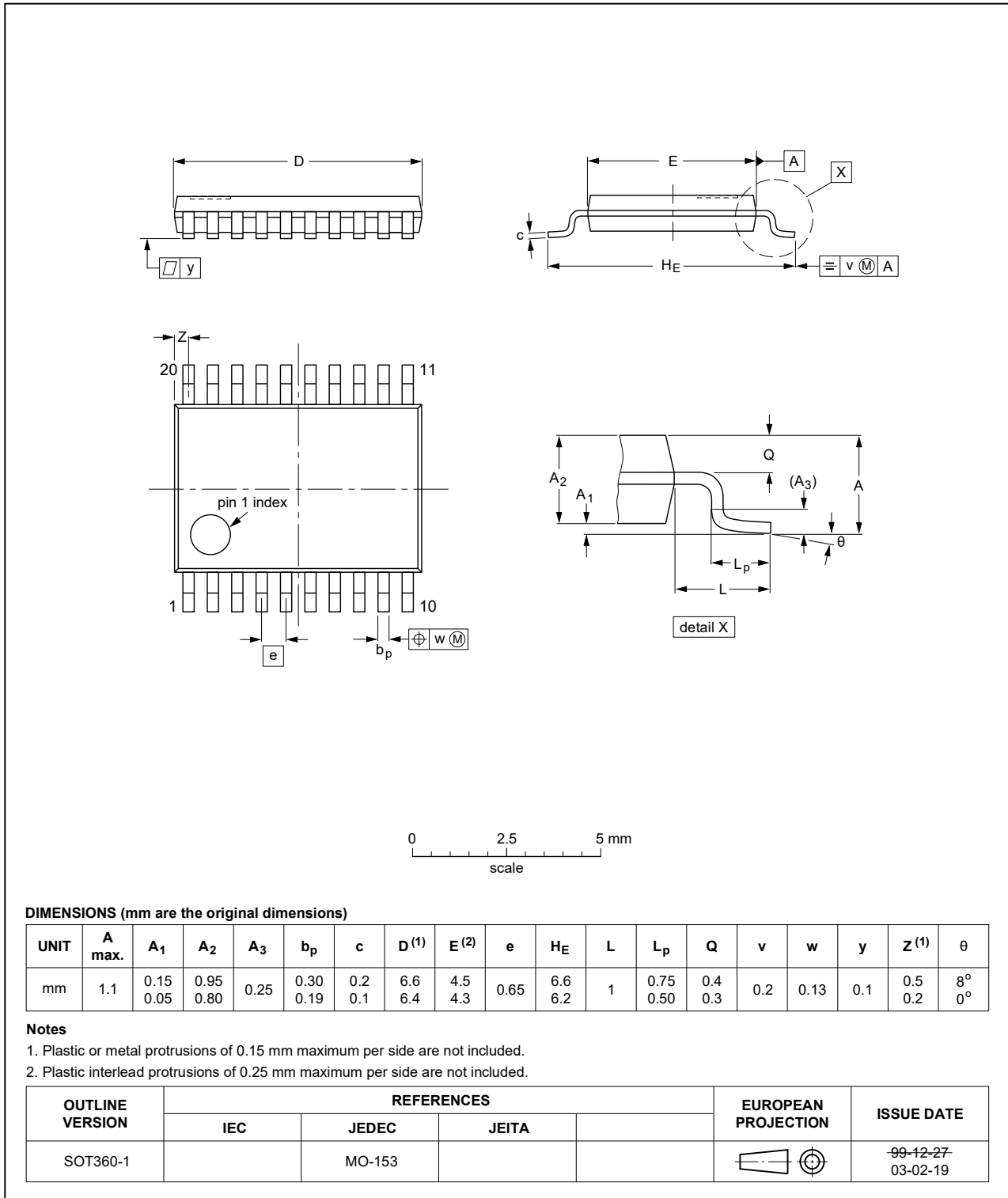


Fig. 9. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

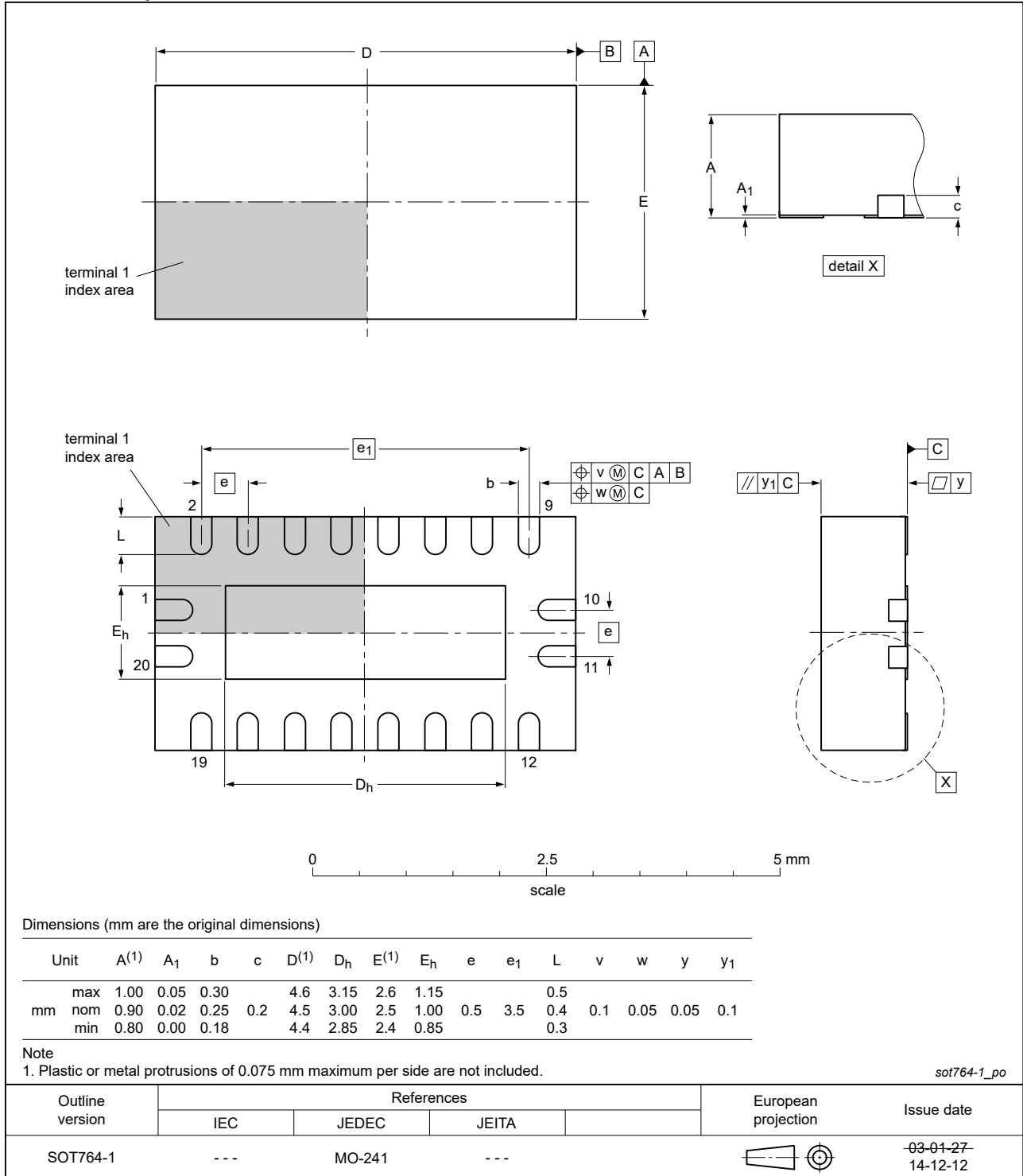


Fig. 10. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC541 v.5	20210430	Product data sheet	-	74ALVC541 v.4
Modifications:	<ul style="list-style-type: none"> • Section 2: Reference to JESD36 removed. • Table 4: Derating values for P_{tot} total power dissipation removed (errata). 			
74ALVC541 v.4	20200930	Product data sheet	-	74ALVC541 v.3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 4: Derating values for P_{tot} total power dissipation have been updated. • Table 6: typo corrected. • Table 7: typo corrected. • Package outline drawing of SOT764-1 (Fig. 10) updated. 			
74ALVC541 v.3	20140120	Product data sheet	-	74ALVC541 v.2
	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. 			
74ALVC541 v.2	20071210	Product data sheet	-	74ALVC541 v.1
74ALVC541 v.1	20021115	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[NLX2G06AMUTCG](#) [NLU2G17AMUTCG](#) [LE87100NQC](#) [LE87100NQCT](#) [LE87285NQC](#) [LE87285NQCT](#) [LE87290YQC](#) [LE87290YQCT](#)
[LE87511NQC](#) [LE87511NQCT](#) [LE87557NQC](#) [LE87557NQCT](#) [LE87614MQC](#) [LE87614MQCT](#) [LE87286NQCT](#)