74ALVCH162827

20-bit buffer/line driver; non-inverting; with 30 Ω termination resistors; 3-state

Rev. 2 — 19 January 2018 Product data sheet

1 General description

The 74ALVCH162827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NAND output enables ($n\overline{OE1}$ and $n\overline{OE2}$) for maximum control flexibility.

The 74ALVCH162827 is designed with 30 Ω series resisters in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

To ensure the high impedance state during power up or power down, $n\overline{OE}$n should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The 74ALVCH162827 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2 Features and benefits

- CMOS low power consumption
- MultiByte flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Bus hold on data inputs
- Current drive ± 12 mA at 3.0 V
- Integrated 30 Ω termination resistors
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH162827DGG	−40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4 Functional diagram

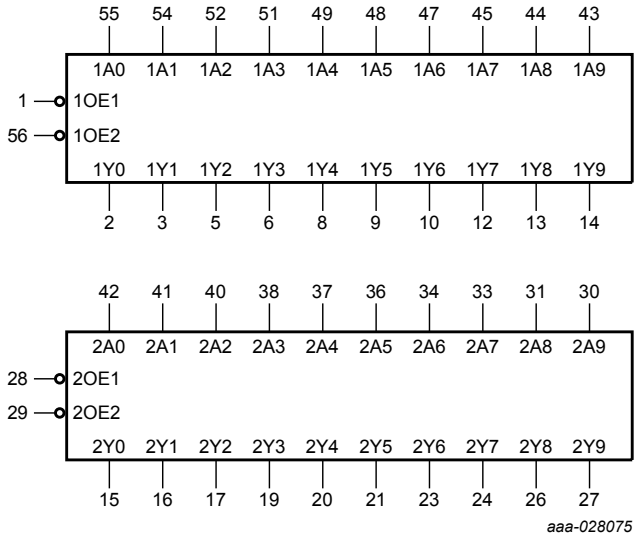


Figure 1. Logic symbol

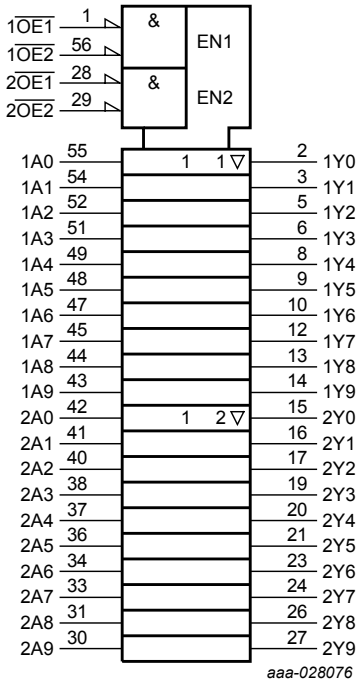


Figure 2. IEC logic symbol

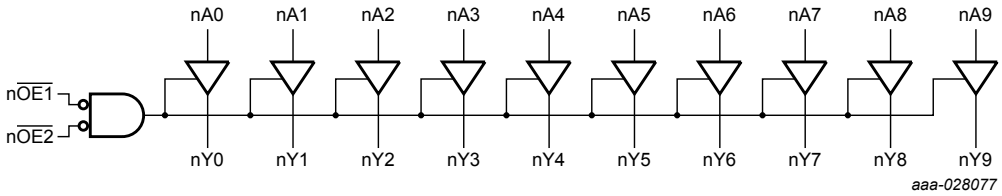


Figure 3. Logic diagram

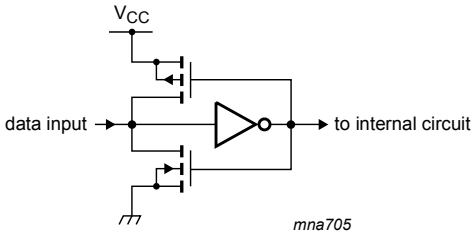


Figure 4. Bus hold circuit

5 Pinning information

5.1 Pinning

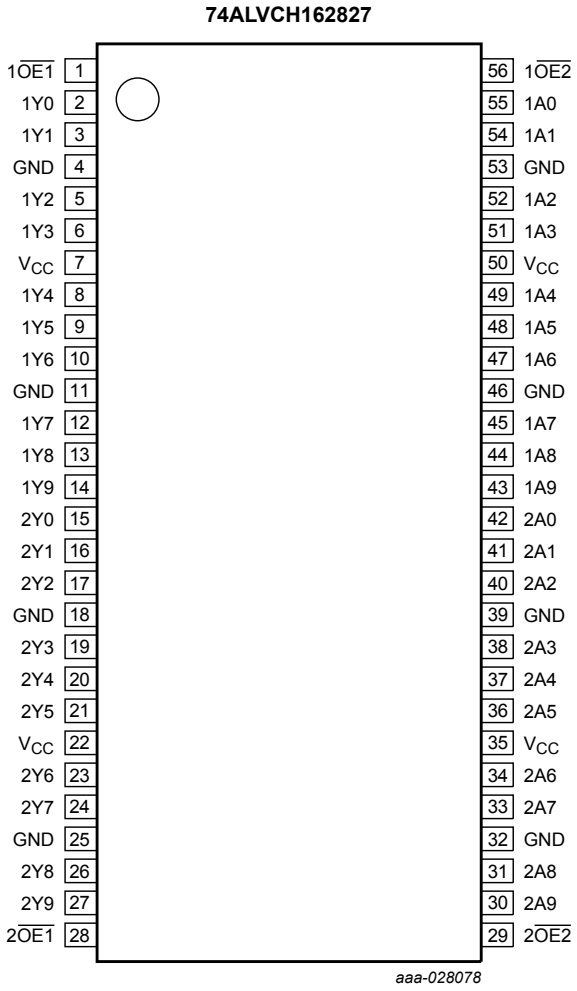


Figure 5. Pin configuration SOT364-1 (TSSOP56)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8, 1A9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data input
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7, 2A8, 2A9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data input
1Y0, 1Y1, 1Y2, 1Y3, 1Y4, 1Y5, 1Y6, 1Y7, 1Y8, 1Y9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data output
2Y0, 2Y1, 2Y2, 2Y3, 2Y4, 2Y5, 2Y6, 2Y7, 2Y8, 2Y9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data output
$1\overline{OE1}$, $1\overline{OE2}$, $2\overline{OE1}$, $2\overline{OE2}$	1, 56, 28, 29	output enable input (active-LOW)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V_{CC}	7, 22, 35, 50	positive voltage supply

6 Functional description

Table 3. Function table

X = don't care; Z = High-impedance OFF-state; H = HIGH voltage level; L = LOW voltage level.

Operating mode	Input		Output
	$n\overline{OEn}$	**nAn**	**nYn**
transparent	L	L	L
transparent	L	H	H
High-impedance	H	X	Z

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+4.6	V
V_I	input voltage	[1]	−0.5	+4.6	V
V_O	output voltage	[1]	−0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V	−50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V	-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		−100	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +85 °C [2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For TSSOP56 packages: above 55 °C derate linearly with 8 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	For maximum speed performance at C_L = 30 pF	2.3	2.7	V
		For maximum speed performance at C_L = 50 pF	3.0	3.6	V
V_I	input voltage		0	V_{CC}	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature	in free air	−40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	0	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions. T_{amb} = −40 °C to +85 °C; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 µA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -4 mA; V_{CC} = 2.3 V	V_{CC} - 0.4	V_{CC} - 0.11	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.17	-	V
		I_O = -4 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.09	-	V
		I_O = -8 mA; V_{CC} = 2.7 V	V_{CC} - 0.7	V_{CC} - 0.19	-	V
		I_O = -6 mA; V_{CC} = 3.0 V	V_{CC} - 0.6	V_{CC} - 0.13	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.27	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I_O = 4 mA; V_{CC} = 2.3 V	-	0.07	0.40	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.11	0.55	V
		I_O = 4 mA; V_{CC} = 2.7 V	-	0.06	0.40	V
		I_O = 8 mA; V_{CC} = 2.7 V	-	0.13	0.60	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.09	0.55	V
		I_O = 12 mA; V_{CC} = 3.0 V	-	0.19	0.80	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 2.3 V to 3.6 V	-	0.1	5	µA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V	45	-	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V	-45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V	-75	-175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V	-500	-	-	µA
I_{OZ}	OFF-state output current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	0.1	10	µA
I_{CC}	supply current	V_{CC} = 2.3 to 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.2	40	µA
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	150	750	µA
C_I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). T_{amb} = −40 °C to +85 °C. For test circuit, see Figure 8.

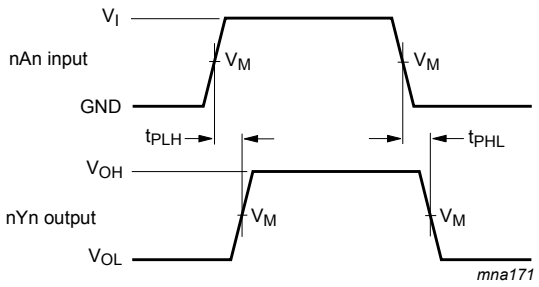
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
t_{pd}	propagation delay	nAn to nYn; see Figure 6 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.0	2.9	4.6	ns
		V_{CC} = 2.7 V	-	3.1	4.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	2.9	4.2	ns
t_{en}	enable time	$n\overline{OE}n$ to nYn; see Figure 7 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.4	3.9	6.4	ns
		V_{CC} = 2.7 V	-	4.4	6.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.6	3.7	5.4	ns
t_{dis}	disable time	$n\overline{OE}n$ to nYn; see Figure 7 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.7	2.2	5.9	ns
		V_{CC} = 2.7 V	-	3.2	5.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.8	3.0	4.7	ns
C_{PD}	power dissipation capacitance	per latch; V_I = GND to V_{CC} [3]				
		output enabled	-	14	-	pF
		output disabled	-	3	-	pF

[1] Typical values are measured at T_{amb} = 25 °C
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V

[2] t_{pd} is the same as t_{PHL} and t_{PLH};
t_{en} is the same as t_{PZH} and t_{PZL};
t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

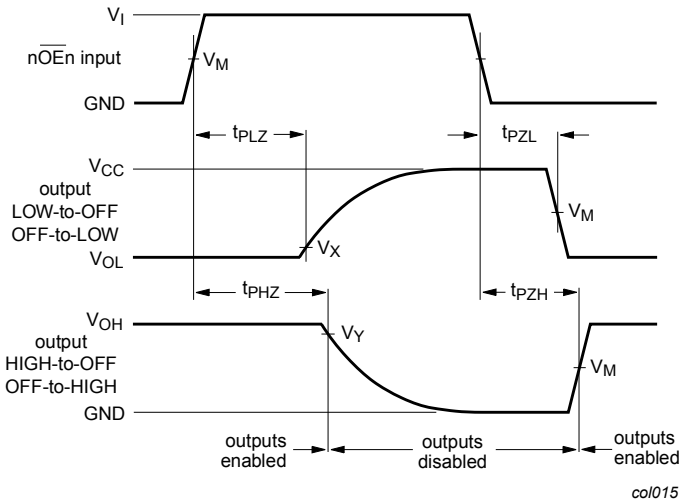
10.1 Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. Input (nAn) to output (nYn) propagation delays



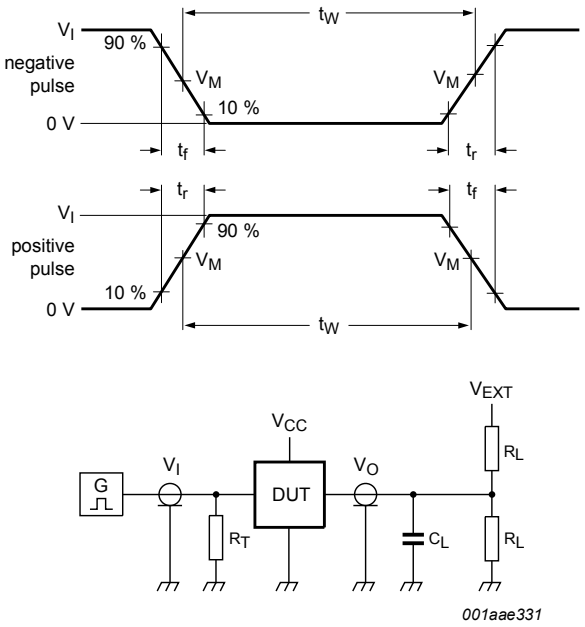
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 7. The 3-state output enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	V_{CC}	0.5 V_{CC}	0.5 V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

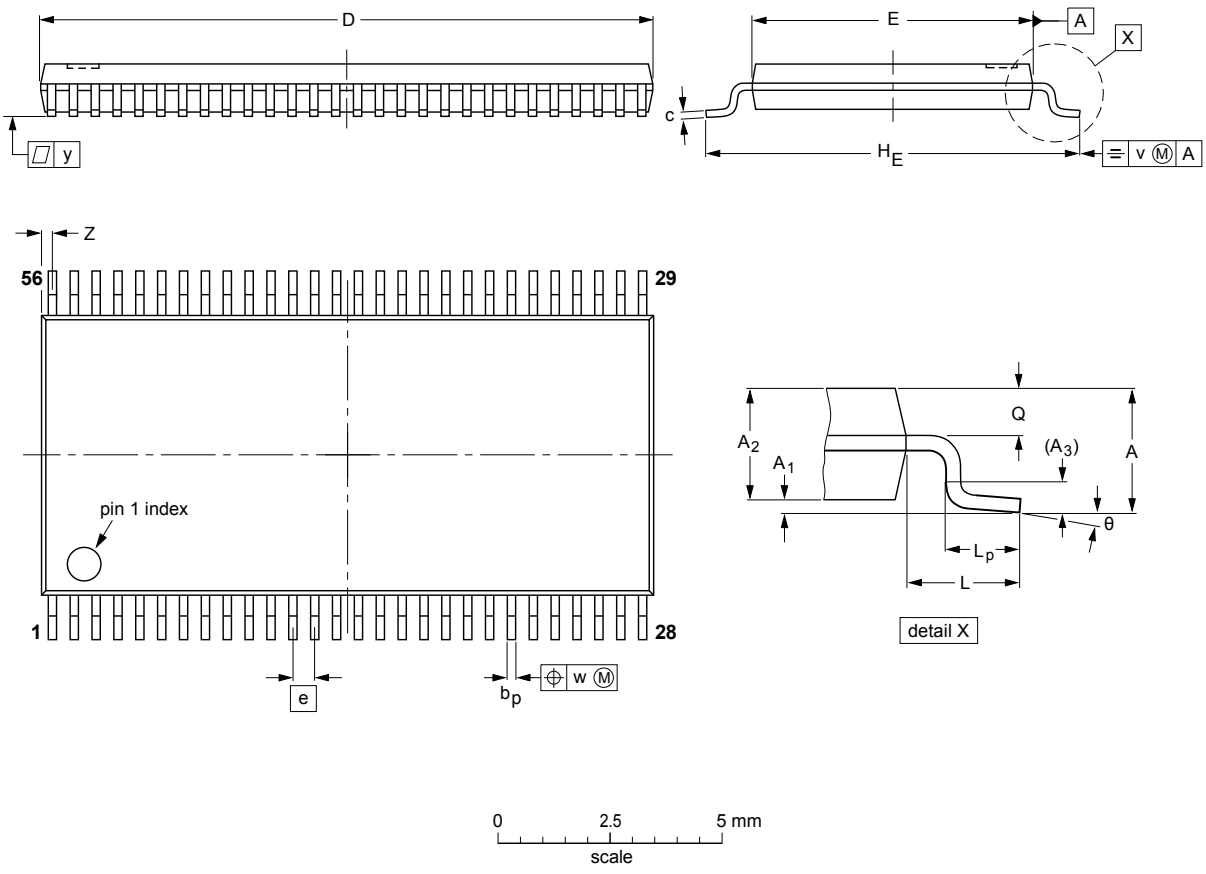
Figure 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

11 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Figure 9. Package outline SOT364-1 (TSSOP56)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH162827 v.2	20180119	Product data sheet	-	74ALVCH162827 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ALVCH162827 v.1	19980929	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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