74ALVCH16823

18-bit bus-interface D-type flip-flop with reset and enable; 3-state

Rev. 3 — 1 February 2018 Product data sheet

1 General description

The 74ALVCH16823 is a 18-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. Incorporates bushold data inputs which eliminate the need for external pull-up resistors to hold unused inputs. The 74ALVCH16823 consists of two sections of nine edge-triggered flip-flops. A clock (nCP) input, an output-enable ($n\overline{OE}$) input, a master reset ($n\overline{MR}$) input and a clock-enable ($n\overline{CE}$) input are provided for each total 9-bit section.

With the clock-enable ($n\overline{CE}$) input LOW, the D-type flip-flops will store the state of their individual nDn-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH nCP transition. Taking $n\overline{CE}$ HIGH disables the clock buffer, thus latching the outputs. Taking the master reset ($n\overline{MR}$) input LOW causes all the nQn outputs to go LOW independently of the clock.

When $n\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When the $n\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $n\overline{OE}$ input does not affect the state of flip-flops.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

2 Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50 Ω transmission lines at 85°C
- All data inputs have bushold
- Complies with JEDEC standard no. 8-1A
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH16823DGG	−40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4 Functional diagram

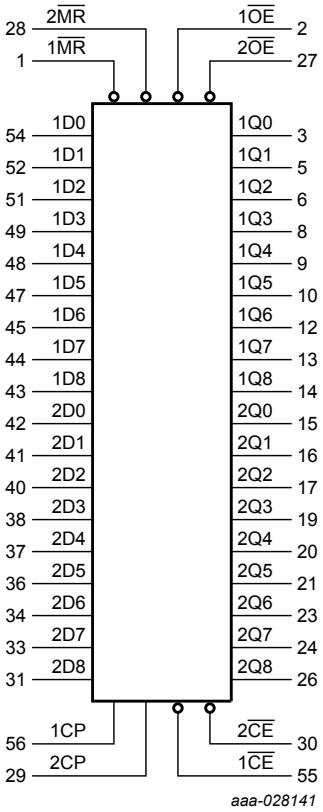


Figure 1. Logic symbol

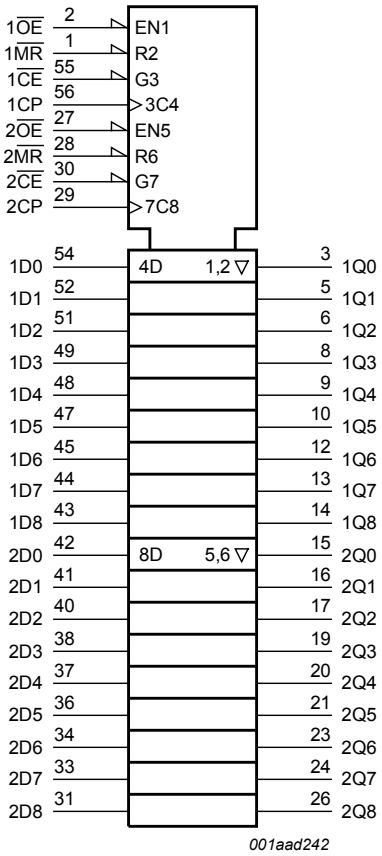


Figure 2. IEC logic symbol

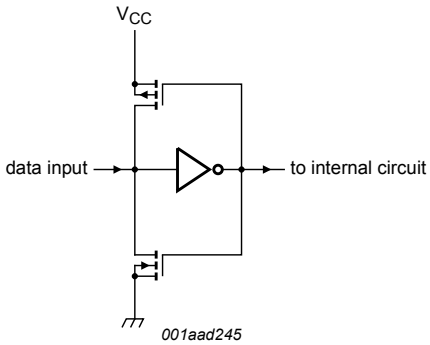


Figure 3. Bushold circuit (one data input)

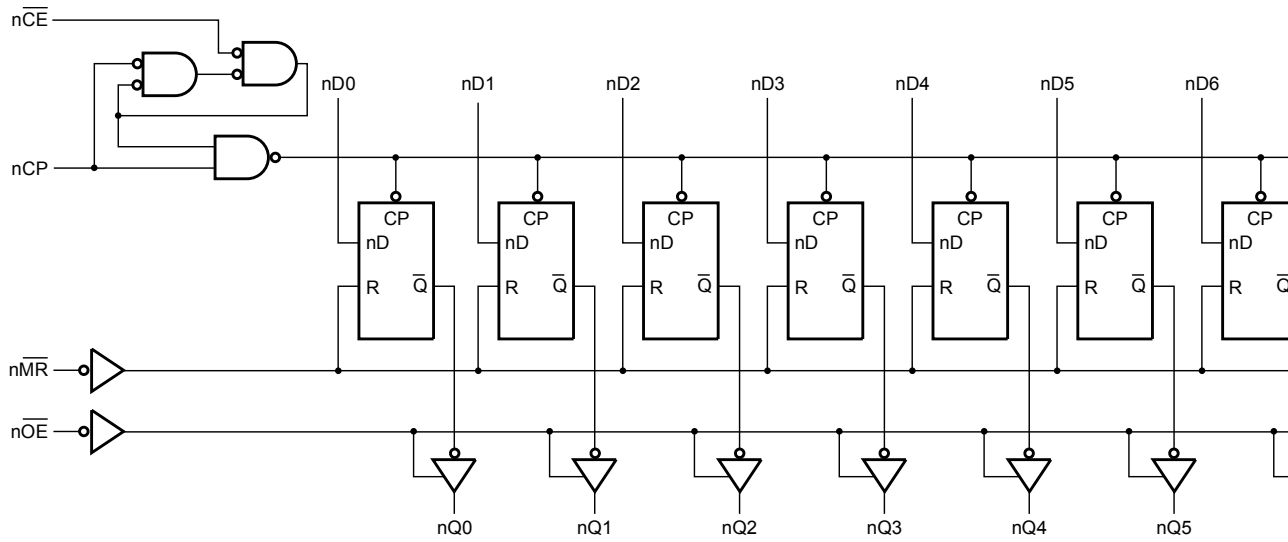


Figure 4. Logic diagram

5 Pinning information

5.1 Pinning

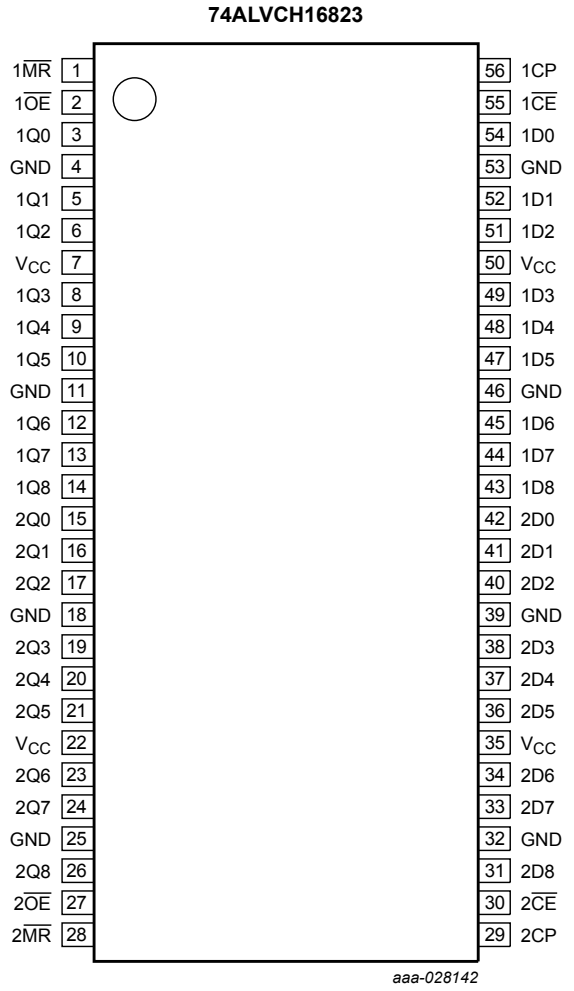


Figure 5. Pin configuration SOT364-1 (TSSOP56)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8	54, 52, 51, 49, 48, 47, 45, 44, 43	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8	3, 5, 6, 8, 9, 10, 12, 13, 14	data outputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8	42, 41, 40, 38, 37, 36, 34, 33, 31	data inputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8	15, 16, 17, 19, 20, 21, 23, 24, 26	data outputs
1$\overline{MR}$, 2$\overline{MR}$	1, 28	master reset inputs (active-LOW)
1$\overline{OE}$, 2$\overline{OE}$	2, 27	output enable inputs (active LOW)
1CP, 2CP	56, 29	clock pulse inputs (active rising edge)
1$\overline{CE}$, 2$\overline{CE}$	55, 30	clock enable inputs (active-LOW)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V_{CC}	7, 22, 35, 50	supply voltage

6 Functional description

Table 3. Function table [1]

Operating mode	Input					Output
	n$\overline{OE}$	n$\overline{MR}$	n$\overline{CE}$	nCP	nDn	nQn
clear	L	L	X	X	X	L
load and read data	L	H	L	↑	h	H
	L	H	L	↑	l	L
hold	L	H	L	L	X	NC
	L	H	H	X	X	NC
disable outputs	H	X	X	X	X	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
NC = no change;
X = don't care;
Z = high-impedance OFF-state;

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+4.6	V
V_I	input voltage	For control pins [1]	−0.5	+5.5	V
		For data inputs [1]	−0.5	V_{CC} + 0.5	V
V_O	output voltage	[1]	−0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V	−50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V	-	±50	mA
$I_{O(sink/source)}$	output sink or source current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		−100	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C [2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	2.5 V range for maximum speed performance at 30 pF output load	2.3	2.7	V
		3.3 V range for maximum speed performance at 50 pF output load	3.0	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage	for data inputs	0	V_{CC}	V
		for control inputs	0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 1.8 V	0.7V_{CC}	0.9	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 1.8 V	-	0.9	0.2V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 µA; V_{CC} = 1.8 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -6 mA; V_{CC} = 1.8 V	V_{CC} - 0.4	V_{CC} - 0.10	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.5	V_{CC} - 0.17	-	V
		I_O = -18 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.8 V to 3.6 V	-	GND	0.20	V
		I_O = 6 mA; V_{CC} = 1.8 V	-	0.09	0.30	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.20	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.40	V
		I_O = 18 mA; V_{CC} = 2.3 V	-	0.23	0.60	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	V
I_I	input leakage current	per control pin; V_{CC} = 1.8 V to 3.6 V; V_I = 5.5 V or GND	-	0.1	5	µA
		per data pin; V_{CC} = 1.8 V to 3.6 V; V_I = V_{CC} or GND	-	0.1	5	µA
I_{OZ}	OFF-state output current	V_{CC} = 1.8 V to 2.7 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	0.1	5	µA
		V_{CC} = 2.7 V to 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	0.1	10	µA
I_{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.2	40	µA
ΔI_{CC}	additional supply current	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	150	750	µA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V	45	-	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V	-45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V	-75	-175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 2.7 V	300	-	-	µA
		V_{CC} = 3.0 V	450	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 2.7 V	-300	-	-	µA
		V_{CC} = 3.6 V	-450	-	-	µA
C_I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10 Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10

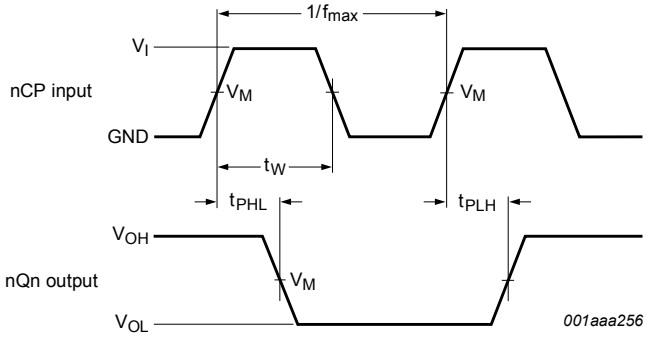
Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{pd}	propagation delay	nCP to nQn; see Figure 6 [2]				
		V_{CC} = 1.2 V	-	10.6	-	ns
		V_{CC} = 1.8 V	1.5	4.5	7.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.8	4.9	ns
		V_{CC} = 2.7 V	1.0	2.7	4.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.5	3.7	ns
		$n\overline{MR}$ to nQn; see Figure 8				
		V_{CC} = 1.2 V	-	9.9	-	ns
		V_{CC} = 1.8 V	1.5	4.6	7.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.9	5.0	ns
		V_{CC} = 2.7 V	1.0	3.1	4.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.6	4.0	ns
t_{en}	enable time	$n\overline{OE}$ to nQn; see Figure 9 [3]				
		V_{CC} = 1.2 V	-	10.4	-	ns
		V_{CC} = 1.8 V	1.5	4.4	7.7	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.8	5.3	ns
		V_{CC} = 2.7 V	1.0	3.1	5.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.5	4.3	ns

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{dis}	disable time	$n\overline{OE}$ to nQn; see Figure 9 [4]				
		V_{CC} = 1.2 V	-	6.7	-	ns
		V_{CC} = 1.8 V	1.5	3.3	5.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.2	4.1	ns
		V_{CC} = 2.7 V	1.0	3.1	4.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.8	3.9	ns
t_{su}	set-up time	nDn to nCP; see Figure 7				
		V_{CC} = 1.8 V	1.5	0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.2	0.2	-	ns
		V_{CC} = 2.7 V	1.5	0.4	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	0.2	-	ns
		$n\overline{CE}$ to nCP; see Figure 7				
		V_{CC} = 1.8 V	2.0	-0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.8	-0.2	-	ns
		V_{CC} = 2.7 V	1.9	-0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	-0.1	-	ns
t_h	hold time	nDn to nCP; see Figure 7				
		V_{CC} = 1.8 V	0.6	-0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.8	-0.1	-	ns
		V_{CC} = 2.7 V	0.6	-0.2	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.8	0.0	-	ns
		$n\overline{CE}$ to nCP; see Figure 7				
		V_{CC} = 1.8 V	0.3	0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.3	0.2	-	ns
		V_{CC} = 2.7 V	0.4	0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	0.1	-	ns
t_W	pulse width	nCP HIGH or LOW; see Figure 6				
		V_{CC} = 1.8 V	4.0	2.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	3.0	1.6	-	ns
		V_{CC} = 2.7 V	3.0	1.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	1.4	-	ns
		$n\overline{MR}$ HIGH or LOW; see Figure 8				
		V_{CC} = 1.8 V	4.0	0.8	-	ns
		V_{CC} = 2.3 V to 2.7 V	3.0	0.4	-	ns
		V_{CC} = 2.7 V	3.0	0.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	0.3	-	ns

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{rec}	recovery time	$n\overline{MR}$ to nCP; see Figure 8				
		V_{CC} = 1.8 V	0.8	0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	0.3	-	ns
		V_{CC} = 2.7 V	0.8	0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	0.2	-	ns
f_{max}	maximum frequency	nCP; see Figure 6				
		V_{CC} = 1.8 V	125	250	-	MHz
		V_{CC} = 2.3 V to 2.7 V	150	300	-	MHz
		V_{CC} = 2.7 V	150	300	-	MHz
		V_{CC} = 3.0 V to 3.6 V	200	350	-	MHz
C_{PD}	power dissipation capacitance	per latch; V_I = GND to V_{CC} [5]				
		outputs enabled	-	16	-	pF
		outputs disabled	-	10	-	pF

[1] Typical values are measured at T_{amb} = 25 °C
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_{en} is the same as t_{PZL} and t_{PZH}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

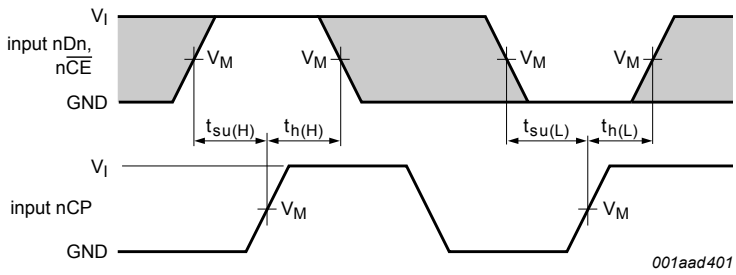
10.1 Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

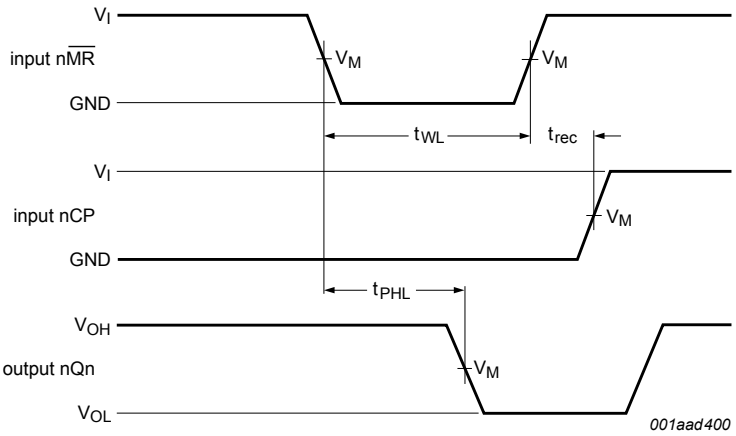
Figure 6. Propagation delay clock input (nCP) to output (nQn), clock pulse (nCP) width and maximum clock (nCP) frequency



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

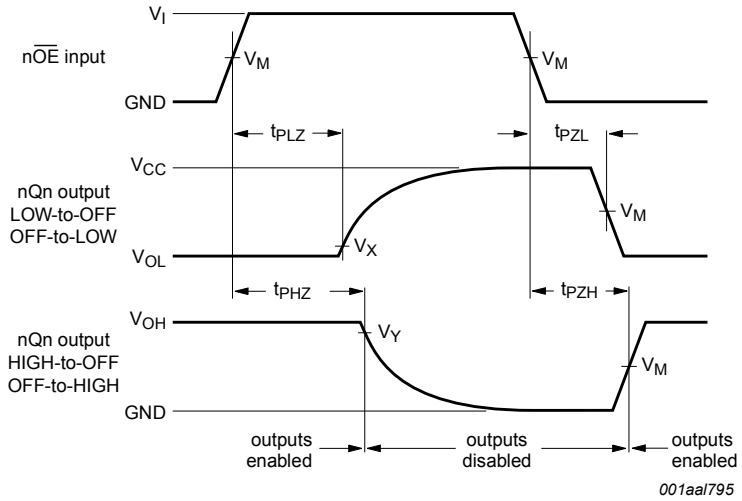
Figure 7. Data set-up and hold times for the nDn or nCE input to the nCP input



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 8. Master reset (nMR) pulse width, master reset (nMR) to output (nQn) propagation delay and master reset (nMR) to clock (nCP) recovery time



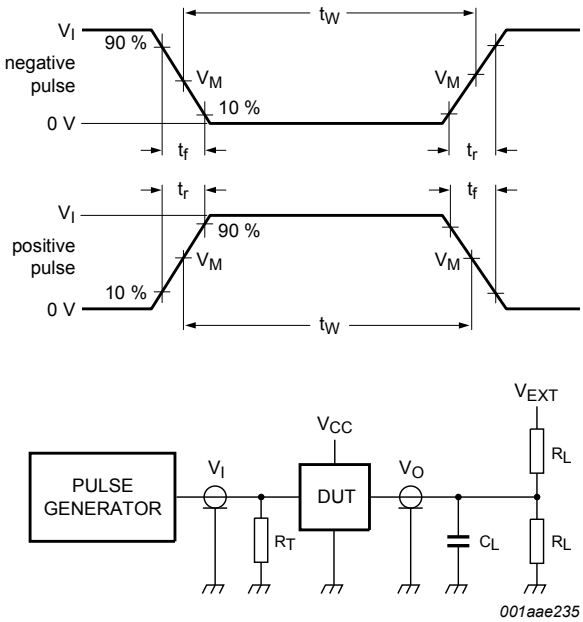
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 9. OFF-state to HIGH and LOW propagation delays and LOW and HIGH to OFF-state propagation delays

Table 8. Measurement points

V_{CC}	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
< 2.7 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
≥ 2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

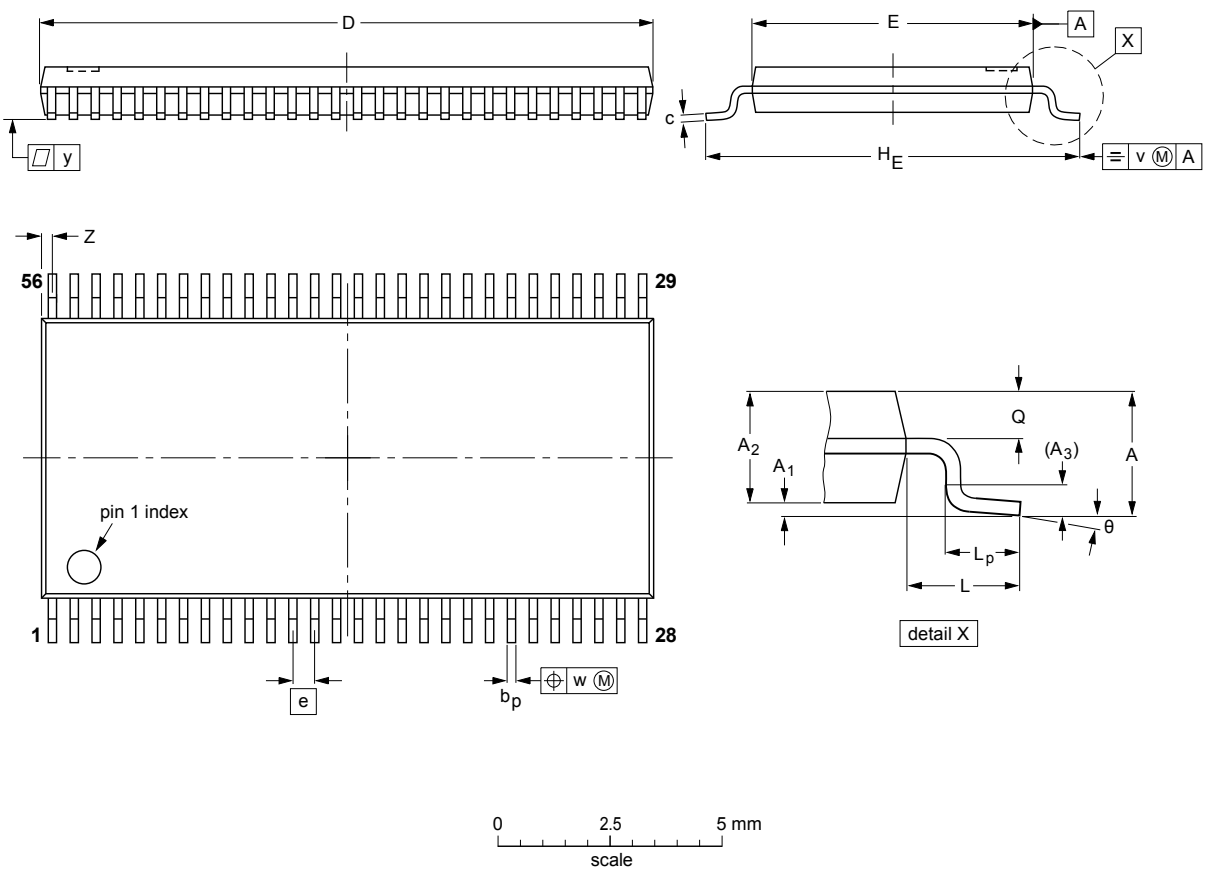
Figure 10. Test circuit for measuring switching times

Table 9. Test data

Input			Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
< 2.7 V	V_{CC}	≤ 2.0 ns	500 Ω	30 pF	GND	2 × V_{CC}	open
≥ 2.7 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V_{CC}	open

11 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Figure 11. Package outline SOT364-1 (TSSOP56)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16823 v.3	20180201	Product data sheet	-	74ALVCH16823 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74ALVCH16823DL (SOT371-1 / SSOP56) removed			
74ALVCH16823 v.2	19980729	Product specification	-	74ALVCH16823 v.1
74ALVCH16823 v.1	19980729	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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