Low-power dual 2-input NAND gate Rev. 10 — 3 July 2017

Product data sheet

#### **General description** 1

The 74AUP2G00 provides dual 2-input NAND function.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire  $V_{CC}$  range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

#### Features and benefits 2

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- · Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 5 000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1 000 V
- Low static power consumption;  $I_{CC} = 0.9 \ \mu A$  (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V<sub>CC</sub>
- I<sub>OFF</sub> circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

# nexperia

# **3** Ordering information

Table 1. Ordering	information								
Type number	Package	Package							
	Temperature Nam range		Description	Version					
74AUP2G00DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1					
74AUP2G00GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1					
74AUP2G00GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm	SOT1089					
74AUP2G00GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2					
74AUP2G00GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm	SOT1116					
74AUP2G00GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm	SOT1203					
74AUP2G00GX	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.35 mm	SOT1233					

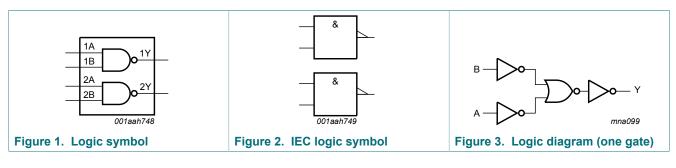
### 4 Marking

Table 2.	Marking	codes
		0000

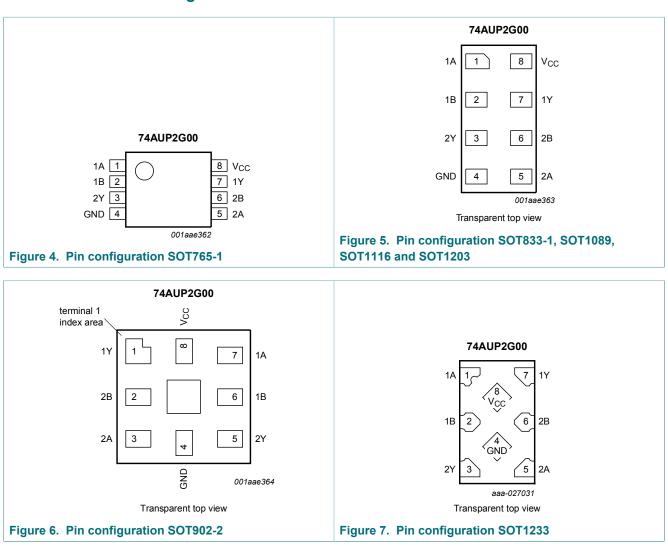
Type number	Marking code <sup>[1]</sup>
74AUP2G00DC	p00
74AUP2G00GT	p00
74AUP2G00GF	pA
74AUP2G00GM	p00
74AUP2G00GN	pA
74AUP2G00GS	pA
74AUP2G00GX	pA

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5 Functional diagram



### 6 Pinning information



### 6.1 Pinning

### 6.2 Pin description

Symbol	Pin		Description
	SOT765-1, SOT833-1, SOT1089, SOT1116, SOT1203 and SOT1233	SOT902-2	
1A, 2A	1, 5	7, 3	data input
1B, 2B	2, 6	6, 2	data input
GND	4	4	ground (0 V)
1Y, 2Y	7, 3	1, 5	data output
V <sub>CC</sub>	8	8	supply voltage

# 7 Functional description

Table 4. Function table <sup>[1]</sup>						
Input		Output				
nA	nB	nY				
L	L	Н				
L	Н	н				
Н	L	Н				
Н	Н	L				

[1] H = HIGH voltage level;

L = LOW voltage level.

### 8 Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
VI	input voltage	[1]	-0.5	+4.6	V
Vo	output voltage	Active mode and Power-down mode <sup>[1]</sup>	-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	$V_{O} = 0 V \text{ to } V_{CC}$	-	±20	mA
I <sub>CC</sub>	supply current		-	+50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C <sup>[2]</sup>	-	250	mW

The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 For VSSOP8 packages: above 110 °C the value of P<sub>tot</sub> derates linearly with 8.0 mW/K.

[2] For VSSOP8 packages: above 110 °C the value of P<sub>tot</sub> derates linearly with 8.0 mW/K. For XSON8 and XQFN8 packages: above 118 °C the value of P<sub>tot</sub> derates linearly with 7.8 mW/K. For X2SON8 package: above 118 °C the value of P<sub>tot</sub> derates linearly with 7.7 mW/K.

### 9 Recommended operating conditions

#### Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit
V <sub>CC</sub>	supply voltage		0.8	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	V <sub>CC</sub>	V
		Power-down mode; $V_{CC}$ = 0 V	0	3.6	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 0.8 V to 3.6 V	-	200	ns/V

# **10 Static characteristics**

### Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Мах	Uni
T <sub>amb</sub> = 25	°C				1	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	0.70 × V <sub>CC</sub>	-	-	V
Г <sub>атb</sub> = 25 ° / <sub>IH</sub>		V <sub>CC</sub> = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC}$ = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
V <sub>OH</sub> ł		$V_{\rm CC}$ = 2.3 V to 2.7 V	-	-	0.7	V
		$V_{CC}$ = 3.0 V to 3.6 V	-	-	0.9	V
√ <sub>ОН</sub>	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{\rm O}$ = -20 $\mu\text{A};V_{\rm CC}$ = 0.8 V to 3.6 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -1.1 mA; V <sub>CC</sub> = 1.1 V	0.75 × V <sub>CC</sub>	-	-	V
		I <sub>O</sub> = -1.7 mA; V <sub>CC</sub> = 1.4 V	1.11	-	-	V
		I <sub>O</sub> = -1.9 mA; V <sub>CC</sub> = 1.65 V	1.32	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	2.05	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.9	-	-	V
		I <sub>O</sub> = -2.7 mA; V <sub>CC</sub> = 3.0 V	2.72	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.6	-	-	V
$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$ $V_{OL} \qquad \text{LOW-level output voltage} \qquad V_{I} = V_{IH} \text{ or } V_{IL}$	$V_{I} = V_{IH} \text{ or } V_{IL}$					
		$I_{O}$ = 20 µA; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.1	V
V <sub>OH</sub> Н		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.3 × V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.31	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.31	V
		$ \frac{V_{CC} = 2.3 \ V \ to 2.7 \ V}{V_{CC} = 3.0 \ V \ to 3.6 \ V} $ $ \frac{1.6}{V_{CC} = 0.8 \ V} $ $ \frac{V_{CC} = 0.8 \ V}{V_{CC} = 0.9 \ V \ to 1.95 \ V} $ $ \frac{V_{CC} = 2.3 \ V \ to 2.7 \ V}{V_{CC} = 2.3 \ V \ to 3.6 \ V} $ $ \frac{V_{CC} = 2.3 \ V \ to 3.6 \ V}{V_{CC} = 2.3 \ V \ to 3.6 \ V} $ $ \frac{V_{CC} = 2.3 \ V \ to 3.6 \ V}{V_{CC} = 3.0 \ V \ to 3.6 \ V} $ $ \frac{V_{CC} = 2.3 \ V \ to 3.6 \ V}{V_{CC} = 3.0 \ V \ to 3.6 \ V} $ $ \frac{V_{CC} = 2.3 \ V \ to 3.6 \ V}{V_{CC} = 3.0 \ V \ to 3.6 \ V} $ $ \frac{V_{CC} = 2.3 \ V \ to 3.6 \ V}{V_{CC} = 0.8 \ V \ to 3.6 \ V} $ $ \frac{V_{CC} = 0.9 \ V \ to 3.6 \ V}{V_{CC} = 0.8 \ V \ to 3.6 \ V} $ $ \frac{V_{CC} = 0.1 \ W_{CC} = 0.8 \ V \ to 3.6 \ V}{V_{CC} = 0.1 \ V} $ $ \frac{V_{CC} = 0.1 \ W_{CC} = 0.8 \ V \ to 3.6 \ V}{V_{CC} = 0.1 \ V} $ $ \frac{V_{CC} = 0.1 \ W_{CC} = 0.8 \ V \ to 3.6 \ V}{V_{CC} = 0.1 \ V} $ $ \frac{V_{CC} = 0.1 \ W_{CC} = 0.8 \ V \ to 3.6 \ V $ $ \frac{V_{CC} = 0.1 \ W_{CC} = 0.8 \ V \ to 3.6 \ V $ $ \frac{V_{CC} = 0.1 \ W_{CC} = 0.8 \ V \ to 3.6 \ V $ $ \frac{V_{CC} = 0.1 \ W_{CC} = 0.8 \ V \ to 3.6 \ V $ $ \frac{V_{CC} = 0.8 \ V \ to 3.6 $	0.31	V		
		$I_{O}$ = 3.1 mA; $V_{CC}$ = 2.3 V	-	-	0.44	V
		$I_{\rm O}$ = 2.7 mA; $V_{\rm CC}$ = 3.0 V	-	-	0.31	V
		$I_{O}$ = 4.0 mA; $V_{CC}$ = 3.0 V	-	-	0.44	V
I	input leakage current	$V_{I}$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V	-	-	±0.1	μA
OFF	power-off leakage current	$V_{I}$ or $V_{O}$ = 0 V to 3.6 V; $V_{CC}$ = 0 V	-	-	±0.2	μA
∆I <sub>OFF</sub>	additional power-off leakage current		-	-	±0.2	μA
сс	supply current		-	-	0.5	μA
∆I <sub>CC</sub>	additional supply current	$V_{I} = V_{CC} - 0.6 V; I_{O} = 0 A;$ [1 $V_{CC} = 3.3 V;$ per pin	1 <u>]</u>	-	40	μA

### Nexperia

# 74AUP2G00

### Low-power dual 2-input NAND gate

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
CI	input capacitance	$V_{CC}$ = 0 V to 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.8	-	pF
Co	output capacitance	$V_{O}$ = GND; $V_{CC}$ = 0 V	-	1.7	-	pF
$T_{amb} = -40$	0 °C to +85 °C				1	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	0.70 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
VIL	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	0.30 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	$c_{CC} = 0 \ V$ -       1.7       -         0.70 × V <sub>CC</sub> -       -       -         p 1.95 V       0.65 × V <sub>CC</sub> -       -         p 2.7 V       1.6       -       -         p 3.6 V       2.0       -       -         p 3.6 V       2.0       -       0.30 × V_0         p 1.95 V       -       -       0.30 × V_0         p 1.95 V       -       -       0.30 × V_0         p 2.7 V       -       -       0.35 × V_0         p 3.6 V       -       -       0.7         p 3.6 V       -       -       0.7         p 3.6 V       -       -       0.7         p 3.6 V       -       -       0.9         -       -       0.7       0.35 × V_0         p 3.6 V       -       -       0.7         p 3.6 V       -       -       0.7         p 3.6 V       0.3.6 V       -       -         p 4.7 V <sub>CC</sub> = 1.1 V       1.03       -       -         nA; V <sub>CC</sub> = 3.0 V       2.55       -       -         nA; V <sub>CC</sub> = 1.1 V       -       -       0.37         nA; V <sub>CC</sub> = 1.65 V	0.9	V	
V <sub>OH</sub>	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{\rm O}$ = -20 $\mu \text{A}; V_{\rm CC}$ = 0.8 V to 3.6 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -1.1 mA; V <sub>CC</sub> = 1.1 V	$0.7 \times V_{CC}$	-	-	V
		I <sub>O</sub> = -1.7 mA; V <sub>CC</sub> = 1.4 V	1.03	-	-	V
		I <sub>O</sub> = -1.9 mA; V <sub>CC</sub> = 1.65 V	1.30	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	1.97	-	-	V
		$I_{O}$ = -3.1 mA; $V_{CC}$ = 2.3 V	1.85	-	-	V
		$I_{\rm O}$ = -2.7 mA; $V_{\rm CC}$ = 3.0 V	2.67	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.55	-       -       0.7       N         -       0.9       N         V <sub>CC</sub> - 0.1       -       -       N         0.7 × V <sub>CC</sub> -       -       N         1.03       -       -       N         1.30       -       -       N         1.85       -       -       N         2.67       -       -       N         2.55       -       -       N         -       0.1       N       N         -       -       0.1       N         -       -       0.3       N         -       -       0.33       N	V	
V <sub>OL</sub>	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{\rm O}$ = 20 µA; $V_{\rm CC}$ = 0.8 V to 3.6 V	-	-	0.1	V
VIH H VIL L VOH H VOH L		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.3 × V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.37	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	.         .         .         .         .         .         0.30 × V <sub>CC</sub> 0.35 × V <sub>CC</sub> 0.35 × V <sub>CC</sub> 0.7         0.9         .         .         .         0.35 × V <sub>CC</sub> 0.7         0.9         .	V
		$I_{O}$ = 2.3 mA; $V_{CC}$ = 2.3 V	-	× $V_{CC}$ -           × $V_{CC}$ -           .6         -           .0         -           -         0.30 × $V_{1}$ -         0.30 × $V_{1}$ -         0.30 × $V_{1}$ -         0.35 × $V_{1}$ -         0.9           -         0.9           -         0.9           -         -           -         0.9           -         -           -         0.1           -         -           -         0.1           -         -           -         0.1           -         -           -         0.3 × $V_{0}$ -         -           -         0.33           -         -           -         0.33           -         -           -         <	0.33	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.33	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.45	V
lı	input leakage current	$V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V	-	-	±0.5	μA
I <sub>OFF</sub>	power-off leakage current	$V_{I}$ or $V_{O}$ = 0 V to 3.6 V; $V_{CC}$ = 0 V	-	-	±0.5	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.6	μA
I <sub>CC</sub>	supply current	$V_1$ = GND or $V_{CC}$ ; $I_0$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.9	μA
ΔI <sub>CC</sub>	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A};$ [1] $V_{CC} = 3.3 \text{ V}; \text{ per pin}$	-	-	50	μA

74AUP2G00 Product data sheet © Nexperia B.V. 2017. All rights reserved.

### Nexperia

### Low-power dual 2-input NAND gate

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
$T_{amb} = -4$	0 °C to +125 °C		1		1	
VIH	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	0.75 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	0.70 × V <sub>CC</sub>	-	-	V
		$V_{CC}$ = 2.3 V to 2.7 V	1.6	-	-	V
		$V_{CC}$ = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	0.25 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.30 × V <sub>CC</sub>	V
V <sub>OH</sub> H		$V_{CC}$ = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{O}$ = -20 $\mu$ A; $V_{CC}$ = 0.8 V to 3.6 V	V <sub>CC</sub> - 0.11	-	-	V
		I <sub>O</sub> = -1.1 mA; V <sub>CC</sub> = 1.1 V	0.6 × V <sub>CC</sub>	-	-	V
		I <sub>O</sub> = -1.7 mA; V <sub>CC</sub> = 1.4 V	0.93	-	-	V
		I <sub>O</sub> = -1.9 mA; V <sub>CC</sub> = 1.65 V	1.17	-	-	V
		$I_{O}$ = -2.3 mA; $V_{CC}$ = 2.3 V	1.77	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.67	-	-	V
		$I_{O}$ = -2.7 mA; $V_{CC}$ = 3.0 V	2.40	-	-	V
		$I_{O}$ = -4.0 mA; $V_{CC}$ = 3.0 V	2.30	-	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{O}$ = 20 µA; $V_{CC}$ = 0.8 V to 3.6 V		-	0.11	V
VIH H VIL I VOH H VOL I VOL I I I I I I I I I I I I I I I I I I I		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.33 × V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.41	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.39	V
		$I_{O}$ = 2.3 mA; $V_{CC}$ = 2.3 V	-	-	0.36	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.50	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.50	V
I <sub>I</sub>	input leakage current	$V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V	-	-	±0.75	μA
I <sub>OFF</sub>	power-off leakage current	$V_{I}$ or $V_{O}$ = 0 V to 3.6 V; $V_{CC}$ = 0 V	-	-	±0.75	μA
Δl <sub>OFF</sub>	additional power-off leakage current	$V_1$ or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.75	μA
I <sub>CC</sub>	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	1.4	μA
∆l <sub>CC</sub>	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A};$ [1] $V_{CC} = 3.3 \text{ V}; \text{ per pin}$	-	-	75	μA

[1] One input at V\_{CC} - 0.6 V, other input at V\_{CC} or GND.

# **11** Dynamic characteristics

#### Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +125 °C			Unit
			Min	Typ <sup>[1]</sup>	Мах	Min	Max (85 °C)	Max (125 °C)	
C <sub>L</sub> = 5 pF									
t <sub>pd</sub>	propagation	nA, nB to nY; see Figure 8 <sup>[2]</sup>							
	delay	V <sub>CC</sub> = 0.8 V	-	17.5	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.5	5.3	11.0	2.1	12.2	13.5	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.0	3.8	6.8	1.8	7.8	8.6	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.6	3.1	5.3	1.4	6.2	6.9	ns
		$V_{CC}$ = 2.3 V to 2.7 V	1.3	2.5	4.0	1.1	4.7	5.2	ns
		$V_{CC}$ = 3.0 V to 3.6 V	1.0	2.2	3.6	1.0	4.2	4.7	ns
C <sub>L</sub> = 10 p	F	·							
t <sub>pd</sub>	propagationd	nA, nB to nY; see Figure 8 [2]							
	elay	V <sub>CC</sub> = 0.8 V	-	21.0	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.4	6.1	13.0	2.2	14.4	15.9	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.4	4.4	7.9	2.2	9.2	10.2	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	3.7	6.2	1.9	7.3	8.1	ns
		$V_{CC}$ = 2.3 V to 2.7 V	1.4	3.0	4.7	1.3	5.6	6.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.3	2.8	4.3	1.2	4.9	5.4	ns
C <sub>L</sub> = 15 p	F								
t <sub>pd</sub>	propagation	nA, nB to nY; see Figure 8 [2]							
	delay	V <sub>CC</sub> = 0.8 V	-	24.5	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.4	6.9	14.8	3.1	16.5	18.2	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.8	5.0	8.9	2.5	10.5	11.6	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	4.1	7.0	2.0	8.3	9.2	ns
		$V_{CC}$ = 2.3 V to 2.7 V	1.7	3.5	5.3	1.5	6.4	7.1	ns
		$V_{CC}$ = 3.0 V to 3.6 V	1.6	3.2	4.9	1.4	5.7	6.3	ns
C <sub>L</sub> = 30 p	F			1	1		1		
t <sub>pd</sub>	propagation	nA, nB to nY; see Figure 8 [2]							
	delay	V <sub>CC</sub> = 0.8 V	-	34.8	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	4.6	9.2	20.1	4.1	22.6	24.9	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	3.0	6.5	11.8	2.9	14.0	15.4	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.6	5.4	9.3	2.3	11.1	12.3	ns
		$V_{CC}$ = 2.3 V to 2.7 V	2.4	4.6	7.1	2.1	8.5	9.4	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.3	4.3	6.5	2.1	7.6	8.4	ns

74AUP2G00 Product data sheet © Nexperia B.V. 2017. All rights reserved.

### **Nexperia**

# 74AUP2G00

#### Low-power dual 2-input NAND gate

Symbol Parameter		Conditions	Ta	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +125 °C			
			Min	Typ <sup>[1]</sup>	Max	Min	Max (85 °C)	Max (125 °C)		
C <sub>L</sub> = 5 pF	, 10 pF, 15 pF	and 30 pF								
C <sub>PD</sub> power	•	$f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$	3]							
	dissipation capacitance	V <sub>CC</sub> = 0.8 V	-	2.8	-	-	-	-	pF	
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	2.9	-	-	-	-	pF	
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	3.0	-	-	-	-	pF	
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	3.0	-	-	-	-	pF	
	V <sub>CC</sub> = 2.3 V to 2.7 V	-	3.4	-	-	-	-	pF		
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	3.9	-	-	-	-	pF	

All typical values are measured at nominal  $\ensuremath{\mathsf{V}_{\text{CC}}}$ 

[1] [2] [3]

 $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ . C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in µW).

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} \times N + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o}) \text{ where:}$ 

 $f_i$  = input frequency in MHz;

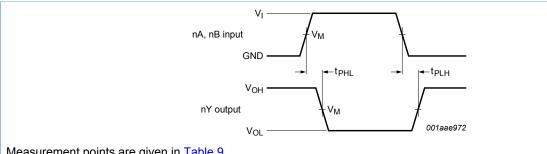
fo = output frequency in MHz;

 $C_L$  = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;  $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of outputs.

### 11.1 Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

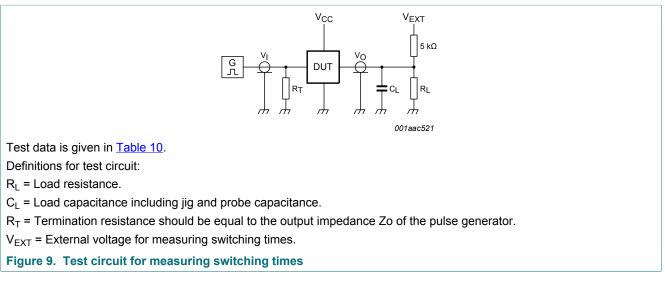
Figure 8. The data input (nA or nB) to output (nY) propagation delays

#### Table 9. Measurement points

Supply voltage	Output	Input		
V <sub>cc</sub>	V <sub>M</sub>	V <sub>M</sub>	VI	$t_r = t_f$
0.8 V to 3.6 V	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 3.0 ns

74AUP2G00 **Product data sheet**  © Nexperia B.V. 2017. All rights reserved.

#### Low-power dual 2-input NAND gate



#### Table 10. Test data

Supply voltage	Load		V <sub>EXT</sub>		
V <sub>CC</sub>	CL	R <sub>L</sub> <sup>[1]</sup>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2 × V <sub>CC</sub>

[1] For measuring enable and disable times  $R_L = 5 k\Omega$ .

For measuring propagation delays, setup and hold times and pulse width R<sub>L</sub> = 1 M $\Omega$ .

Low-power dual 2-input NAND gate

# 12 Package outline

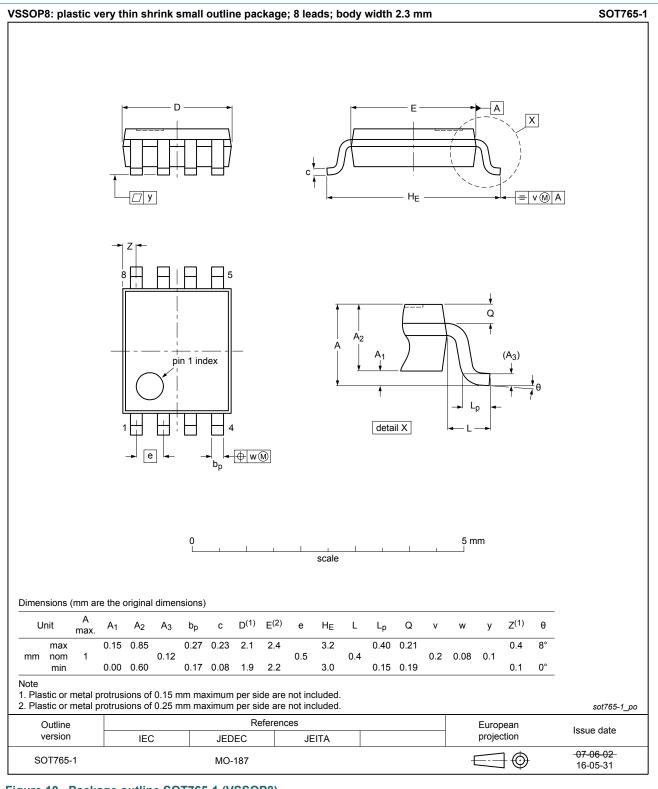


Figure 10. Package outline SOT765-1 (VSSOP8)

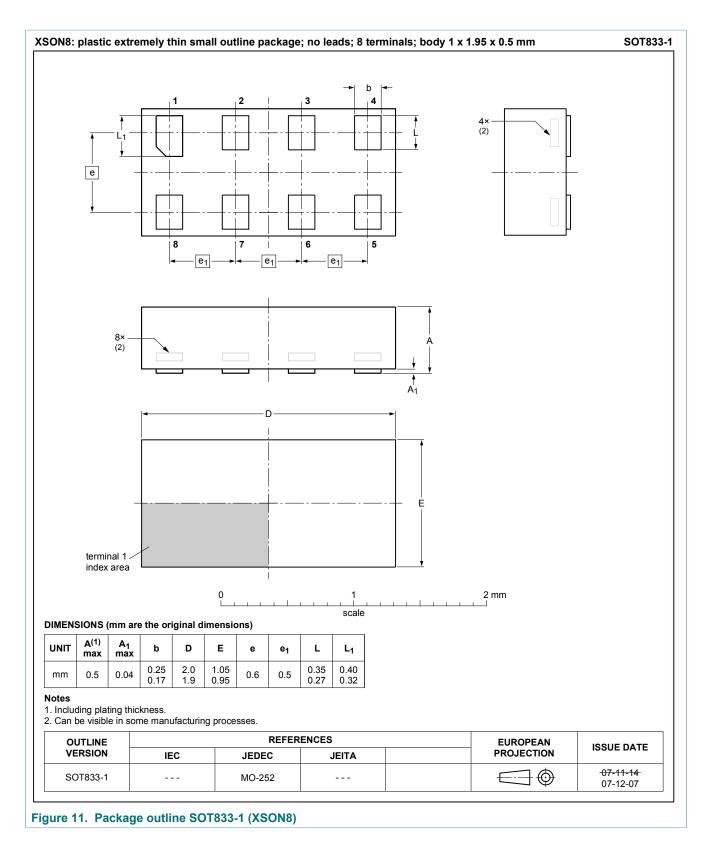
All information provided in this document is subject to legal disclaimers.

Product data sheet

74AUP2G00

© Nexperia B.V. 2017. All rights reserved.

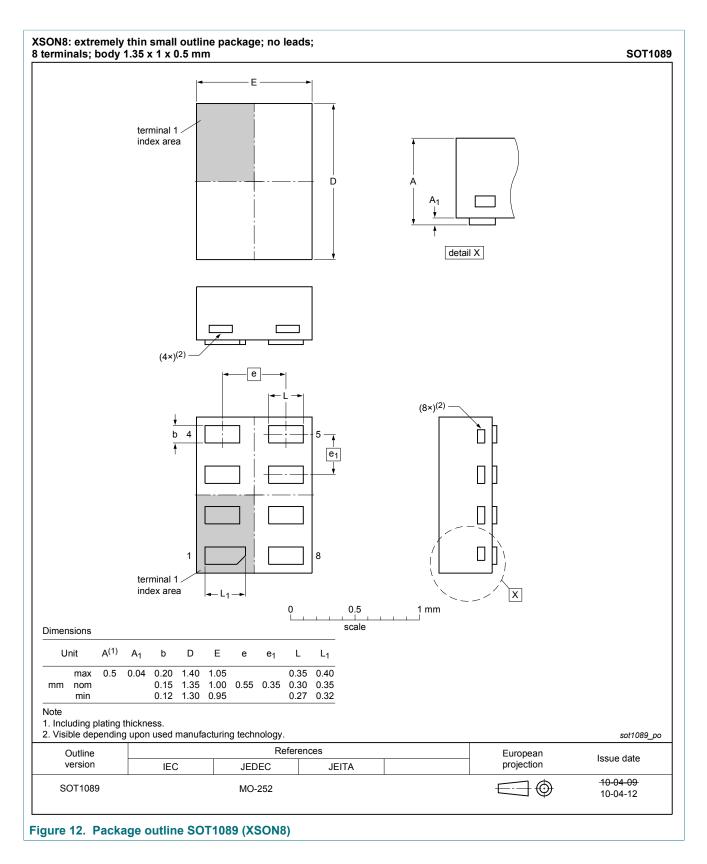
#### Low-power dual 2-input NAND gate



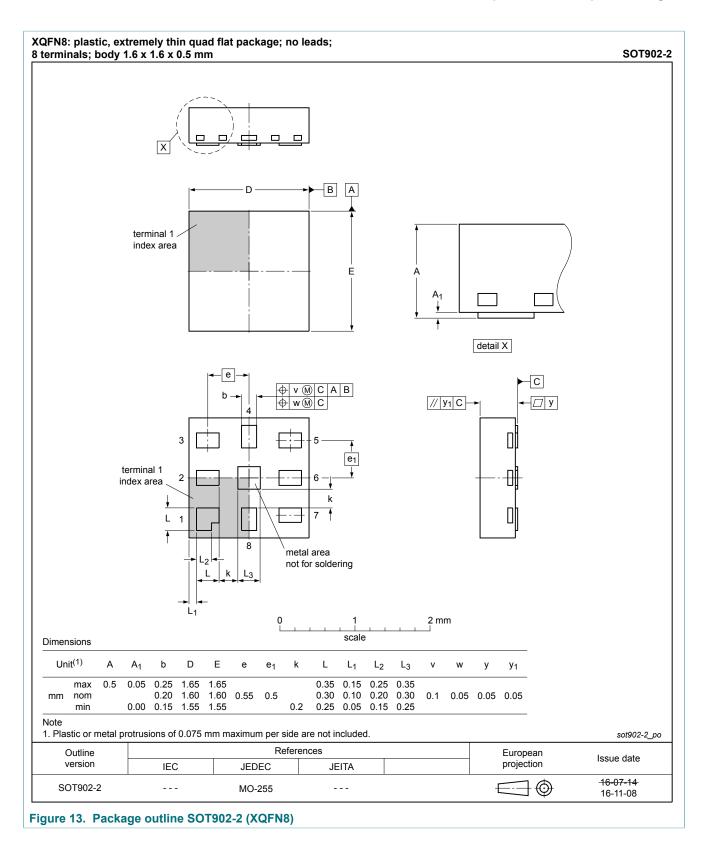
### Nexperia

# 74AUP2G00

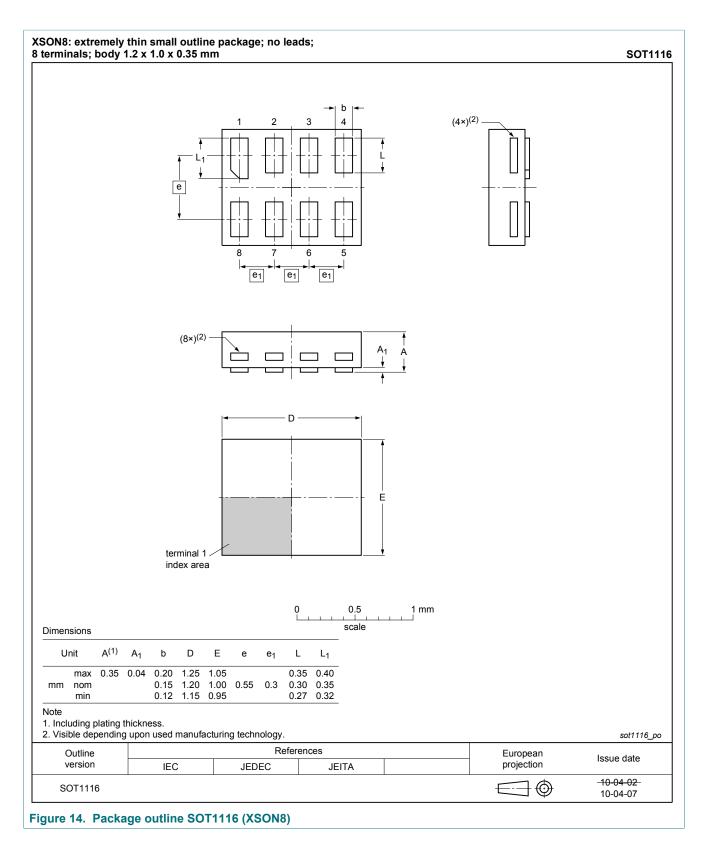
#### Low-power dual 2-input NAND gate



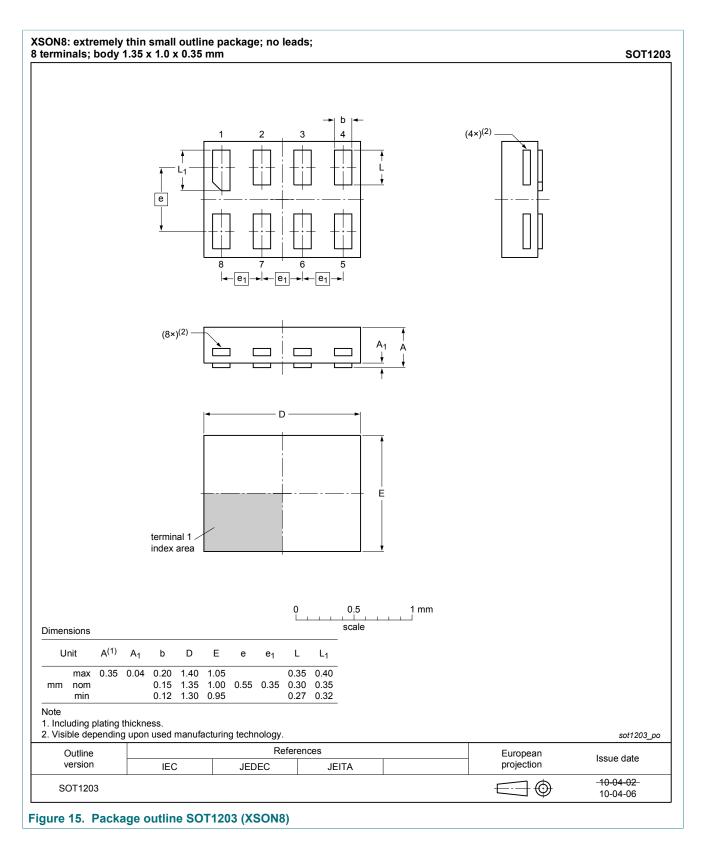
#### Low-power dual 2-input NAND gate



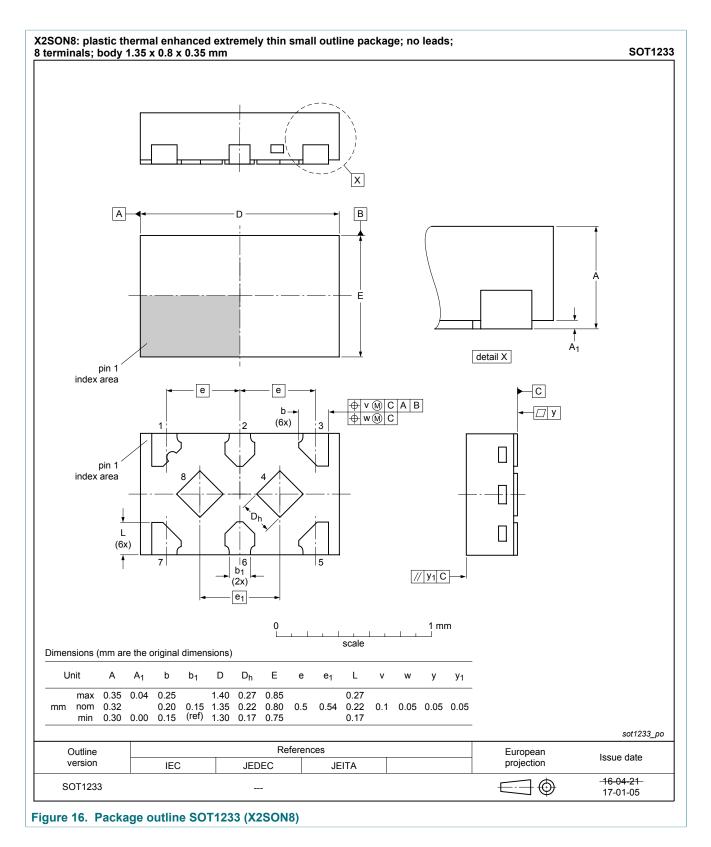
#### Low-power dual 2-input NAND gate



#### Low-power dual 2-input NAND gate



#### Low-power dual 2-input NAND gate



### **13 Abbreviations**

Table 11. Abbreviations			
Acronym	Description		
CDM	Charged Device Model		
DUT	Device Under Test		
ESD	ElectroStatic Discharge		
НВМ	Human Body Model		
MM	Machine Model		

# 14 Revision history

#### Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G00 v.10	20170703	Product data sheet	-	74AUP2G00 v.9
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Figure 7 and Figure 16 (drawings SOT1233/X2SON8) updated</li> <li>Type number 74AUP2G00GD removed.</li> </ul>			
74AUP2G00 v.9	20161028	Product data sheet	-	74AUP2G00 v.8
Modifications:	Added type number 74AUP2G00GX (SOT1233/X2SON8)			
74AUP2G00 v.8	20130205	Product data sheet	-	74AUP2G00 v.7
Modifications:	For type number 74AUP2G00GD XSON8U has changed to XSON8.			
74AUP2G00 v.7	20120608	Product data sheet	-	74AUP2G00 v.6
74AUP2G00 v.6	20111201	Product data sheet	-	74AUP2G00 v.5
74AUP2G00 v.5	20101021	Product data sheet	-	74AUP2G00 v.4
74AUP2G00 v.4	20080605	Product data sheet	-	74AUP2G00 v.3
74AUP2G00 v.3	20080403	Product data sheet	-	74AUP2G00 v.2
74AUP2G00 v.2	20070515	Product data sheet	-	74AUP2G00 v.1
74AUP2G00 v.1	20060825	Product data sheet	-	-

### 15 Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

Please consult the most recently issued document before initiating or completing a design. [1]

The term 'short data sheet' is explained in section "Definitions".

[2] [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

### **15.2 Definitions**

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 15.3 Disclaimers

Limited warranty and liability - Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia. In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia

Right to make changes - Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use - Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale - Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer

No offer to sell or license - Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

#### Low-power dual 2-input NAND gate

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer

design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

#### **15.4 Trademarks**

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

### Nexperia

# 74AUP2G00

### Low-power dual 2-input NAND gate

### Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	
5	Functional diagram	
6	Pinning information	
6.1	Pinning	
6.2	Pin description	4
7	Functional description	4
8	Limiting values	5
9	Recommended operating conditions	5
10	Static characteristics	6
11	Dynamic characteristics	9
11.1	Waveforms and test circuit	10
12	Package outline	12
13	Abbreviations	19
14	Revision history	19
15	Legal information	

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© Nexperia B.V. 2017.

All rights reserved.

For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 3 July 2017 Document identifier: 74AUP2G00

# **X-ON Electronics**

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Logic Gates category:

Click to view products by Nexperia manufacturer:

Other Similar products are found below :

74HC85N NLU1G32AMUTCG NLVHC1G08DFT1G CD4068BE NL17SG32P5T5G NL17SG86DFT2G NLV14001UBDR2G NLX1G11AMUTCG NLX1G97MUTCG 74LS38 74LVC32ADTR2G MC74HCT20ADTR2G NLV17SZ00DFT2G NLV17SZ02DFT2G NLV74HC02ADR2G 74HC32S14-13 74LS133 M38510/30402BDA 74LVC1G86Z-7 74LVC2G08RA3-7 NLV74HC08ADTR2G NLV74HC14ADR2G NLV74HC20ADR2G NLX2G86MUTCG 5962-8973601DA 74LVC2G02HD4-7 NLU1G00AMUTCG 74LVC2G32RA3-7 74LVC2G00HD4-7 NL17SG02P5T5G 74LVC2G00HK3-7 74LVC2G86HK3-7 NLX1G99DMUTWG NLV74HC1G00DFT2G NLVHC1G08DFT2G NLV7SZ57DFT2G NLV74VHC04DTR2G NLV27WZ86USG NLV27WZ00USG NLU1G86CMUTCG NLU1G08CMUTCG NL17SZ32P5T5G NL17SZ00P5T5G NL17SH02P5T5G 74AUP2G00RA3-7 NLV74HC02ADTR2G NLX1G332CMUTCG NL17SG86P5T5G NL17SZ05P5T5G NLV74VHC00DTR2G