74AVC16244

16-bit buffer/line driver; 3.6 V tolerant; 3-state

Rev. 3 — 20 February 2018 Product data sheet

1 General description

The 74AVC16244 is a 16-bit non-inverting buffer/line driver with 3-state outputs. This device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-state outputs are controlled by the output enable inputs $n\overline{OE}$. A HIGH level on input $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

The 74AVC16244 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down, input $n\overline{OE}$ should be tied to V_{CC} through a pull-up resistor (Live Insertion).

A dynamic controlled output (DCO) circuitry is implemented to support termination line drive during transient (see Figure 4).

2 Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-1A (2.7 V to 3.6 V)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple V_{CC} and GND pins to minimize noise and ground bounce
- Supports Live Insertion

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC16244DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4 Functional diagram

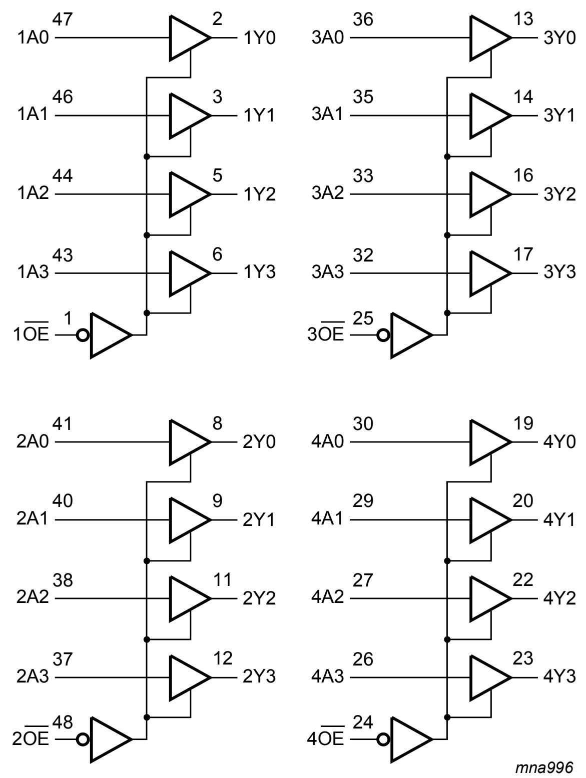


Figure 1. Logic symbol

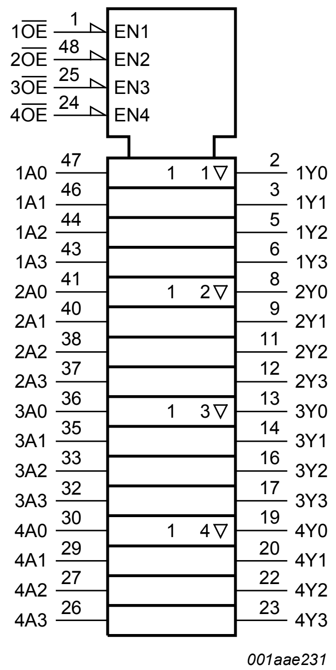


Figure 2. IEC logic symbol

5 Pinning information

5.1 Pinning

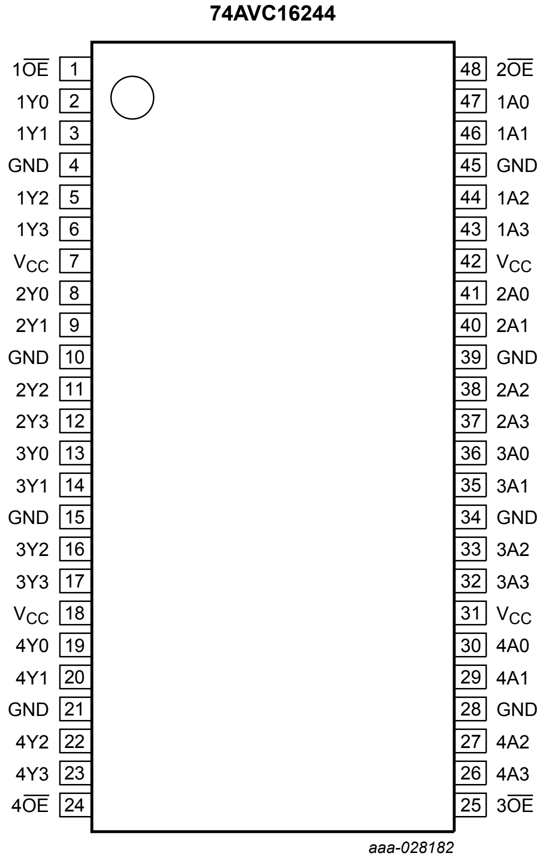


Figure 3. Pin configuration SOT362-1 (TSSOP48)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	1, 48, 25, 24	output enable inputs (active LOW)
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data inputs
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data inputs
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data inputs
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data inputs
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data outputs
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data outputs
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data outputs
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage

6 Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
V_I	input voltage	[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	output HIGH or LOW [1]	-0.5	V_{CC} + 0.5	V
		output 3-state [1]	-0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for low-voltage applications	1.2	-	3.6	V
		according to JEDEC Low Voltage Standards	1.65	-	1.95	V
			2.3	-	2.7	V
			3.0	-	3.6	V
V_I	input voltage		0	-	3.6	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	3.6	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.3 V	0	-	30	ns/V
		V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

9 Static characteristics

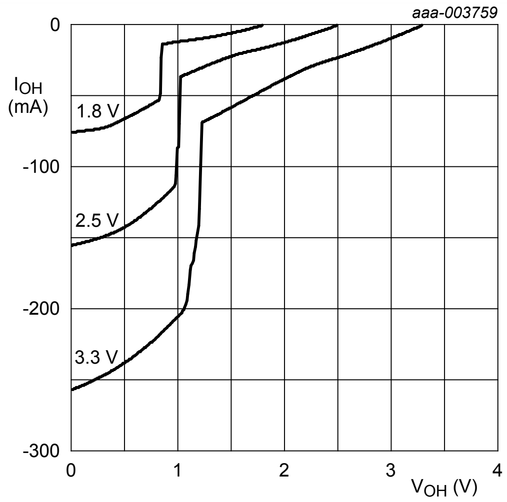
Table 6. Static characteristics

At recommended operating conditions. T_{amb} = −40 °C to +85 °C; Voltages are referenced to GND (ground = 0 V).

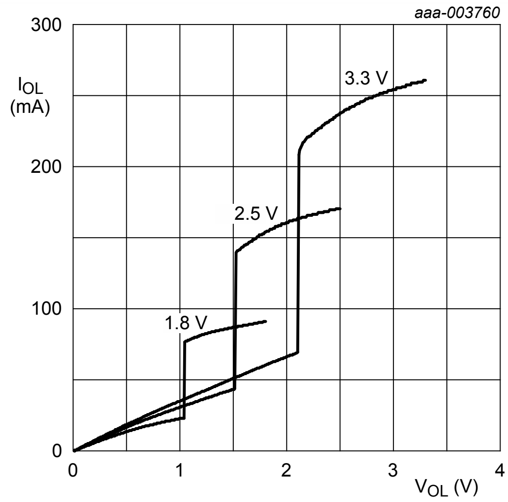
Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 x V_{CC}	0.9	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 1.65 V to 1.95 V	-	0.9	0.35 x V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; see Figure 4				
		I_O = -100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} - 0.20	V_{CC}	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	V_{CC} - 0.45	V_{CC} - 0.10	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	V_{CC} - 0.55	V_{CC} - 0.28	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	V_{CC} - 0.70	V_{CC} - 0.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; see Figure 4				
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	GND	0.20	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	0.10	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	0.26	0.55	V
		I_O = 12 mA; V_{CC} = 3.0 V	-	0.36	0.70	V
I_I	input leakage current	per input pin; V_I = V_{CC} or GND; V_{CC} = 1.65 V to 3.6 V	-	0.1	2.5	μA
I_{OFF}	power-off leakage current	V_I or V_O = 3.6 V; V_{CC} = 0.0 V	-	0.1	±10	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND				
		V_{CC} = 1.65 V to 2.7 V	-	0.1	5	μA
		V_{CC} = 3.0 V to 3.6 V	-	0.1	10	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A				
		V_{CC} = 1.65 V to 2.7 V	-	0.1	20	μA
		V_{CC} = 3.0 V to 3.6 V	-	0.2	40	μA
C_I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

9.1 Dynamic controlled output graphs



a. HIGH-level output current.



b. LOW-level output current.

Figure 4. Output current as a function of output voltage.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

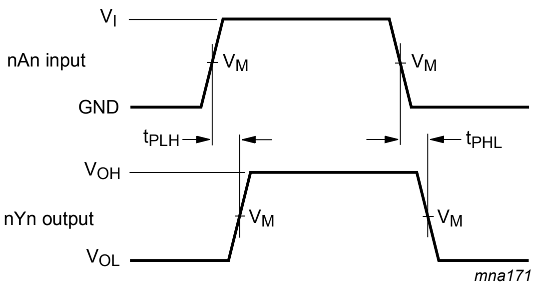
Symbol	Parameter	Conditions		-40 °C to +85 °C		Unit
			Min	Typ[1]	Max	
t_{pd}	propagation delay	nAn to nYn; see Figure 5 [2]				
		V_{CC} = 1.2 V	-	2.6	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	1.8	-	ns
		V_{CC} = 1.65 V to 1.95 V	0.7	1.7	3.1	ns
		V_{CC} = 2.3 V to 2.7 V	0.6	1.3	1.9	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	1.1	1.7	ns
t_{en}	enable time	$n\overline{OE}$ to nYn; see Figure 6 [2]				
		V_{CC} = 1.2 V	-	5.2	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	3.3	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.3	2.7	5.5	ns
		V_{CC} = 2.3 V to 2.7 V	0.9	1.9	4.3	ns
		V_{CC} = 3.0 V to 3.6 V	0.7	1.7	3.5	ns
t_{dis}	disable time	$n\overline{OE}$ to nYn; see Figure 6 [2]				
		V_{CC} = 1.2 V	-	5.7	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	4.3	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	3.2	6.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	1.9	4.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	1.8	3.5	ns
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC} [3]				
		outputs enabled	-	34	-	pF
		outputs disabled	-	1	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

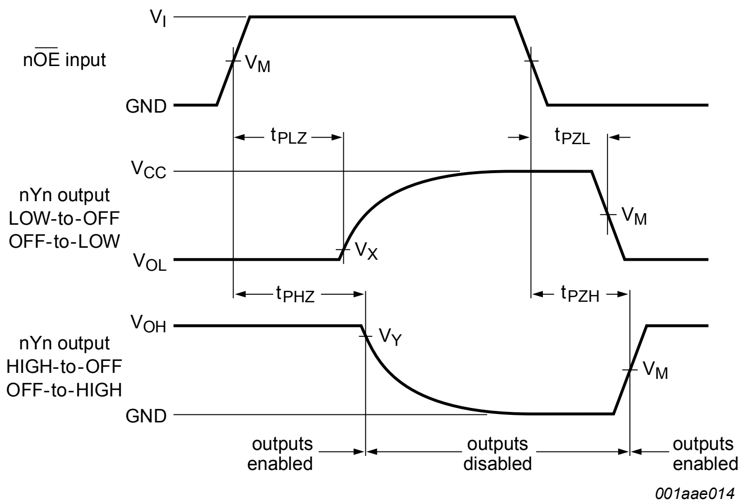
10.1 Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Inputs nAn to output nYn propagation delays



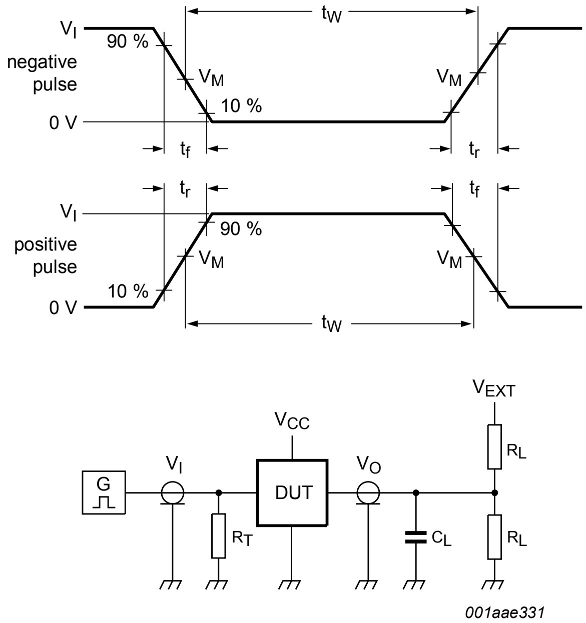
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
≤2.3 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

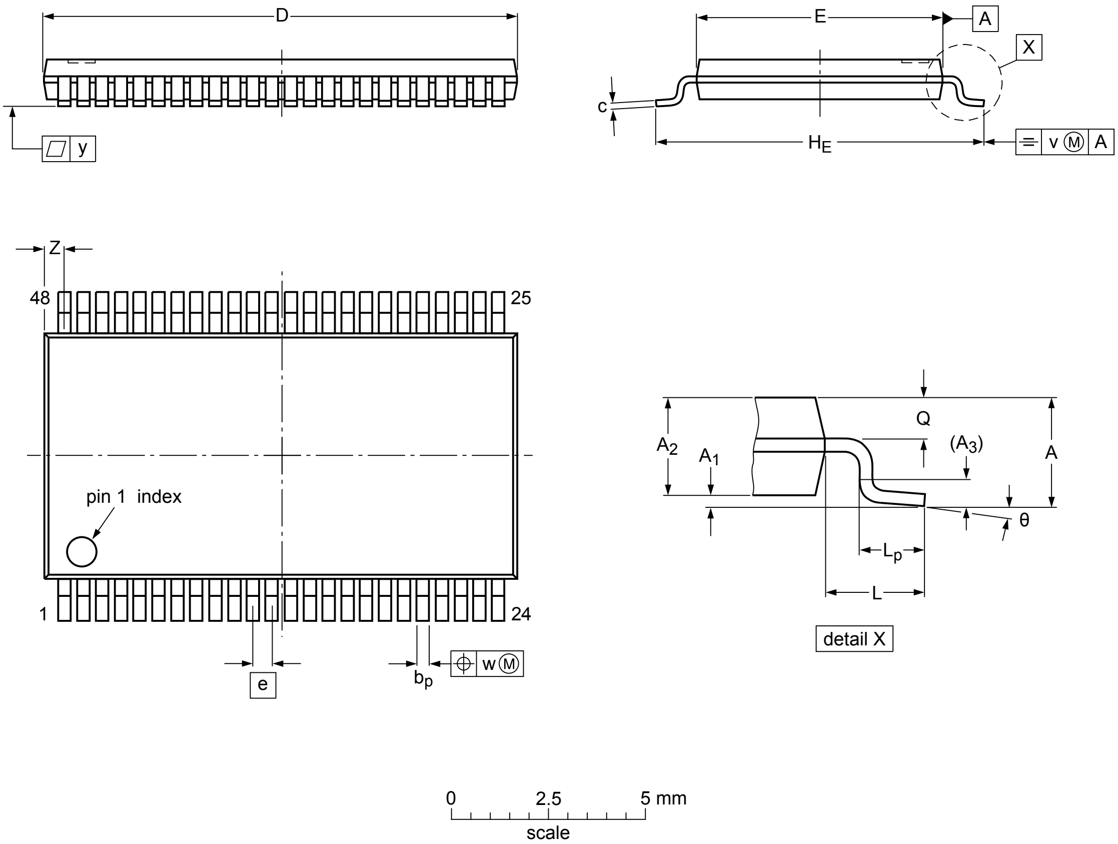
Figure 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
≤2.3 V	V_{CC}	≤ 2.0 ns	30 pF	1000 Ω	open	2 x V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 x V_{CC}	GND
3.0 V to 3.6 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 x V_{CC}	GND

11 Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~03-02-19~~ 13-08-05

Figure 8. Package outline SOT362-1 (TSSOP48)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DCO	Dynamic Controlled Output
DUT	Device Under Test

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC16244 v.3	20180220	Product data sheet	-	74AVC16244 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74AVC16244 v.2	19991115	Product specification	-	74AVC16244 v.1
74AVC16244 v.1	19981211	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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Contents

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