

74AXP1G10

Low-power 3-input NAND gate

Rev. 1 — 20 October 2015

Product data sheet

1. General description

The 74AXP1G10 is a single 3-input NAND gate.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.7 V to 2.75 V. It is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.7 V to 2.75 V
- Low input capacitance; $C_I = 0.5$ pF (typical)
- Low output capacitance; $C_O = 1.0$ pF (typical)
- Low dynamic power consumption; $C_{PD} = 2.5$ pF at $V_{CC} = 1.2$ V (typical)
- Low static power consumption; $I_{CC} = 0.6$ μ A (85 °C maximum)
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-12A.01 (1.1 V to 1.3 V)
 - ◆ JESD8-11A.01 (1.4 V to 1.6 V)
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A.01 (2.3 V to 2.7 V)
- ESD protection:
 - ◆ HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 2.75 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AXP1G10GM	-40 °C to +85 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AXP1G10GN	-40 °C to +85 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74AXP1G10GS	-40 °C to +85 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74AXP1G10GM	RM
74AXP1G10GN	RM
74AXP1G10GS	RM

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

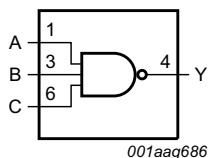


Fig 1. Logic symbol

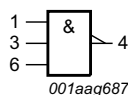


Fig 2. IEC logic symbol

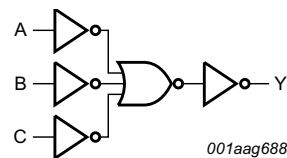
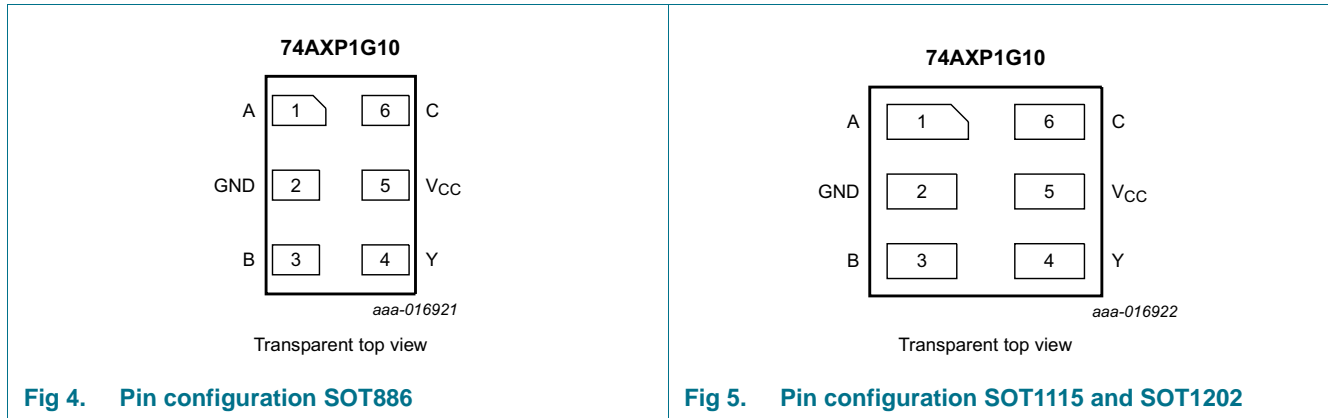


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
A	1	data input
GND	2	ground (0 V)
B	3	data input
Y	4	data output
V _{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table^[1]

Input			Output
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+3.3	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		-0.5	+3.3	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage		-0.5	+3.3	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.7	2.75	V
V_I	input voltage		0	2.75	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	2.75	V
T_{amb}	ambient temperature		-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.7$ V to 2.75 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions, unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$				Unit	
			Min	Typ 25 °C	Max 25 °C	Max 85 °C		
V_{IH}	HIGH-level input voltage	$V_{CC} = 0.75\text{ V to }0.85\text{ V}$	$0.75 \times V_{CC}$	-	-	-	V	
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	-	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.6	-	-	-	V	
V_{IL}	LOW-level input voltage	$V_{CC} = 0.75\text{ V to }0.85\text{ V}$	-	-	$0.25 \times V_{CC}$	$0.25 \times V_{CC}$	V	
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	$0.35 \times V_{CC}$	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	0.7	V	
V_{OH}	HIGH-level output voltage	$I_O = -20\text{ }\mu\text{A}; V_{CC} = 0.7\text{ V}$	-	0.69	-	-	V	
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 0.75\text{ V}$	0.65	-	-	-	V	
		$I_O = -2\text{ mA}; V_{CC} = 1.1\text{ V}$	0.825	-	-	-	V	
		$I_O = -3\text{ mA}; V_{CC} = 1.4\text{ V}$	1.05	-	-	-	V	
		$I_O = -4.5\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	-	-	-	V	
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.7	-	-	-	V	
V_{OL}	LOW-level output voltage	$I_O = 20\text{ }\mu\text{A}; V_{CC} = 0.7\text{ V}$	-	0.01	-	-	V	
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 0.75\text{ V}$	-	-	0.1	0.1	V	
		$I_O = 2\text{ mA}; V_{CC} = 1.1\text{ V}$	-	-	0.275	0.275	V	
		$I_O = 3\text{ mA}; V_{CC} = 1.4\text{ V}$	-	-	0.35	0.35	V	
		$I_O = 4.5\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.45	0.45	V	
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.7	0.7	V	
I_I	input leakage current	$V_I = 0\text{ V to }2.75\text{ V};$ $V_{CC} = 0\text{ V to }2.75\text{ V}$	[1]	-	0.001	± 0.1	± 0.5	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 0\text{ V to }2.75\text{ V};$ $V_{CC} = 0\text{ V}$	[1]	-	0.01	± 0.1	± 0.5	μA
ΔI_{OFF}	additional power-off leakage current	V_I or $V_O = 0\text{ V or }2.75\text{ V};$ $V_{CC} = 0\text{ V to }0.1\text{ V}$	[1]	-	0.02	± 0.1	± 0.5	μA
I_{CC}	supply current	$V_I = 0\text{ V or }V_{CC}; I_O = 0\text{ A}$	[1]	-	0.01	0.3	0.6	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.5\text{ V}; I_O = 0\text{ A};$ $V_{CC} = 2.5\text{ V}$	-	-	2	100	150	μA

[1] Typical values are measured at $V_{CC} = 1.2\text{ V}$.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 12](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	A, B, C to Y; see Figure 6 ^{[2][3]}						
		V _{CC} = 0.75 V to 0.85 V	3	12	51	1	116	ns
		V _{CC} = 1.1 V to 1.3 V	1.7	4.5	8.4	1.6	8.7	ns
		V _{CC} = 1.4 V to 1.6 V	1.3	3.2	5.5	1.2	5.9	ns
		V _{CC} = 1.65 V to 1.95 V	1.1	2.6	4.5	1.0	4.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.9	2.0	3.2	0.8	3.5	ns
t _t	transition time	V _{CC} = 2.7 V; see Figure 6 ^[4]	-	-	-	1.0	-	ns
C _I	input capacitance	V _I = 0 V or V _{CC} ; V _{CC} = 0 V to 2.75 V	-	0.5	-	-	-	pF
C _O	output capacitance	V _O = 0 V; V _{CC} = 0 V	-	1.0	-	-	-	pF
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = 0 V to V _{CC} ^[5]						
		V _{CC} = 0.75 V to 0.85 V	-	2.4	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.5	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	2.5	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	2.6	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	2.8	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] For additional propagation delay values at different load capacitances, see [Figure 7](#) to [Figure 11](#).

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + C_L \times V_{CC}^2 \times f_o$ where:

f_i = input frequency in MHz;

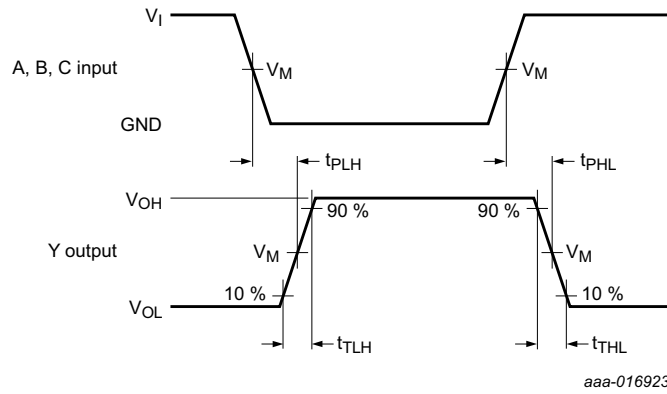
f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching.

12. Waveforms

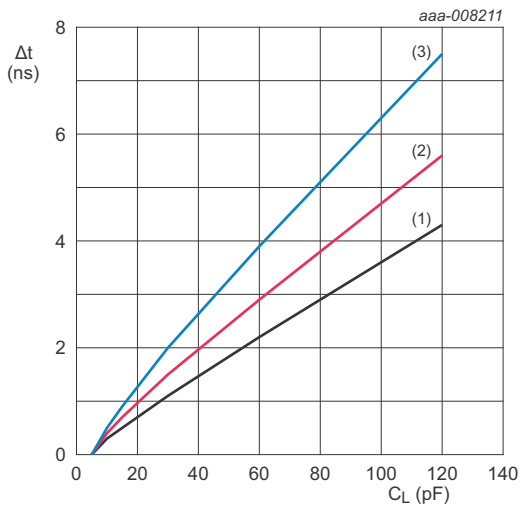


Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The data input (A, B, C) to output (Y) propagation delays and output transition times

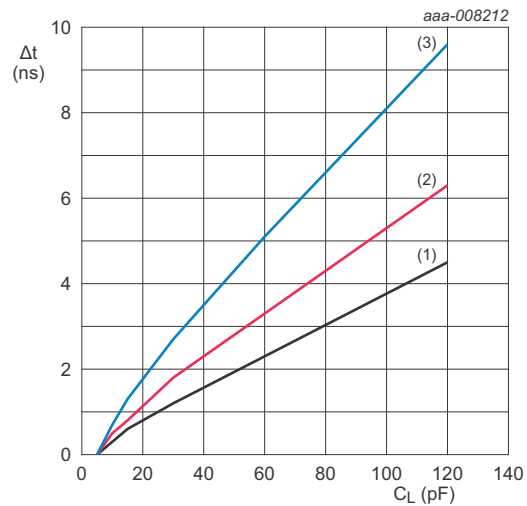
Table 9. Measurement points

Supply voltage	Input			Output
V_{CC}	V_M	V_I	$t_r = t_f$	V_M
0.75 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns	$0.5 \times V_{CC}$



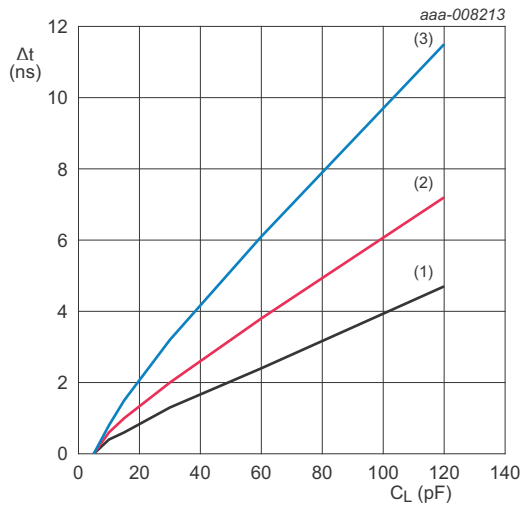
$T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$ unless otherwise specified.
 (1) Minimum: $V_{CC} = 2.7$ V
 (2) Typical: $T_{amb} = 25\text{ °C}$; $V_{CC} = 2.5$ V
 (3) Maximum: $V_{CC} = 2.3$ V

Fig 7. Additional t_{pd} versus load capacitance



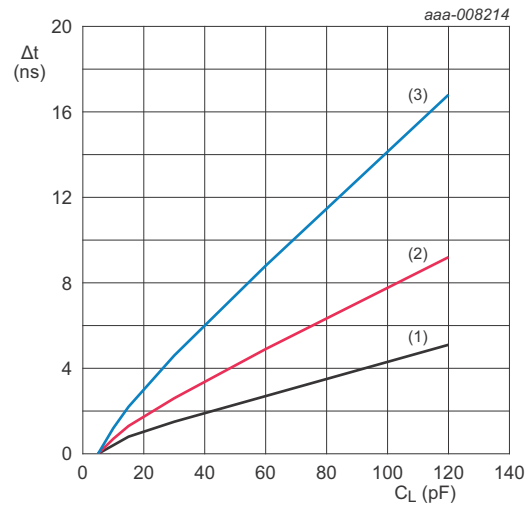
$T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$ unless otherwise specified.
 (1) Minimum: $V_{CC} = 1.95$ V
 (2) Typical: $T_{amb} = 25\text{ °C}$; $V_{CC} = 1.8$ V
 (3) Maximum: $V_{CC} = 1.65$ V

Fig 8. Additional t_{pd} versus load capacitance



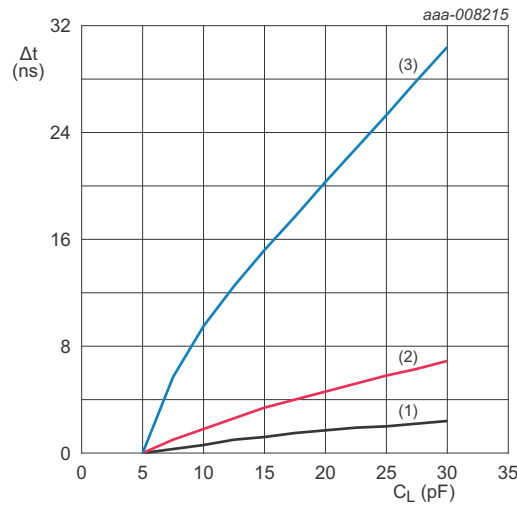
- $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.
- (1) Minimum: $V_{CC} = 1.6\text{ V}$
 - (2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 1.5\text{ V}$
 - (3) Maximum: $V_{CC} = 1.4\text{ V}$

Fig 9. Additional t_{pd} versus load capacitance



- $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.
- (1) Minimum: $V_{CC} = 1.3\text{ V}$
 - (2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 1.2\text{ V}$
 - (3) Maximum: $V_{CC} = 1.1\text{ V}$

Fig 10. Additional t_{pd} versus load capacitance



- $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.
- (1) Minimum: $V_{CC} = 0.85\text{ V}$
 - (2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 0.8\text{ V}$
 - (3) Maximum: $V_{CC} = 0.75\text{ V}$

Fig 11. Additional t_{pd} versus load capacitance



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 12. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.75 V to 2.7 V	5 pF	10 k Ω	0 V	0 V	$2 \times V_{CC}$

13. Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

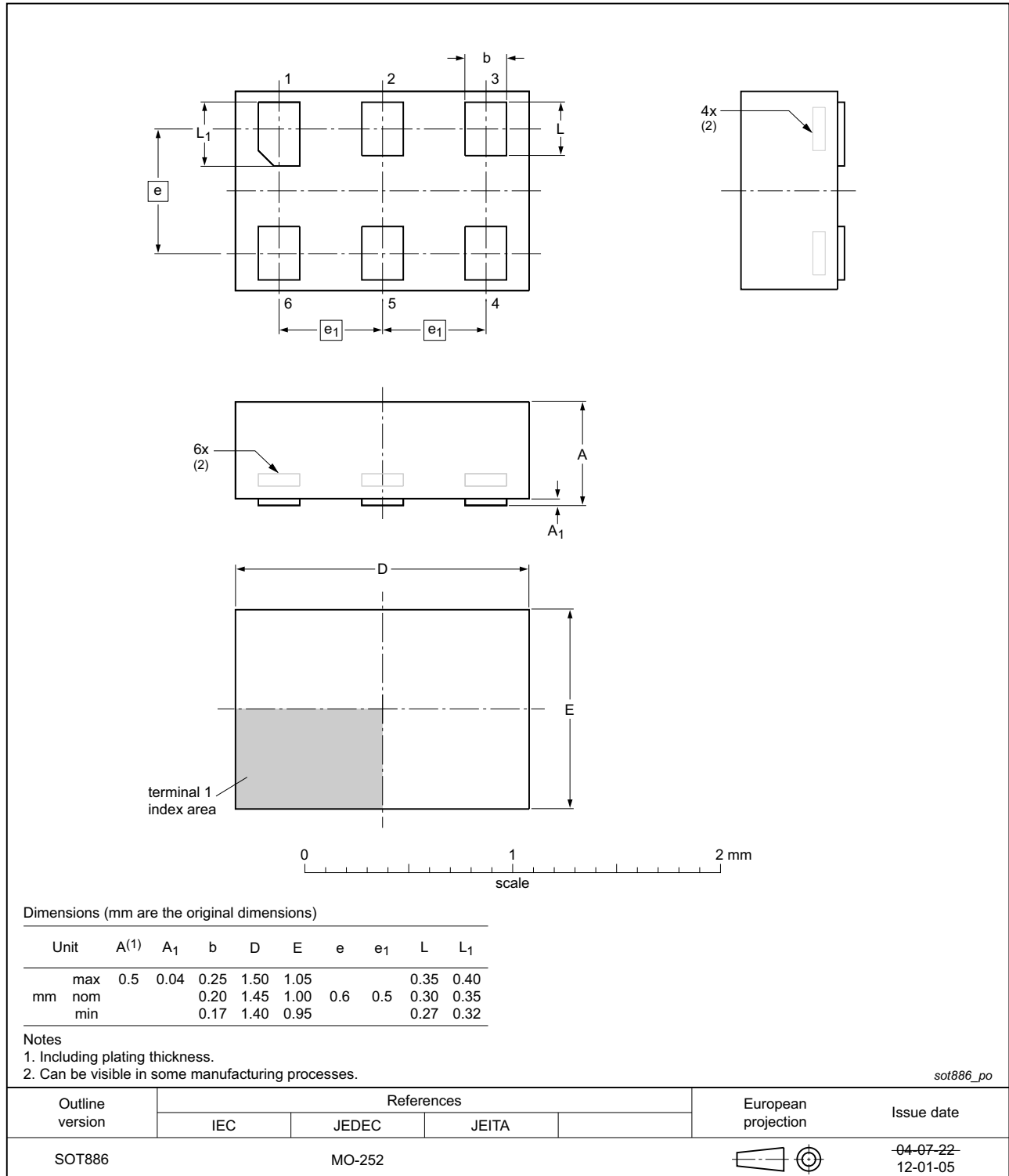


Fig 13. Package outline SOT886 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm**

SOT1115



Fig 14. Package outline SOT1115 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm**

SOT1202



Fig 15. Package outline SOT1202 (XSON6)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AXP1G10 v.1	20151020	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[NLX1G11AMUTCG](#) [NLX1G97MUTCG](#) [74LS38](#) [74LVC32ADTR2G](#) [MC74HCT20ADTR2G](#) [NLV17SZ00DFT2G](#) [NLV17SZ02DFT2G](#)
[NLV74HC02ADR2G](#) [74HC32S14-13](#) [74LS133](#) [M38510/30402BDA](#) [74LVC1G86Z-7](#) [74LVC2G08RA3-7](#) [NLV74HC08ADTR2G](#)
[NLV74HC14ADR2G](#) [NLV74HC20ADR2G](#) [NLX2G86MUTCG](#) [5962-8973601DA](#) [74LVC2G02HD4-7](#) [NLU1G00AMUTCG](#)
[74LVC2G32RA3-7](#) [74LVC2G00HD4-7](#) [NL17SG02P5T5G](#) [74LVC2G00HK3-7](#) [74LVC2G86HK3-7](#) [NLX1G99DMUTWG](#)
[NLVVHC1G00DFT2G](#) [NLVHC1G08DFT2G](#) [NLV7SZ57DFT2G](#) [NLV74VHC04DTR2G](#) [NLV27WZ86USG](#) [NLV27WZ00USG](#)
[NLU1G86CMUTCG](#) [NLU1G08CMUTCG](#) [NL17SZ32P5T5G](#) [NL17SZ00P5T5G](#) [NL17SH02P5T5G](#) [74AUP2G00RA3-7](#)
[NLV74HC02ADTR2G](#) [NLX1G332CMUTCG](#) [NL17SG86P5T5G](#) [NL17SZ05P5T5G](#) [NLV74VHC00DTR2G](#)