Low-power 2-input EXCLUSIVE-OR gate Rev. 1 — 13 November 2015

Product data sheet

General description 1.

The 74AXP1G86 is a single 2-input EXCLUSIVE-OR gate.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.7 V to 2.75 V. It is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

Features and benefits 2.

- Wide supply voltage range from 0.7 V to 2.75 V
- Low input capacitance; C_I = 0.5 pF (typical)
- Low output capacitance; C_O = 1.0 pF (typical)
- Low dynamic power consumption; C_{PD} = 2.6 pF at V_{CC} = 1.2 V (typical)
- Low static power consumption; I_{CC} = 0.6 μA (85 °C maximum)
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-12A.01 (1.1 V to 1.3 V)
 - ◆ JESD8-11A.01 (1.4 V to 1.6 V)
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A.01 (2.3 V to 2.7 V)
- ESD protection:
 - ♦ HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - CDM JESD22-C101E exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 2.75 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C



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3. Ordering information

Table 1. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
74AXP1G86GM	–40 °C to +85 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1.45 \times 0.5 mm	SOT886				
74AXP1G86GN	–40 °C to +85 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115				
74AXP1G86GS	–40 °C to +85 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $1.0 \times 1.0 \times 0.35$ mm	SOT1202				
74AXP1G86GX	-40 °C to +85 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body $0.8 \times 0.8 \times 0.35$ mm	SOT1226				

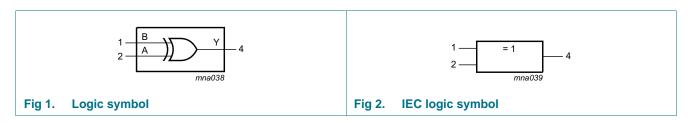
4. Marking

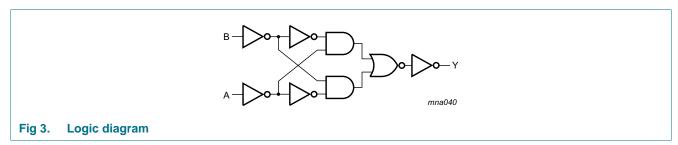
Table 2. Marking

Type number	Marking code ^[1]
74AXP1G86GM	rH
74AXP1G86GN	rH
74AXP1G86GS	rH
74AXP1G86GX	rH

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

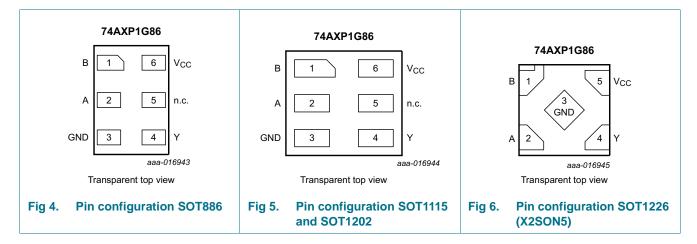
5. Functional diagram





6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	XSON6	X2SON5	
В	1	1	data input
А	2	2	data input
GND	3	3	ground (0 V)
Υ	4	4	data output
n.c.	5	-	not connected
V _{CC}	6	5	supply voltage

7. Functional description

Table 4. Function table[1]

Input	Output	
A B Y		Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

[1] H = HIGH voltage level; L = LOW voltage level.

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+3.3	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage		[1] -0.5	+3.3	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
Vo	output voltage		[1] -0.5	+3.3	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±20	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$	-	250	mW

^[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		0.7	2.75	V
VI	input voltage		0	2.75	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	2.75	V
T _{amb}	ambient temperature		-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 0.7 V to 2.75 V	0	200	ns/V

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions, unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$				Unit
				Min	Typ 25 °C	Max 25 °C	Max 85 °C	
V_{IH}	HIGH-level input	V _{CC} = 0.75 V to 0.85 V		$0.75 \times V_{CC}$	-	-	-	V
	voltage	V _{CC} = 1.1 V to 1.95 V		$0.65 \times V_{CC}$	-	-	-	V
		V _{CC} = 2.3 V to 2.7 V		1.6	-	-	-	V
V_{IL}	LOW-level input	V _{CC} = 0.75 V to 0.85 V		-	-	$0.25 \times V_{CC}$	$0.25 \times V_{CC}$	V
	voltage	V _{CC} = 1.1 V to 1.95 V		-	-	$0.35 \times V_{CC}$	$0.35 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7 V		-	-	0.7	0.7	V
V_{OH}	HIGH-level	$I_O = -20 \mu A; V_{CC} = 0.7 V$		-	0.69	-	-	V
	output voltage	$I_O = -100 \mu A; V_{CC} = 0.75 V$		0.65	-	-	-	V
		$I_O = -2 \text{ mA}; V_{CC} = 1.1 \text{ V}$		0.825	-	-	-	V
		$I_O = -3 \text{ mA}; V_{CC} = 1.4 \text{ V}$		1.05	-	-	-	V
		$I_O = -4.5 \text{ mA}; V_{CC} = 1.65 \text{ V}$		1.2	-	-	-	V
		$I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$		1.7	-	-	-	V
V_{OL}	LOW-level	$I_O = 20 \mu A; V_{CC} = 0.7 V$		-	0.01	-	-	V
	output voltage	$I_O = 100 \mu A; V_{CC} = 0.75 V$		-	-	0.1	0.1	V
		$I_O = 2 \text{ mA}; V_{CC} = 1.1 \text{ V}$		-	-	0.275	0.275	V
		$I_O = 3 \text{ mA}; V_{CC} = 1.4 \text{ V}$		-	-	0.35	0.35	V
		$I_O = 4.5 \text{ mA}; V_{CC} = 1.65 \text{ V}$		-	-	0.45	0.45	V
		$I_0 = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$		-	-	0.7	0.7	V
l _l	input leakage current	V _I = 0 V to 2.75 V; V _{CC} = 0 V to 2.75 V	[1]	-	0.001	±0.1	±0.5	μА
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 0$ V to 2.75 V; $V_{CC} = 0$ V	[1]	-	0.01	±0.1	±0.5	μΑ
ΔI_{OFF}	additional power-off leakage current	V_{I} or $V_{O} = 0$ V or 2.75 V; $V_{CC} = 0$ V to 0.1 V	[1]	-	0.02	±0.1	±0.5	μА
I _{CC}	supply current	$V_I = 0 \text{ V or } V_{CC}; I_O = 0 \text{ A}$	<u>[1]</u>	-	0.01	0.3	0.6	μΑ
Δl _{CC}	additional supply current	$V_I = V_{CC} - 0.5 \text{ V}; I_O = 0 \text{ A};$ $V_{CC} = 2.5 \text{ V}$		-	2	100	150	μΑ

^[1] Typical values are measured at V_{CC} = 1.2 V.

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11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 13.

Symbol	Parameter	neter Conditions		amb = 25	°C	$T_{amb} = -40$ °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation	A, B to Y; see Figure 7						
	delay	V _{CC} = 0.75 V to 0.85 V	3	15	72	2	164	ns
		V _{CC} = 1.1 V to 1.3 V	1.7	5.2	10.8	1.7	11.3	ns
		V _{CC} = 1.4 V to 1.6 V	1.3	3.7	6.8	1.3	7.4	ns
		V _{CC} = 1.65 V to 1.95 V	1.1	3.0	5.4	1.1	6.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.9	2.3	3.8	0.8	4.3	ns
t _t	transition time	$V_{CC} = 2.7 \text{ V}$; see <u>Figure 7</u> [4]	-	-	-	1.0	-	ns
Cı	input capacitance	V _I = 0 V or V _{CC} ; V _{CC} = 0 V to 2.75 V	-	0.5	-	-	-	pF
Co	output capacitance	$V_{O} = 0 \text{ V}; V_{CC} = 0 \text{ V}$	-	1.0	-	-	-	pF
C _{PD}	power dissipation	$f_i = 1 \text{ MHz}; V_I = 0 \text{ V to V}_{CC}$ [5]			1			
	capacitance	V _{CC} = 0.75 V to 0.85 V	-	2.5	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.6	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	2.6	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	2.7	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.0	-	-	-	pF

- [1] All typical values are measured at nominal V_{CC} .
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] For additional propagation delay values at different load capacitances, see Figure 8 to Figure 12.
- [4] t_t is the same as t_{THL} and t_{TLH} .
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + C_L \times V_{CC}^2 \times f_o$ where:

f_i = input frequency in MHz;

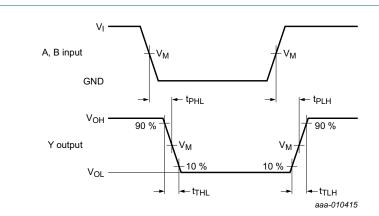
f_o = output frequency in MHz;

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching.

12. Waveforms



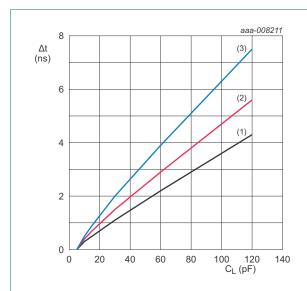
Measurement points are given in Table 9.

 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The data input (A, B) to output (Y) propagation delays and out put transition times

Table 9. Measurement points

Supply voltage	Input	Output		
V _{CC}	V _M	V _I	$t_r = t_f$	V _M
0.75 V to 2.7 V	$0.5 \times V_{CC}$	V _{CC}	≤ 3.0 ns	$0.5 \times V_{CC}$



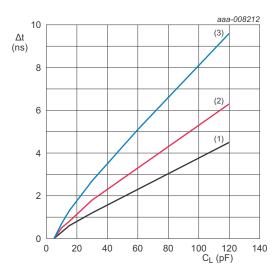
 T_{amb} = -40 °C to +85 °C unless otherwise specified.

(1) Minimum: $V_{CC} = 2.7 \text{ V}$

(2) Typical: $T_{amb} = 25 \,^{\circ}C$; $V_{CC} = 2.5 \,^{\circ}V$

(3) Maximum: $V_{CC} = 2.3 \text{ V}$

Fig 8. Additional t_{pd} versus load capacitance



 T_{amb} = -40 °C to +85 °C unless otherwise specified.

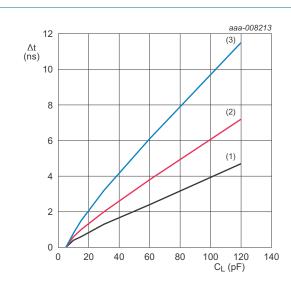
(1) Minimum: $V_{CC} = 1.95 \text{ V}$

(2) Typical: T_{amb} = 25 °C; V_{CC} = 1.8 V

(3) Maximum: $V_{CC} = 1.65 \text{ V}$

Fig 9. Additional t_{pd} versus load capacitance

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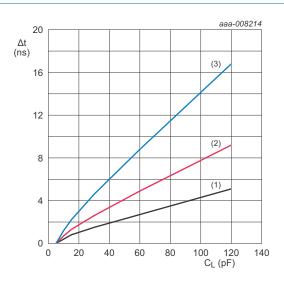
 T_{amb} = -40 °C to +85 °C unless otherwise specified.

(1) Minimum: $V_{CC} = 1.6 \text{ V}$

(2) Typical: $T_{amb} = 25 \,^{\circ}C; V_{CC} = 1.5 \,^{\circ}V$

(3) Maximum: $V_{CC} = 1.4 \text{ V}$

Fig 10. Additional tpd versus load capacitance



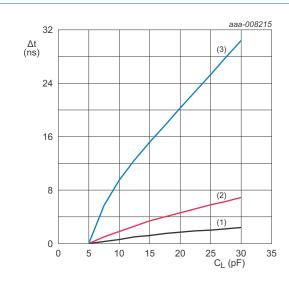
 $T_{amb} = -40$ °C to +85 °C unless otherwise specified.

(1) Minimum: $V_{CC} = 1.3 \text{ V}$

(2) Typical: $T_{amb} = 25 \, ^{\circ}C$; $V_{CC} = 1.2 \, V$

(3) Maximum: $V_{CC} = 1.1 \text{ V}$

Fig 11. Additional tpd versus load capacitance



 $T_{amb} = -40 \, ^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ unless otherwise specified.

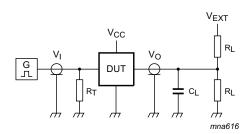
(1) Minimum: $V_{CC} = 0.85 \text{ V}$

(2) Typical: $T_{amb} = 25 \,^{\circ}\text{C}$; $V_{CC} = 0.8 \,^{\circ}\text{V}$

(3) Maximum: $V_{CC} = 0.75 \text{ V}$

Fig 12. Additional t_{pd} versus load capacitance

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Test data is given in Table 10.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 13. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V _{EXT}			
V _{CC}	CL	R _L	t _{PLH} , t _{PHL} t _{PZH} , t _{PHZ} t _{PZL} , t _{PLZ}			
0.75 V to 2.7 V	5 pF	10 kΩ	0 V	0 V	$2 \times V_{CC}$	

13. Package outline

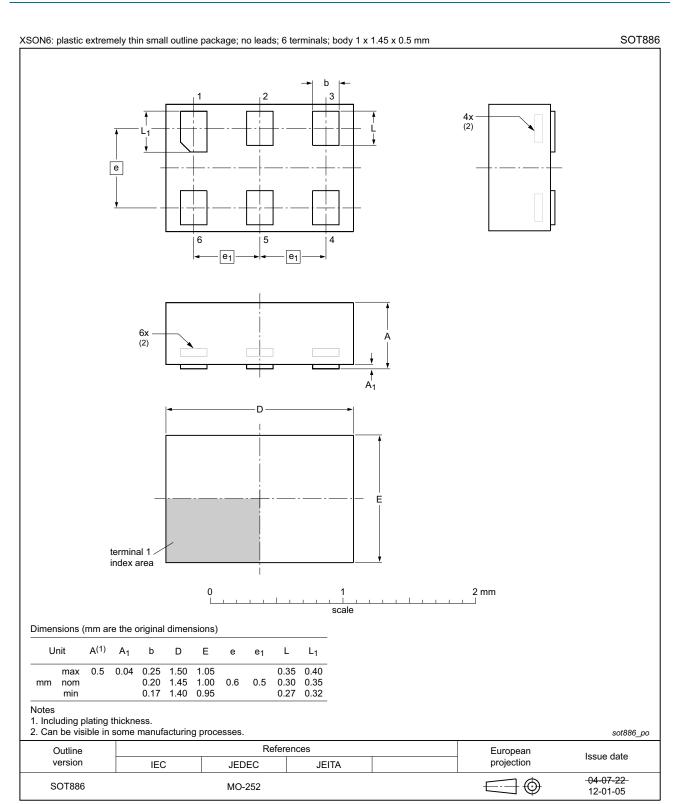


Fig 14. Package outline SOT886 (XSON6)

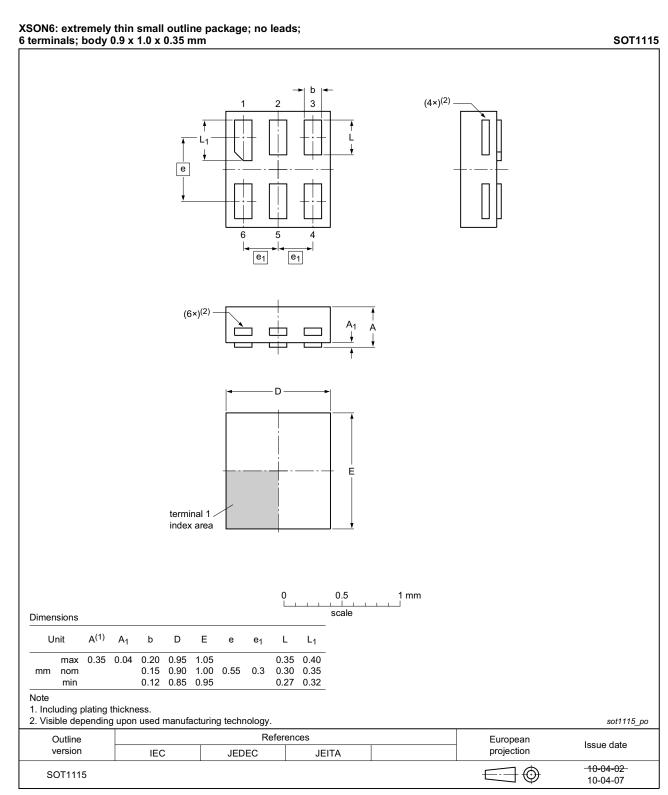


Fig 15. Package outline SOT1115 (XSON6)

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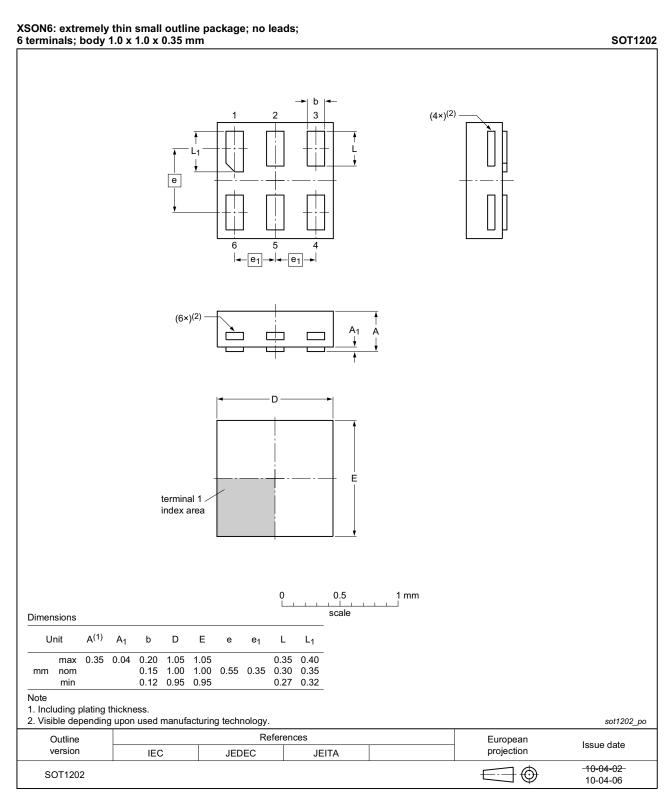


Fig 16. Package outline SOT1202 (XSON6)

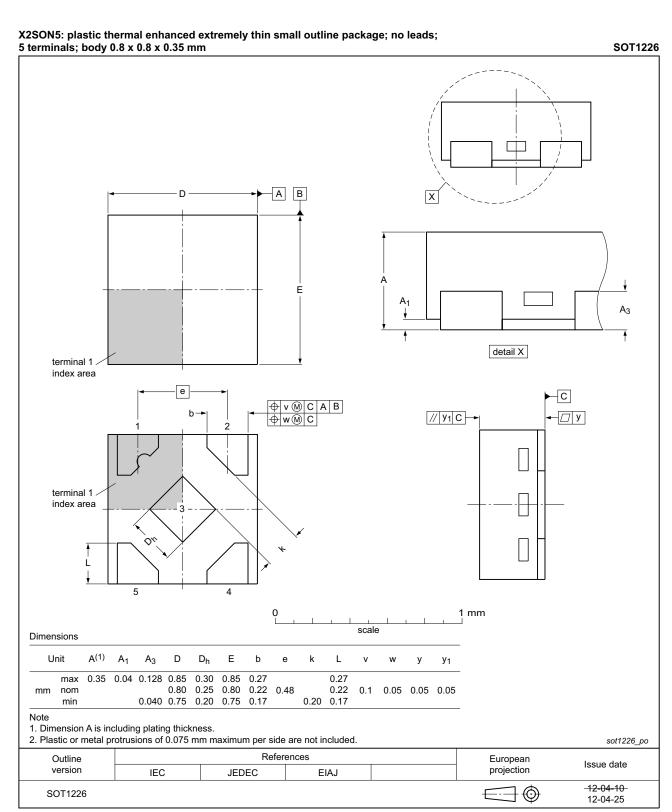


Fig 17. Package outline SOT1226 (X2SON5)

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14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AXP1G86 v.1	20151113	Product data sheet	-	-

Low-power 2-input EXCLUSIVE-OR gate

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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 NLV74HC20ADR2G
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