74AXP4T245

4-bit dual supply translating transceiver; 3-state

Rev. 2 — 6 February 2020 Product data sheet

1. General description

The 74AXP4T245 is an 4-bit dual supply translating transceiver with 3-state outputs that enable bidirectional level translation. The device can be used as two 2-bit transceivers or as a 4-bit transceiver. It features four 2-bit input-output ports (nAn and nBn), a direction control input (nDIR), a output enable input ($n\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.9 V and 5.5 V making the device suitable for translating between any of the low voltage nodes (0.9 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). No power supply sequencing is required and output glitches during power supply transitions are prevented using patented circuitry. As a result glitches will not appear on the outputs for supply transitions during power-up/down between 20 mV/µs and 5.5 V/s.

Pins nAn, $n\overline{OE}$ and nDIR are referenced to $V_{CC(A)}$ and pins nBn are referenced to $V_{CC(B)}$. A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input ($n\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both nAn and nBn are in the high-impedance OFF-state.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 0.9 V to 5.5 V
  - $V_{CC(B)}$: 0.9 V to 5.5 V
- Low input capacitance; C_I = 1.2 pF (typical)
- Low output capacitance; C_O = 3.6 pF (typical)
- Low dynamic power consumption; C_{PD} = 10 pF (typical)
- Low static power consumption; I_{CC} = 2 µA (25 °C maximum)
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-12 (1.1 V to 1.3 V; inputs)
  - JESD8-11 (1.4 V to 1.6 V)
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD12-6 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2 kV
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1 kV
- Latch-up performance exceeds 100 mA per JESD78D Class II
- Inputs accept voltages up to 5.5 V
- Low noise overshoot and undershoot < 10% of V_{CCO}
- I_{OFF} circuitry provides partial power-down mode operation
- Specified from -40 °C to +125 °C

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AXP4T245PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AXP4T245BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

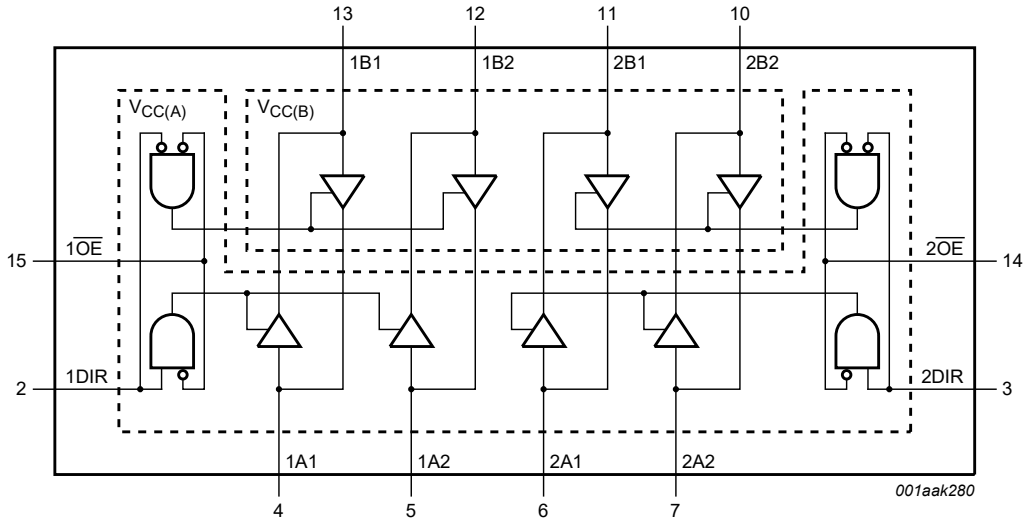


Fig. 1. Logic symbol

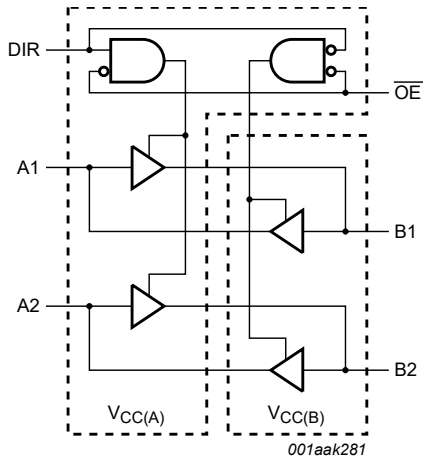


Fig. 2. Logic diagram (one 2-bit transceiver)

5. Pinning information

5.1. Pinning

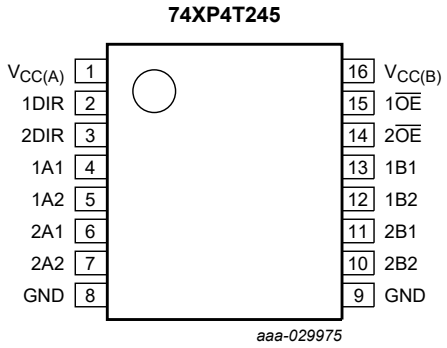
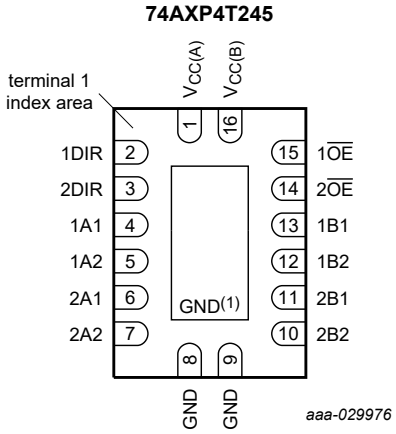


Fig. 3. Pin configuration SOT403-1 (TSSOP16)



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 4. Pin configuration SOT763-1 (DHVQFN16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A (nAn, n$\overline{OE}$ and nDIR are referenced to $V_{CC(A)}$)
1DIR, 2DIR	2, 3	direction control
1A1, 1A2	4, 5	data input or output
2A1, 2A2	6, 7	data input or output
GND [1]	8, 9	ground (0 V)
2B2, 2B1	10, 11	data input or output
1B2, 1B1	12, 13	data input or output
2$\overline{OE}$, 1$\overline{OE}$	14, 15	output enable input (active LOW)
$V_{CC(B)}$	16	supply voltage B (nBn is referenced to $V_{CC(B)}$)

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input		Input/output [1]	
$V_{CC(A)}$, $V_{CC(B)}$	$n\overline{OE}$ [2]	nDIR [2]	nAn [2]	nBn [2]
0.9 V to 5.5 V	L	L	nAn = nBn	input
0.9 V to 5.5 V	L	H	input	nBn = nAn
0.9 V to 5.5 V	H	X	Z	Z
GND [1]	X	X	Z	Z

[1] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.
[2] nAn, nDIR and $n\overline{OE}$ are referenced to $V_{CC(A)}$; nBn is referenced to $V_{CC(B)}$.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			-0.5	+6.5	V
I_{IK}	input clamping current	V_I < 0 V		-20	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	V_O < 0 V		-20	-	mA
V_O	output voltage	Active mode	[1][2][3]	-0.5	V_{CCO} + 0.5	V
		Suspend or 3-state mode	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±25	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin		-	100	mA
I_{GND}	ground current	per GND pin		-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output port.
[3] V_{CCO} + 0.5 V should not exceed 6.5 V.
[4] For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			0.9	5.5	V
$V_{CC(B)}$	supply voltage B			0.9	5.5	V
V_I	input voltage			0	5.5	V
V_O	output voltage	Active mode	[1]	0	V_{CCO}	V
		Suspend or 3-state mode		0	5.5	V
T_{amb}	ambient temperature			-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CCI} = 0.9 V	[2]	-	20	ns/V
		V_{CCI} = 1.2 V		-	20	ns/V
		V_{CCI} = 1.4 V to 1.95 V		-	20	ns/V
		V_{CCI} = 2.3 V to 2.7 V		-	20	ns/V
		V_{CCI} = 3 V to 3.6 V		-	10	ns/V
		V_{CCI} = 4.5 V to 5.5 V		-	8	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.
[2] V_{CCI} is the supply voltage associated with the input port.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +125 °C	+25 °C	
			Min	Typ	Max
V_{IH}	HIGH-level input voltage	nAn, nBn, nDIR, n$\overline{OE}$ input [1]			
		V_{CCI} = 0.9 V	0.7V_{CCI}	-	-
		V_{CCI} = 1.1 V to 1.95 V	0.65V_{CCI}	-	-
		V_{CCI} = 2.3 V to 2.7 V	1.6	-	-
		V_{CCI} = 3.0 V to 3.6 V	2.0	-	-
		V_{CCI} = 4.5 V to 5.5 V	0.7V_{CCI}	-	-
V_{IL}	LOW-level input voltage	nAn, nBn, nDIR, n$\overline{OE}$ input [1]			
		V_{CCI} = 0.9 V	-	-	0.3V_{CCI}
		V_{CCI} = 1.1 V to 1.95 V	-	-	0.35V_{CCI}
		V_{CCI} = 2.3 V to 2.7 V	-	-	0.7
		V_{CCI} = 3.0 V to 3.6 V	-	-	0.8
		V_{CCI} = 4.5 V to 5.5 V	-	-	0.3V_{CCI}
V_{OH}	HIGH-level output voltage	V_I = V_{IH} [2]			
		I_O = -0.1 mA; V_{CCO} = 0.9 V to 5.5 V [3]	V_{CCO} - 0.1	V_{CCO}	-
		I_O = -1.5 mA; V_{CCO} = 1.1 V	0.825	-	-
		I_O = -3 mA; V_{CCO} = 1.4 V	1.05	-	-
		I_O = -4.5 mA; V_{CCO} = 1.65 V	1.2	-	-
		I_O = -8 mA; V_{CCO} = 2.3 V	1.7	-	-
		I_O = -10 mA; V_{CCO} = 3.0 V	2.2	-	-
		I_O = -12 mA; V_{CCO} = 4.5 V	3.7	-	-

Symbol	Parameter	Conditions	-40 °C to +125 °C	+25 °C	
			Min	Typ	Max
V_{OL}	LOW-level output voltage	$V_I = V_{IL}$ [2]			
		I_O = 0.1 mA; V_{CCO} = 0.9 V to 5.5 V [3]	-	0	0.1
		I_O = 1.5 mA; V_{CCO} = 1.1 V	-	-	0.275
		I_O = 3 mA; V_{CCO} = 1.4 V	-	-	0.35
		I_O = 4.5 mA; V_{CCO} = 1.65 V	-	-	0.45
		I_O = 8 mA; V_{CCO} = 2.3 V	-	-	0.7
		I_O = 10 mA; V_{CCO} = 3.0 V	-	-	0.8
		I_O = 8 mA; V_{CCO} = 4.5 V	-	-	0.5
		I_O = 12 mA; V_{CCO} = 4.5 V	-	-	0.8
I_I	input leakage current	nDIR, n$\overline{OE}$ input; V_I = 0 V to 5.5 V; V_{CCI} = 0.9 V to 5.5 V	-	-	±0.1
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; V_{CCO} = 0.9 V to 5.5 V [2]	-	-	±0.1
		suspend mode A port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V [2]	-	-	±0.1
		suspend mode B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V [2]	-	-	±0.1
I_{OFF}	power-off leakage current	nDIR, n$\overline{OE}$ input; V_I = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.9 V to 5.5 V	-	-	0.1
		A port; V_I or V_O = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.9 V to 5.5 V	-	-	0.1
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.9 V to 5.5 V	-	-	0.1
ΔI_{OFF}	additional power-off leakage current	nDIR, n$\overline{OE}$ input; V_I = 0 V or 5.5 V; $V_{CC(A)}$ = 0 V to 0.1 V; $V_{CC(B)}$ = 0.9 V to 5.5 V	-	-	±0.1
		A port; V_O = 0 V or 5.5 V; $V_{CC(A)}$ = 0 V to 0.1 V; $V_{CC(B)}$ = 0.9 V to 5.5 V; V_I = 0 V or 5.5 V	-	-	±0.1
		B port; V_O = 0 V or 5.5 V; $V_{CC(B)}$ = 0 V to 0.1 V; $V_{CC(A)}$ = 0.9 V to 5.5 V; V_I = 0 V or 5.5 V	-	-	±0.1

Symbol	Parameter	Conditions	-40 °C to +125 °C	+25 °C	
			Min	Typ	Max
I_{CC}	supply current	A port; V_I = 0 V or V_{CCI}; I_O = 0 A [1]			
		$V_{CC(A)}$, $V_{CC(B)}$ = 0.9 V to 5.5 V	-	-	2
		$V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V	-	-	2
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-	-	-0.1
		B port; V_I = 0 V or V_{CCI}; I_O = 0 A			
		$V_{CC(A)}$, $V_{CC(B)}$ = 0.9 V to 5.5 V	-	-	2
		$V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 0 V	-	-	-0.1
		$V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 5.5 V	-	-	2
ΔI_{CC}	additional supply current	per input; other pins at V_{CCI} or ground (0 V); I_O = 0 A; $V_{CC(A)}$, $V_{CC(B)}$ = 4.5 V to 5.5 V; V_I = V_{CCI} - 0.6 V [4]	-	2	100

[1] V_{CCI} is the supply voltage associated with the control inputs or input port.
[2] V_{CCO} is the supply voltage associated with the output port.
[3] Typical values for V_{OL} and V_{OH} are measured at V_{CCO} is 0.9 V.
[4] Typical values for ΔI_{CC} are measured at $V_{CC(A)}$, $V_{CC(B)}$ = 5 V.

Table 7. Typical total supply current $I_{CC(A)}$ at T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V).

$V_{CC(A)}$	$V_{CC(B)}$						
	0 V	**0.9 V**	**1.2 V**	**1.5 V**	**1.8 V**	**2.5 V**	
0 V	0.00	0.01	0.01	0.01	0.01	0.01	
0.9 V	0.01	0.01	0.01	0.01	0.01	0.01	
1.2 V	0.01	0.01	0.01	0.01	0.01	0.01	
1.5 V	0.01	0.02	0.01	0.01	0.01	0.01	
1.8 V	0.01	0.06	0.03	0.01	0.01	0.01	
2.5 V	0.01	0.20	0.17	0.12	0.07	0.01	
3.3 V	0.01	0.39	0.37	0.34	0.29	0.12	
5.0 V	0.01	0.96	0.96	0.94	0.90	0.77	

Table 8. Typical total supply current $I_{CC(B)}$ at T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V).

$V_{CC(A)}$	$V_{CC(B)}$						
	0 V	**0.9 V**	**1.2 V**	**1.5 V**	**1.8 V**	**2.5 V**	
0 V	0.00	0.01	0.01	0.01	0.01	0.01	
0.9 V	0.01	0.01	0.01	0.02	0.06	0.20	
1.2 V	0.01	0.01	0.01	0.01	0.03	0.17	
1.5 V	0.01	0.01	0.01	0.01	0.01	0.12	
1.8 V	0.01	0.01	0.01	0.01	0.01	0.07	
2.5 V	0.01	0.01	0.01	0.01	0.01	0.01	
3.3 V	0.01	0.01	0.01	0.01	0.01	0.01	
5.0 V	0.01	0.01	0.01	0.01	0.01	0.01	

10. Dynamic characteristics

Table 9. Typical dynamic characteristics at $V_{CC(A)}$ = 0.9 V and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 5 and Fig. 6.

Symbol	Parameter	Conditions		$V_{CC(B)}$							Unit
				0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{pd}	propagation delay	nAn to nBn	[1]	40	22	18.5	16.5	15	15	15	ns
		nBn to nAn	[1]	40	33	32	31	31	31	32	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	[1]	34	34	34	34	34	34	34	ns
		n$\overline{OE}$ to nBn	[1]	42	30	26	26	24	25	23	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	[1]	49	49	49	49	49	49	49	ns
		n$\overline{OE}$ to nBn	[1]	52	32	28	27	27	27	30	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 10. Typical dynamic characteristics at $V_{CC(B)}$ = 0.9 V and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 5 and Fig. 6.

Symbol	Parameter	Conditions		$V_{CC(A)}$							Unit
				0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{pd}	propagation delay	nAn to nBn	[1]	40	33	32	31	31	31	32	ns
		nBn to nAn	[1]	40	22	18.5	16.5	15	15	15	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	[1]	34	16	11	10	7	7.7	5.3	ns
		n$\overline{OE}$ to nBn	[1]	42	31	28	28	27	27	27	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	[1]	49	18	11.5	8.4	5.6	4.5	3.6	ns
		n$\overline{OE}$ to nBn	[1]	52	39	36	35	34	34	35	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 11. Typical power dissipation capacitance at $V_{CC(A)}$ = $V_{CC(B)}$ and T_{amb} = 25 °C

[1] [2]Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$							Unit
			0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
C_{PD}	power dissipation capacitance	A port: (direction A to B); B port: (direction B to A)	0.5	0.5	0.5	0.5	0.5	0.7	0.9	pF
		A port: (direction B to A); B port: (direction A to B)	9.0	9.3	9.5	9.7	9.9	10.2	10.9	pF
C_I	input capacitance	V_I = 0 V or V_{CCI}; V_{CCI} = 0 V to 5.5 V	1.2	1.2	1.2	1.2	1.2	1.2	1.2	pF
$C_{I/O}$	input/output capacitance	V_O = 0 V; V_{CCO} = 0 V	3.6	3.6	3.6	3.6	3.6	3.6	3.6	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f_i = 1 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; R_L = ∞ Ω.

Table 12. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 5 and Fig. 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$							
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V	
			Min	Max	Min	Max	Min	Max	Min	Ma
t_{pd}	propagation delay	nAn to nBn [1]								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	4	38	3.6	25	3.4	21	3.1	16
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	3.5	33	3	21	2.8	16.5	2.6	12.
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	3.1	32	2.7	19	2.4	15	2.2	11
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	2.8	31	2.4	17.5	2.1	13.5	1.9	9.1
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	2.7	31	2.3	17	2	13	1.8	8.5
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	2.7	31	2.2	16.5	1.9	12.5	1.6	8.1
		nBn to nAn								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	4	38	3.5	33	3.1	32	2.8	31
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	3.6	25	3	21	2.7	19	2.4	17.
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	3.4	21	2.8	16.5	2.4	15	2.1	13.
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	3.1	16	2.6	12.5	2.2	11	1.9	9.1
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	2.9	14.5	2.4	10.5	2.1	9	1.7	7.5
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	2.7	14.5	2.2	9.8	1.9	8.2	1.6	6.6

Symbol	Parameter	Conditions	$V_{CC(B)}$							
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V	
			Min	Max	Min	Max	Min	Max	Min	Ma
t_{en}	enable time	$n\overline{OE}$ to nAn [1]								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	4.6	48	4.6	48	4.6	48	4.6	48
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	3.6	24	3.6	24	3.6	24	3.6	24
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	2.9	17.5	2.9	17.5	2.9	17.5	2.9	17.
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	2.3	11	2.3	11	2.3	11	2.3	11
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	2	8.1	2	8.1	2	8.1	2	8.1
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	1.8	6	1.8	6	1.8	6	1.8	6
		$n\overline{OE}$ to nBn								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	5	46	4.6	32	4.1	27	4.1	24
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	4.2	40	3.8	24	3.5	19.5	3.3	16
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	3.9	36	3.3	21	3	17.5	2.8	13.
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	3.4	35	2.8	18.5	2.5	14.5	2.3	11
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	3.2	34	2.7	17.5	2.3	13.5	2.1	9.5
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	3.1	37	2.4	17	2.1	13	1.9	8.7

Symbol	Parameter	Conditions	$V_{CC(B)}$							
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V	
			Min	Max	Min	Max	Min	Max	Min	Ma
t_{dis}	disable time	$n\overline{OE}$ to nAn [1]								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	4.9	36	4.9	36	4.9	36	4.9	36
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	3.9	22	3.9	22	3.9	22	3.9	22
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	4	19	4	19	4	19	4	19
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	2.9	13	2.9	13	2.9	13	2.9	13
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	3.5	13	3.5	13	3.5	13	3.5	13
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	2.4	9.7	2.4	9.7	2.4	9.7	2.4	9.7
		$n\overline{OE}$ to nBn								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	5.6	41	4.8	32	5.1	30	4.4	26
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	5.1	34	4.4	25	4.6	23	3.8	18.
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	4.7	32	4	23	4.3	21	3.4	16.
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	4.3	29.5	3.6	20.6	3.9	18.5	3	14.
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	4.2	29	3.5	19.5	3.7	17.5	2.9	13.
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	4.1	28	3.3	19	3.6	16.5	2.7	12.
t_t	transition time	nAn, nBn output								
		$V_{CC(A)}$ = 1.1 V to 5.5 V	1	-	1	-	1	-	1	-

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 13. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 5 and Fig. 6.

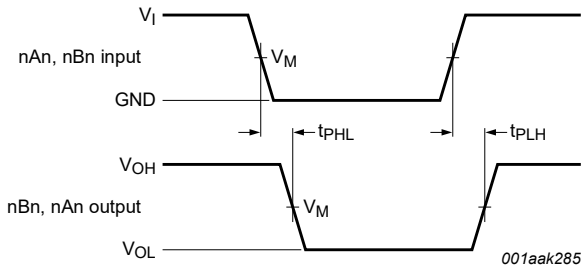
Symbol	Parameter	Conditions	$V_{CC(B)}$							
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V	
			Min	Max	Min	Max	Min	Max	Min	Ma
t_{pd}	propagation delay	nAn to nBn [1]								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	4	38	3.6	26	3.4	22	3.1	17
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	3.5	33	3	22	2.8	17.5	2.6	13.
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	3.1	32	2.7	20	2.4	16	2.2	12
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	2.8	31	2.4	18.5	2.1	14.5	1.9	9.8
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	2.7	31	2.3	18	2	14	1.8	9.2
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	2.7	31	2.2	17.5	1.9	13.5	1.6	8.8
		nBn to nAn								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	4	38	3.5	33	3.1	32	2.8	31
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	3.6	26	3	22	2.7	20	2.4	18.
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	3.4	22	2.8	17.5	2.4	16	2.1	14.
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	3.1	17	2.6	13.5	2.2	12	1.9	9.8
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	2.9	15	2.4	11.5	2.1	9.7	1.7	8.1
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	2.7	15	2.2	10.5	1.9	8.7	1.6	7.1

Symbol	Parameter	Conditions	$V_{CC(B)}$							
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V	
			Min	Max	Min	Max	Min	Max	Min	Ma
t_{en}	enable time	$n\overline{OE}$ to nAn [1]								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	4.6	48	4.6	48	4.6	48	4.6	48
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	3.6	25	3.6	25	3.6	25	3.6	25
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	2.9	18.5	2.9	18.5	2.9	18.5	2.9	18.
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	2.3	11.5	2.3	11.5	2.3	11.5	2.3	11.
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	2	8.7	2	8.7	2	8.7	2	8.7
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	1.8	6.5	1.8	6.5	1.8	6.5	1.8	6.5
		$n\overline{OE}$ to nBn								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	5	46	4.6	32	4.1	28	4.1	25
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	4.2	40	3.8	25	3.5	21	3.3	17
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	3.9	36	3.3	23	3	19	2.8	14.
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	3.4	35	2.8	19.5	2.5	15.5	2.3	12
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	3.2	34	2.7	18.5	2.3	14.5	2.1	10.
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	3.1	37	2.4	18	2.1	14	1.9	9.4

Symbol	Parameter	Conditions	$V_{CC(B)}$							
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V	
			Min	Max	Min	Max	Min	Max	Min	Ma
t_{dis}	disable time	$n\overline{OE}$ to nAn [1]								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	4.9	36	4.9	36	4.9	36	4.9	36
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	3.9	23	3.9	23	3.9	23	3.9	23
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	4	20	4	20	4	20	4	20
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	2.9	14	2.9	14	2.9	14	2.9	14
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	3.5	14	3.5	14	3.5	14	3.5	14
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	2.4	10.2	2.4	10.2	2.4	10.2	2.4	10.
		$n\overline{OE}$ to nBn								
		$V_{CC(A)}$ = 1.2 V ± 0.1 V	5.6	41	4.8	33	5.1	31	4.4	27
		$V_{CC(A)}$ = 1.5 V ± 0.1 V	5.1	35	4.4	27	4.6	25	3.8	20
		$V_{CC(A)}$ = 1.8 V ± 0.15 V	4.7	33	4	24	4.3	22	3.4	17.
		$V_{CC(A)}$ = 2.5 V ± 0.2 V	4.3	31	3.6	22	3.9	19.5	3	15.
		$V_{CC(A)}$ = 3.3 V ± 0.3 V	4.2	30	3.5	21	3.7	18.5	2.9	14.
		$V_{CC(A)}$ = 5.0 V ± 0.5 V	4.1	29	3.3	20	3.6	17.5	2.7	13.
t_t	transition time	nAn, nBn output								
		$V_{CC(A)}$ = 1.1 V to 5.5 V	1		1		1		1	

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

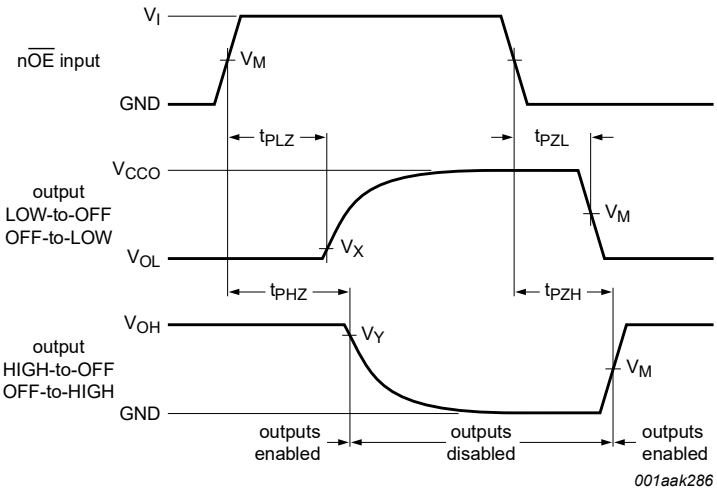
10.1. Waveforms and test circuit



Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times



Measurement points are given in Table 14.

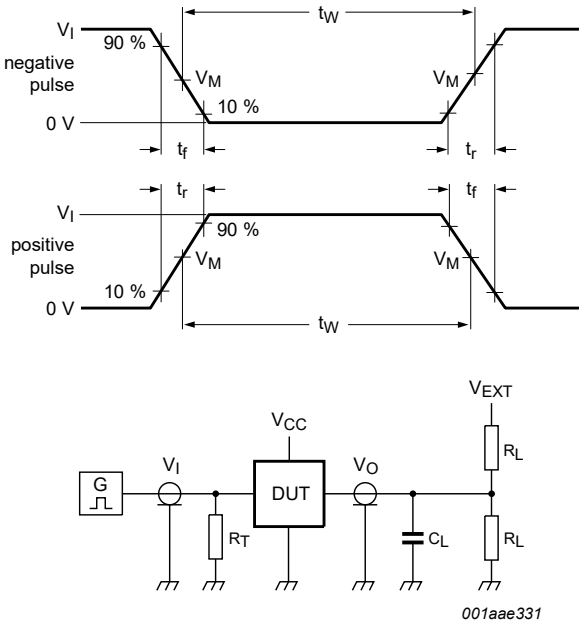
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Enable and disable times

Table 14. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.9 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 5.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in Table 15.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

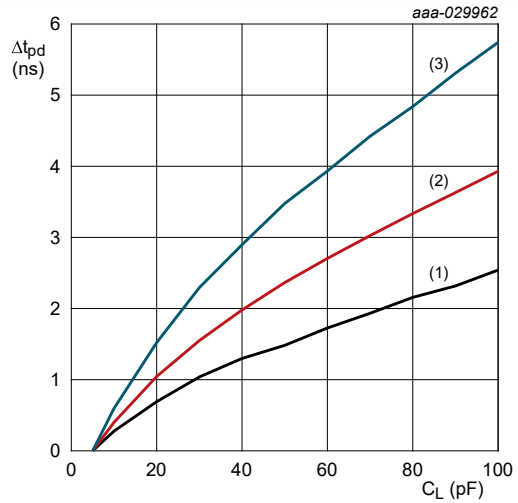
Table 15. Test data

Supply voltage	Load		Input		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	C_L	R_L	t_r, t_f	V_I [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [2]
0.9 V to 5.5 V	5 pF	10 kΩ	≤3.0 ns	V_{CCI}	GND	GND	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the data input port.

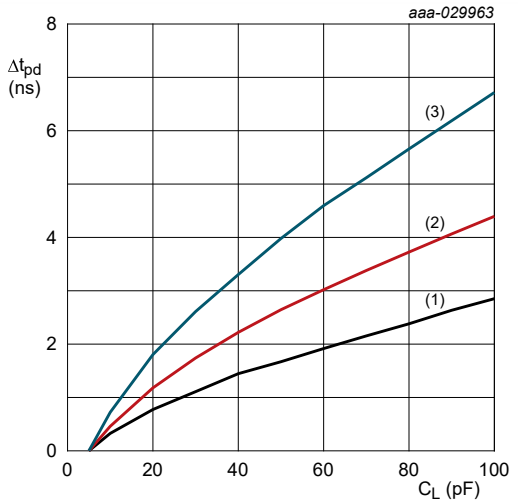
[2] V_{CCO} is the supply voltage associated with the output port.

10.2. Additional propagation delay versus load capacitance graphs



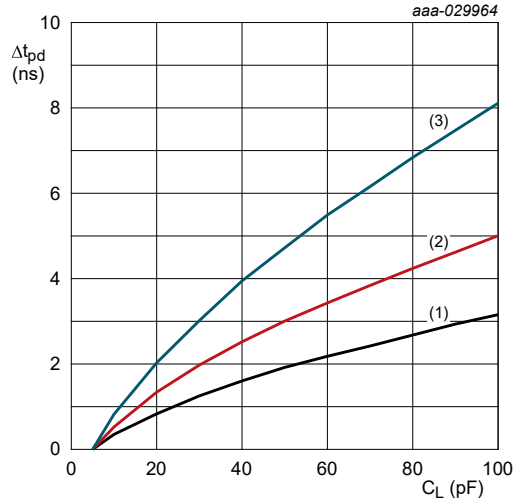
T_{amb} = -40 °C to +125 °C
For t_{PLH}, t_{PHL}, t_{PZH} and t_{PZL}
(1) Minimum: V_{CCO} = 5.5 V
(2) Typical: T_{amb} = 25 °C; V_{CCO} = 5 V
(3) Maximum: V_{CCO} = 4.5 V

Fig. 8. Additional propagation delay versus load capacitance



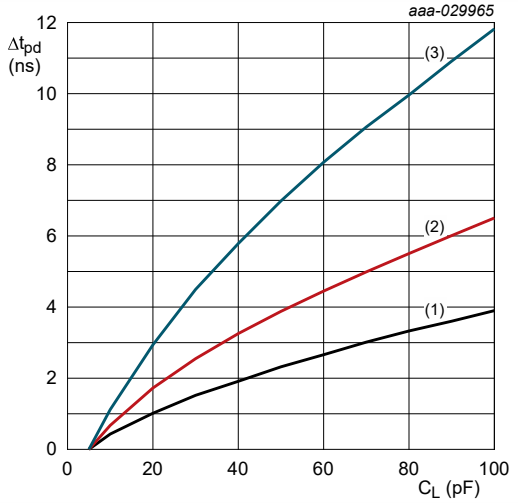
T_{amb} = -40 °C to +125 °C
For t_{PLH}, t_{PHL}, t_{PZH} and t_{PZL}
(1) Minimum: V_{CCO} = 3.6 V
(2) Typical: T_{amb} = 25 °C; V_{CCO} = 3.3 V
(3) Maximum: V_{CCO} = 3 V

Fig. 9. Additional propagation delay versus load capacitance



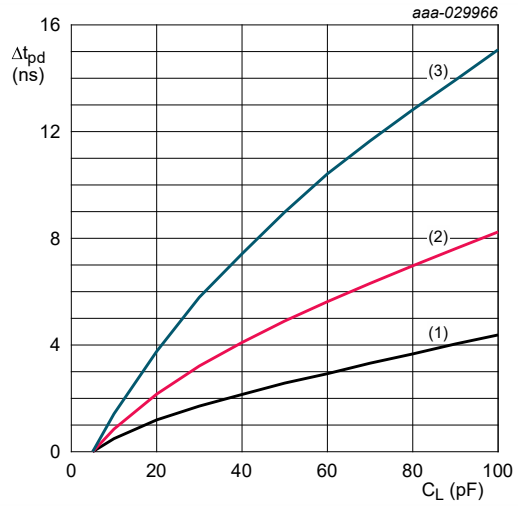
T_{amb} = -40 °C to +125 °C
For t_{PLH}, t_{PHL}, t_{PZH} and t_{PZL}
(1) Minimum: V_{CCO} = 2.7 V
(2) Typical: T_{amb} = 25 °C; V_{CCO} = 2.5 V
(3) Maximum: V_{CCO} = 2.3 V

Fig. 10. Additional propagation delay versus load capacitance



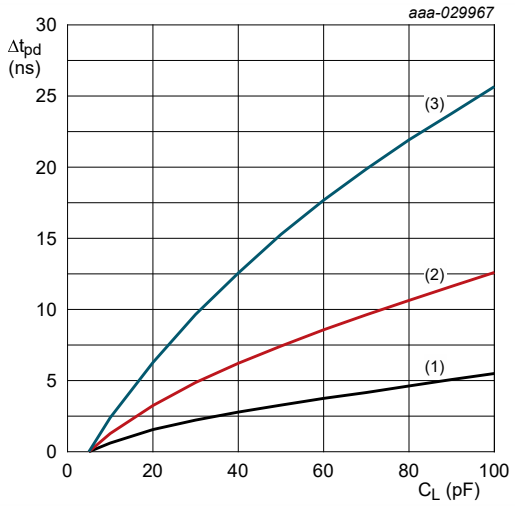
T_{amb} = -40 °C to +125 °C
For t_{PLH}, t_{PHL}, t_{PZH} and t_{PZL}
(1) Minimum: V_{CCO} = 1.95 V
(2) Typical: T_{amb} = 25 °C; V_{CCO} = 1.8 V
(3) Maximum: V_{CCO} = 1.65 V

Fig. 11. Additional propagation delay versus load capacitance



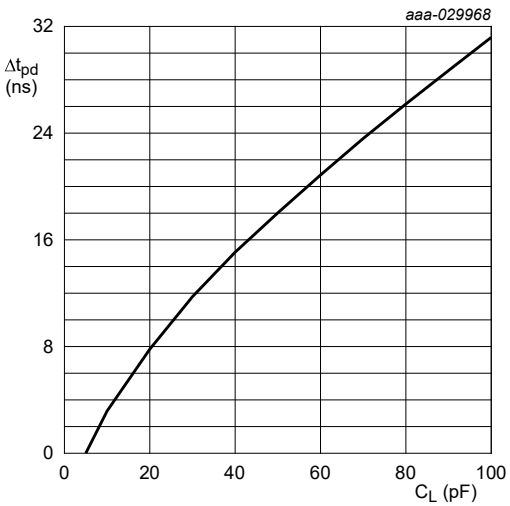
T_{amb} = -40 °C to +125 °C
For t_{PLH}, t_{PHL}, t_{PZH} and t_{PZL}
(1) Minimum: V_{CCO} = 1.6 V
(2) Typical: T_{amb} = 25 °C; V_{CCO} = 1.5 V
(3) Maximum: V_{CCO} = 1.4 V

Fig. 12. Additional propagation delay versus load capacitance



T_{amb} = -40 °C to +125 °C
For t_{PLH}, t_{PHL}, t_{PZH} and t_{PZL}
(1) Minimum: V_{CCO} = 1.3 V
(2) Typical: T_{amb} = 25 °C; V_{CCO} = 1.2 V
(3) Maximum: V_{CCO} = 1.1 V

Fig. 13. Additional propagation delay versus load capacitance



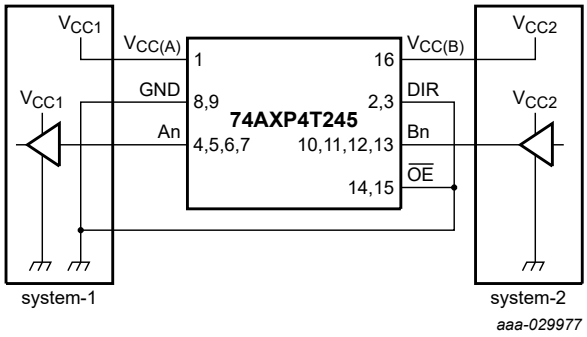
T_{amb} = 25 °C; V_{CCO} = 0.9 V
For t_{PLH}, t_{PHL}, t_{PZH} and t_{PZL}

Fig. 14. Additional propagation delay versus load capacitance

11. Application information

11.1. Unidirectional logic level-shifting application

The circuit given in Fig. 15 is an example of the 74AXP4T245 being used in an unidirectional logic level-shifting application.



Schematic given for one channel.

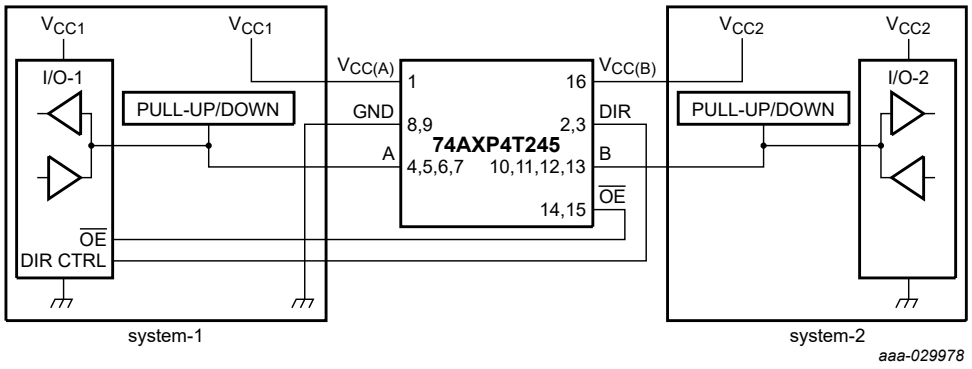
Fig. 15. Unidirectional logic level-shifting application

Table 16. Description unidirectional logic level-shifting application

Name	Function	Description
$V_{CC(A)}$	V_{CC1}	supply voltage of system-1 (0.9 V to 5.5 V)
GND	GND	device GND
A	OUT	output level depends on V_{CC1} voltage
B	IN	input threshold value depends on V_{CC2} voltage
DIR	DIR	the GND (LOW level) determines B port to A port direction
$V_{CC(B)}$	V_{CC2}	supply voltage of system-2 (0.9 V to 5.5 V)
$\overline{OE}$	$\overline{OE}$	The GND (LOW level) enables the output ports

11.2. Bidirectional logic level-shifting application

Fig. 16 shows the 74AXP4T245 being used in a bidirectional logic level-shifting application.



Schematic given for one channel.

Pull-up or pull-down only needed for 74AXP4T245.

Fig. 16. Bidirectional logic level-shifting application

Table 17 gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

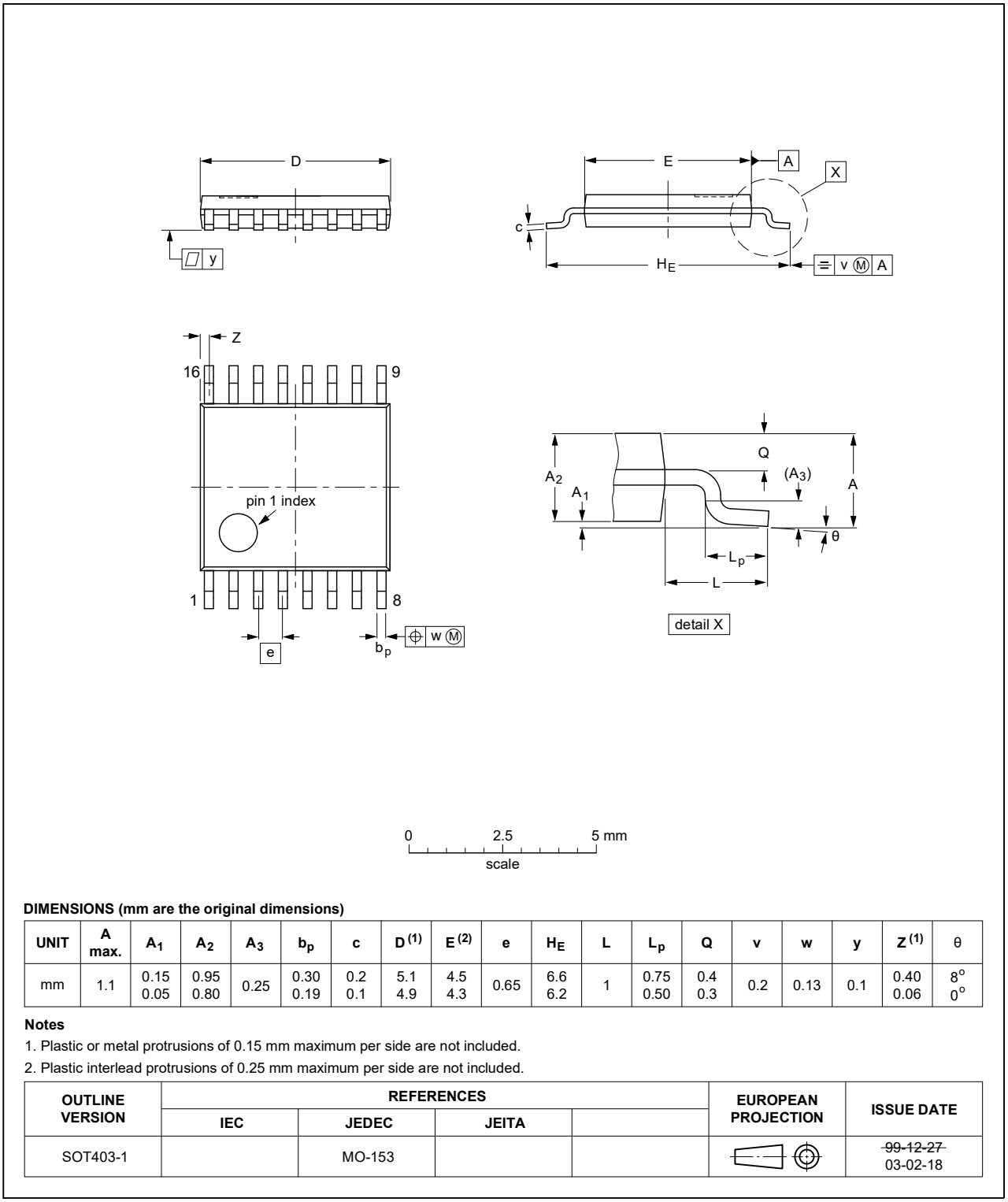
Table 17. Description bidirectional logic level-shifting application

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

State	DIR CTRL	$\overline{OE}$	I/O-1	I/O-2	Description
1	H	L	output	input	system-1 data to system-2
2	H	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	H	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold.
4	L	L	input	output	system-2 data to system-1

12. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

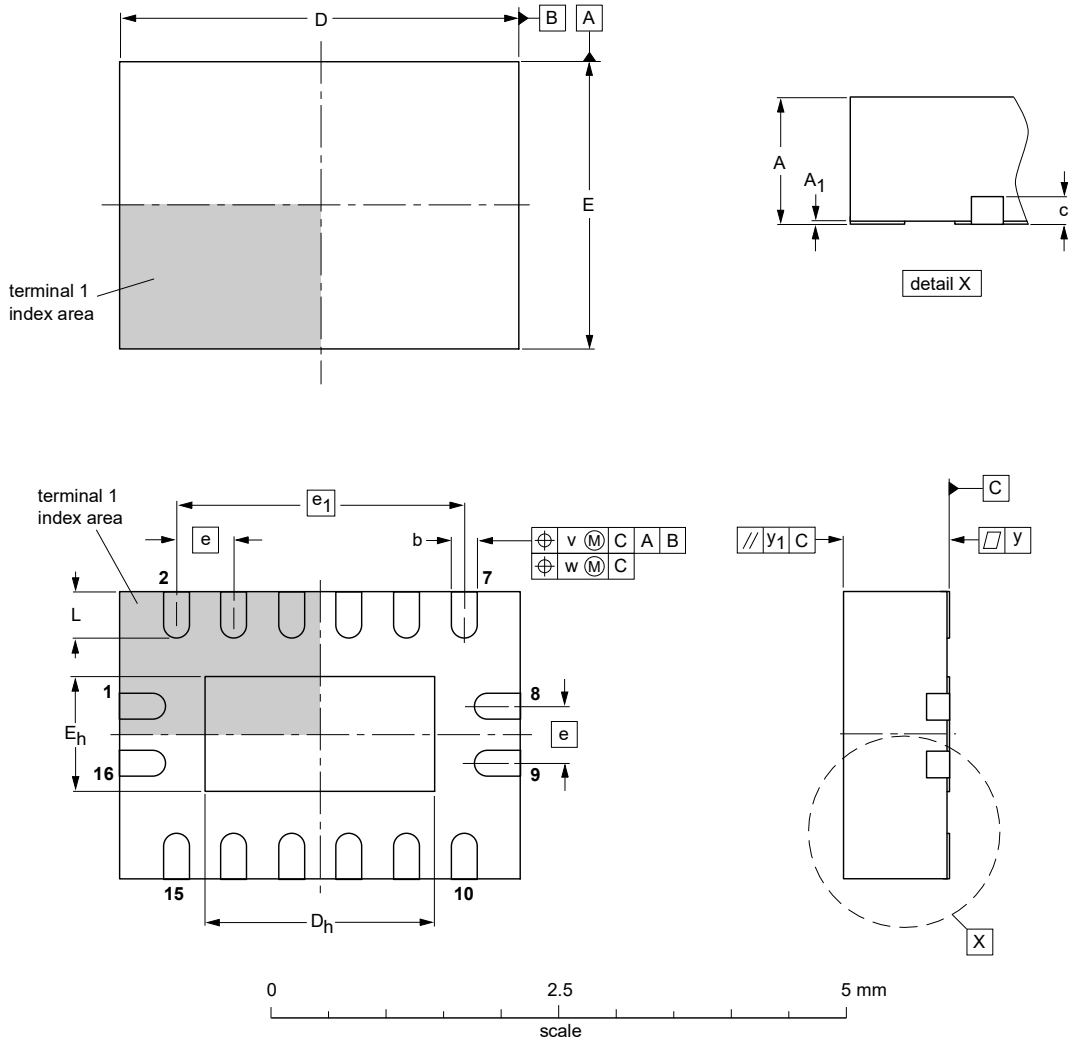
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 17. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 18. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AXP4T245 v.2	20200206	Product data sheet	-	-
Modifications:	• Section 1: General description updated.			
74AXP4T245 v.1	20190624	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 6 February 2020

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Translation - Voltage Levels ***category:***

Click to view products by Nexperia ***manufacturer:***

Other Similar products are found below :

NLSX4373DMR2G NLSX5012MUTAG NLSX0102FCT2G NLSX4302EBMUTCG PCA9306FMUTAG MC100EPT622MNG NLSX3014MUTAG NLSV4T244EMUTAG NLSX5011MUTCG NLV9306USG NLVSX4014MUTAG NLSV4T3144MUTAG NLVSX4373MUTAG MAX3371ELT+T NLSX3013BFCT1G NLV7WBD3125USG NLSX3012DMR2G 74AVCH1T45FZ4-7 NLVSV1T244MUTBG 74AVC1T45GS-Q100H CLVC16T245MDGGREP MC10H124FNG CAVCB164245MDGGREP CD40109BPWR MC10H350FNG MC10H125FNG MC100EPT21MNR4G MC100EP91DWG NLSV2T244MUTAG NLSX3013FCT1G NLSX5011AMX1TCG PCA9306USG SN74AVCA406LZQSR NLSX4014DTR2G NLSX3018DTR2G LTC1045CSW#PBF LTC1045CN#PBF SY100EL92ZG 74AXP1T34GMH 74AXP1T34GNH PI4ULS3V204LE ADG3245BRUZ-REEL7 ADG3123BRUZ ADG3245BRUZ ADG3246BCPZ ADG3308BCPZ-REEL ADG3233BRJZ-REEL7 ADG3233BRMZ ADG3241BKSZ-500RL7 ADG3242BRJZ-REEL7