

74HC151; 74HCT151

8-input multiplexer

Rev. 8 — 18 March 2021

Product data sheet

1. General description

The 74HC151; 74HCT151 are 8-bit multiplexer with eight binary inputs (I0 to I7), three select inputs (S0 to S2) and an enable input (E). One of the eight binary inputs is selected by the select inputs and routed to the complementary outputs (Y and \bar{Y}). A HIGH on E forces the output Y LOW and output \bar{Y} HIGH. Inputs also include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Specified in compliance with JEDEC standard no. 7A
- Input levels:
 - For 74HC151: CMOS level
 - For 74HCT151: TTL level
- Low-power dissipation
- Non-inverting data path
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC151D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT151D				
74HC151DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC151PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT151PW				

4. Functional diagram

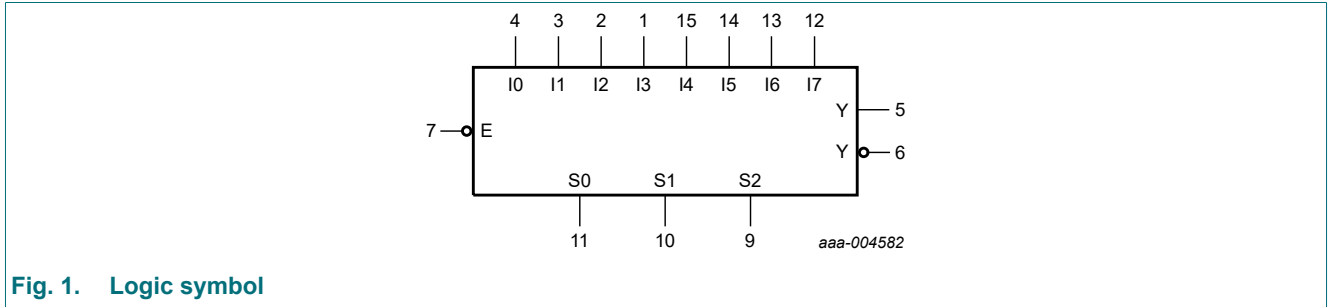


Fig. 1. Logic symbol

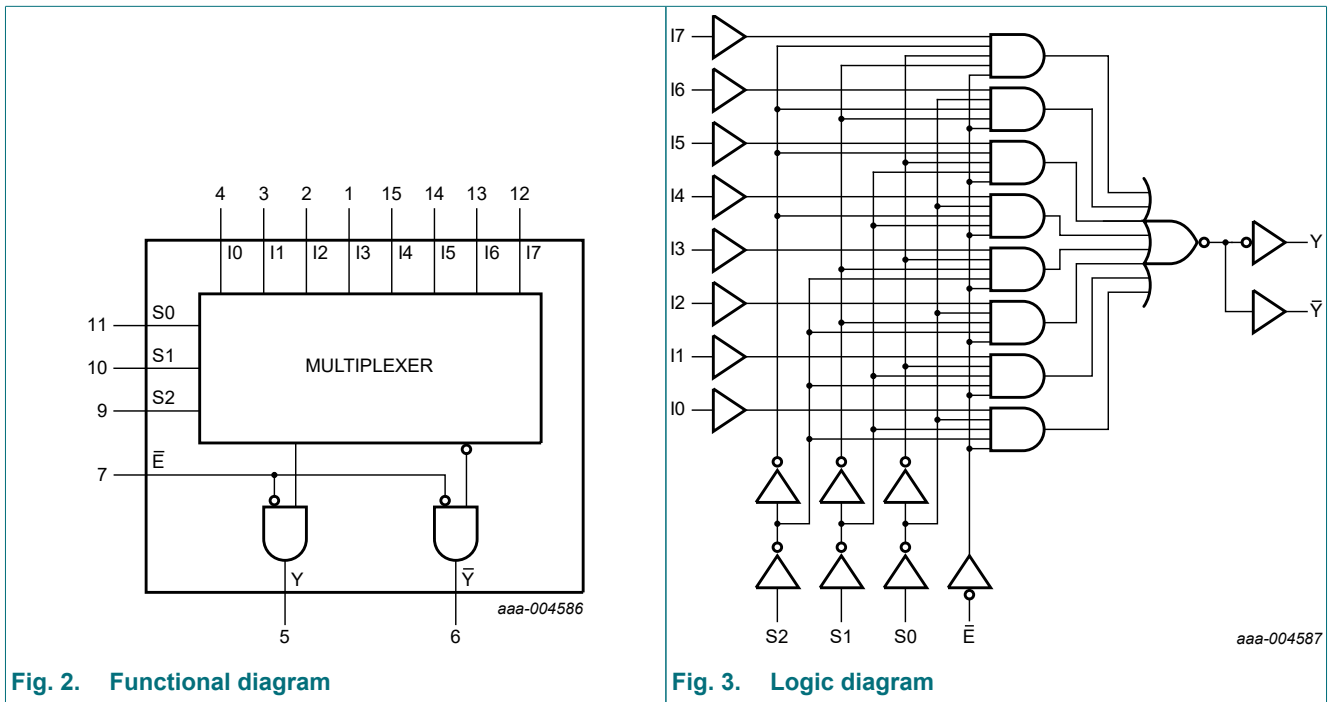


Fig. 2. Functional diagram

Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning

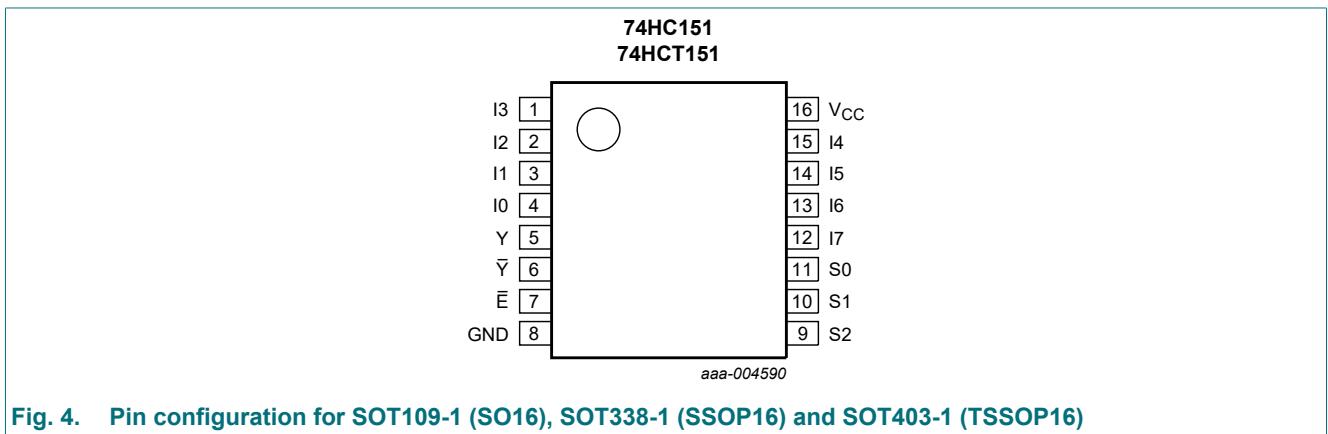


Fig. 4. Pin configuration for SOT109-1 (SO16), SOT338-1 (SSOP16) and SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
I0 to I7	4, 3, 2, 1, 15, 14, 13, 12	data inputs
Y	5	multiplexer output
\bar{Y}	6	complementary multiplexer output
\bar{E}	7	enable input (active LOW)
GND	8	ground (0 V)
S0, S1, S2	11, 10, 9	common data select inputs
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input												Output	
\bar{E}	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	\bar{Y}	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]	-	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
 For SOT338-1 (SSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
 For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC151			74HCT151			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC151										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT151										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		per input pin; In inputs	-	45	162	-	203	-	221	µA
		per input pin; \bar{E} input	-	30	108	-	135	-	147	µA
		per input pin; Sn input	-	150	540	-	675	-	735	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC151										
t_{pd}	propagation delay	In to Y; see Fig. 5 [1]								
		$V_{CC} = 2.0$ V	-	52	170	-	215	-	255	ns
		$V_{CC} = 4.5$ V	-	19	34	-	43	-	51	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	15	29	-	37	-	43	ns
		In to \bar{Y} ; see Fig. 5 [1]								
		$V_{CC} = 2.0$ V	-	58	185	-	230	-	280	ns
		$V_{CC} = 4.5$ V	-	21	37	-	46	-	56	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	17	31	-	39	-	48	ns
		Sn to Y; see Fig. 6 [1]								
		$V_{CC} = 2.0$ V	-	61	185	-	230	-	280	ns
		$V_{CC} = 4.5$ V	-	22	37	-	46	-	56	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	18	31	-	39	-	48	ns
		Sn to \bar{Y} ; see Fig. 6 [1]								
		$V_{CC} = 2.0$ V	-	61	205	-	255	-	310	ns
		$V_{CC} = 4.5$ V	-	22	41	-	51	-	62	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	18	35	-	43	-	53	ns
		\bar{E} to Y; see Fig. 6								
		$V_{CC} = 2.0$ V	-	41	125	-	155	-	190	ns
		$V_{CC} = 4.5$ V	-	15	25	-	31	-	38	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	12	-	-	-	-	-	ns
$V_{CC} = 6.0$ V	-	12	21	-	26	-	32	ns		
\bar{E} to \bar{Y} ; see Fig. 6										
$V_{CC} = 2.0$ V	-	47	145	-	180	-	220	ns		
$V_{CC} = 4.5$ V	-	17	29	-	36	-	44	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	14	25	-	31	-	38	ns		
t_t	transition time	Y, \bar{Y} ; see Fig. 5 [2]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ [3]	-	40	-	-	-	-	pF	

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT151										
t _{pd}	propagation delay	In to Y; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	22	38	-	48	-	57	ns
		V _{CC} = 5 V; C _L = 15 pF	-	19	-	-	-	-	-	ns
		In to \bar{Y} ; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	22	38	-	48	-	57	ns
		V _{CC} = 5 V; C _L = 15 pF	-	19	-	-	-	-	-	ns
		S _n to Y; see Fig. 6 [1]								
		V _{CC} = 4.5 V	-	23	41	-	51	-	62	ns
		V _{CC} = 5 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		S _n to \bar{Y} ; see Fig. 6 [1]								
		V _{CC} = 4.5 V	-	25	43	-	54	-	65	ns
		V _{CC} = 5 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		\bar{E} to Y; see Fig. 6 [1]								
		V _{CC} = 4.5 V	-	16	29	-	36	-	44	ns
V _{CC} = 5 V; C _L = 15 pF	-	13	-	-	-	-	-	ns		
\bar{E} to \bar{Y} ; see Fig. 6 [1]										
V _{CC} = 4.5 V	-	21	36	-	45	-	54	ns		
V _{CC} = 5 V; C _L = 15 pF	-	18	-	-	-	-	-	ns		
t _t	transition time	Y, \bar{Y} ; see Fig. 5 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V [3]	-	40	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] t_t is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

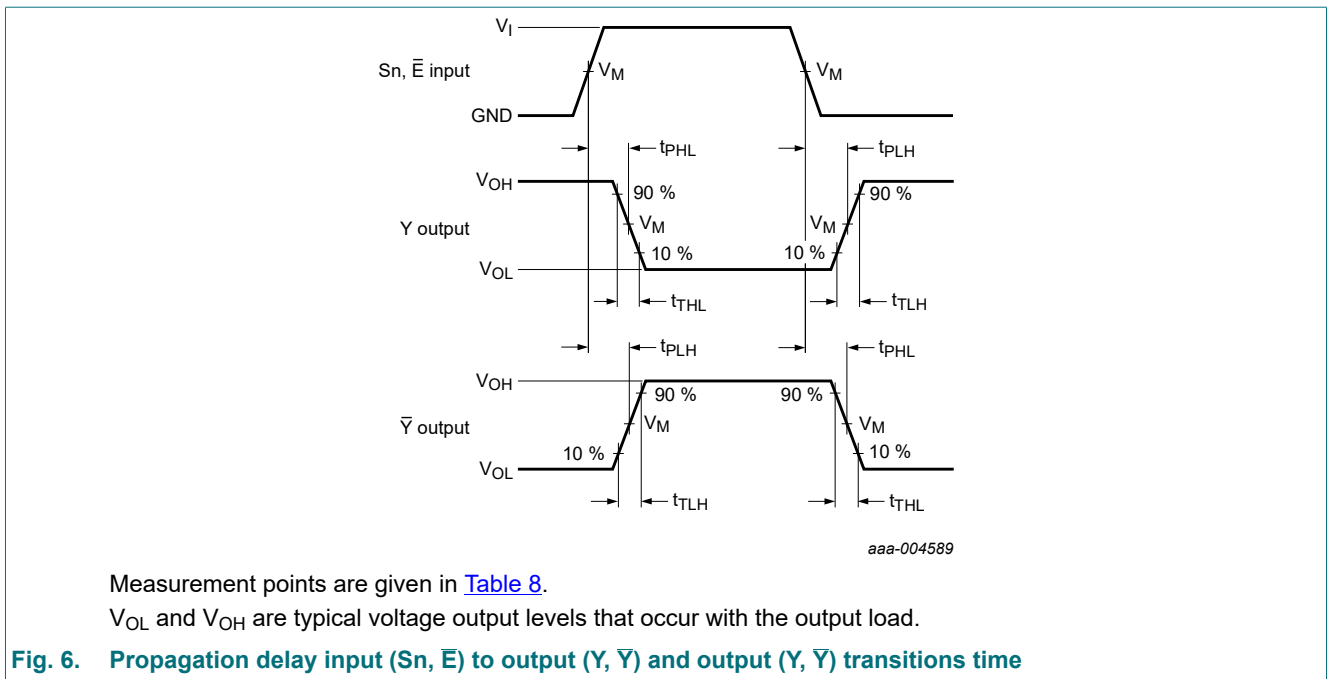
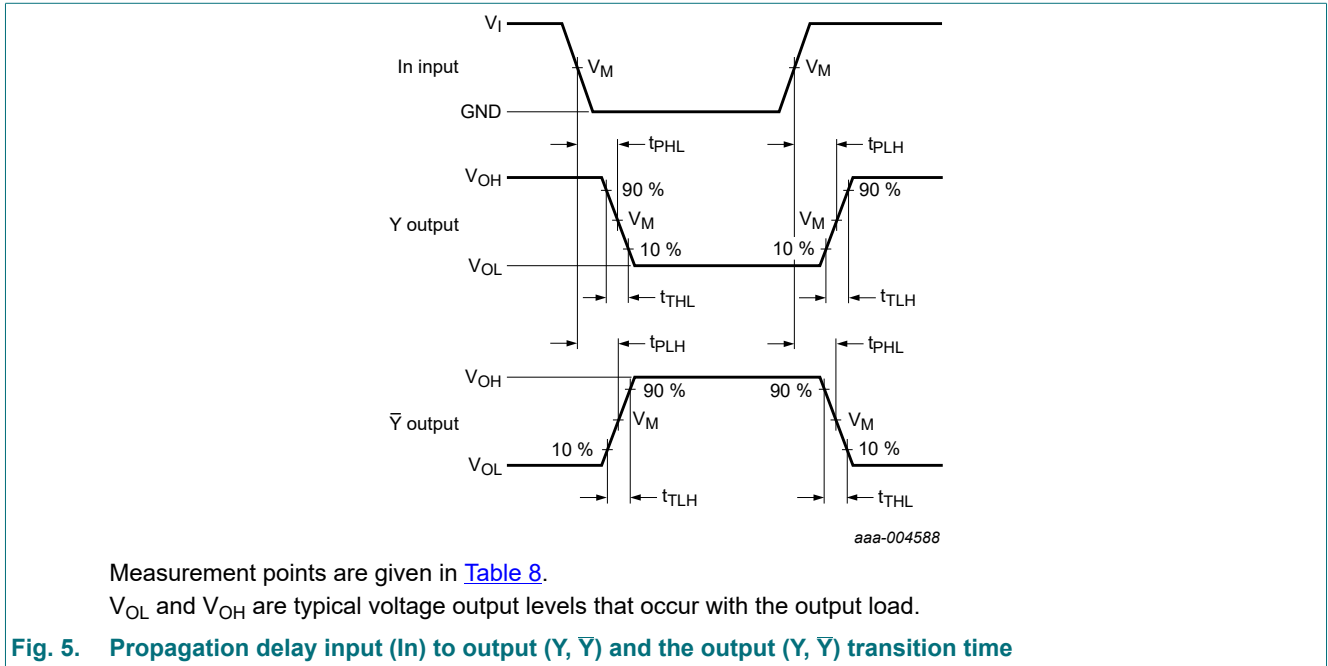
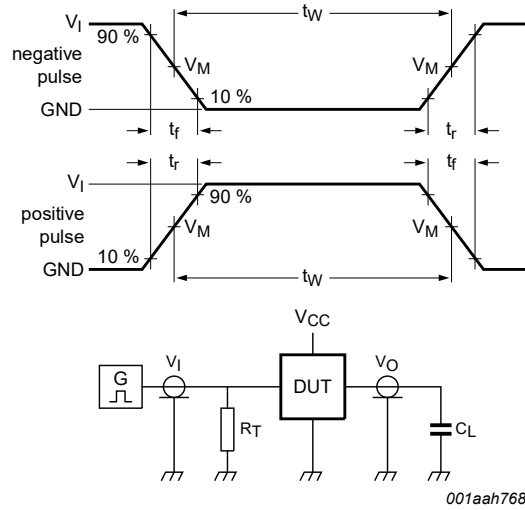


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC151	$0.5V_{CC}$	$0.5V_{CC}$
74HCT151	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC151	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT151	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

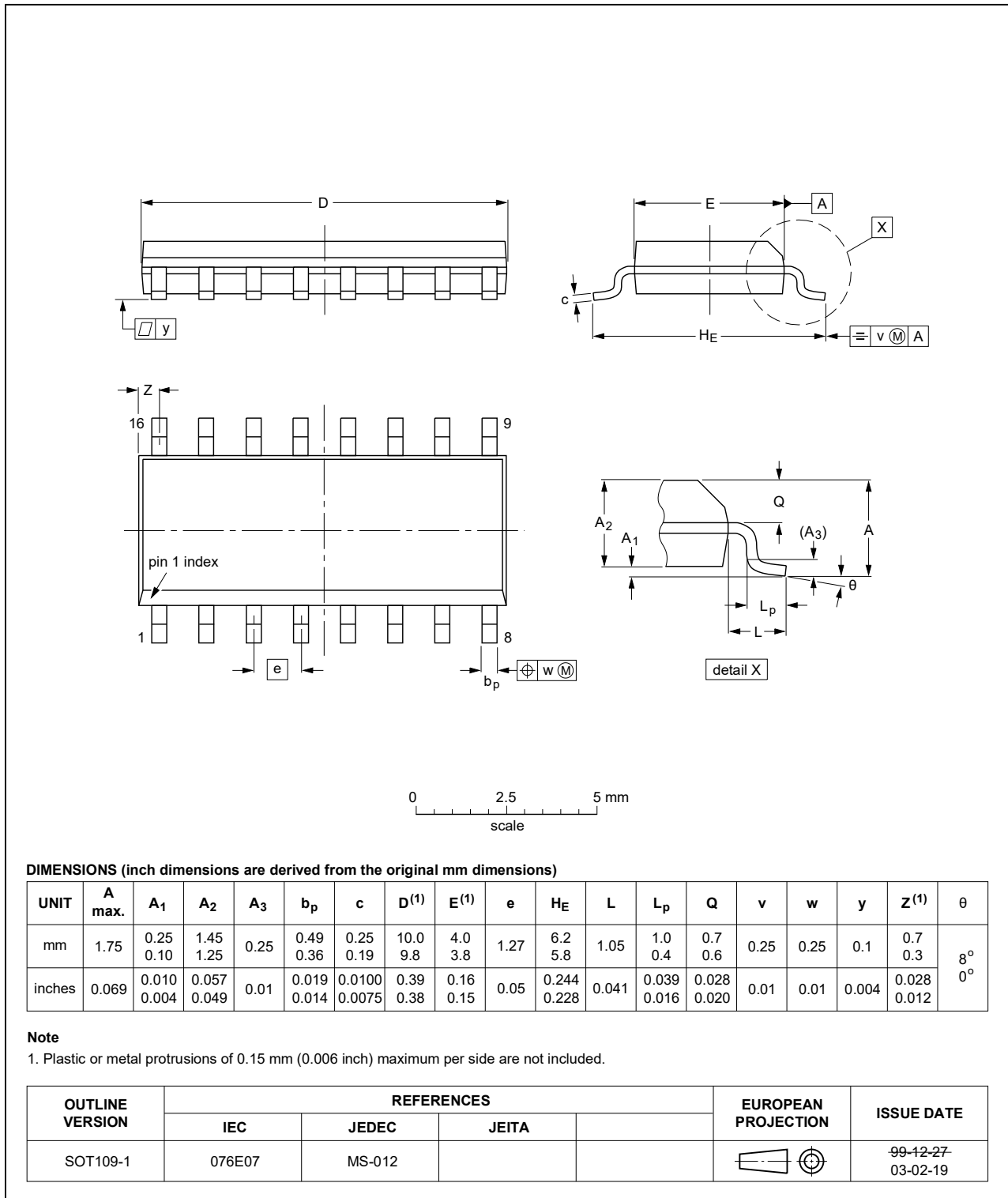


Fig. 8. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

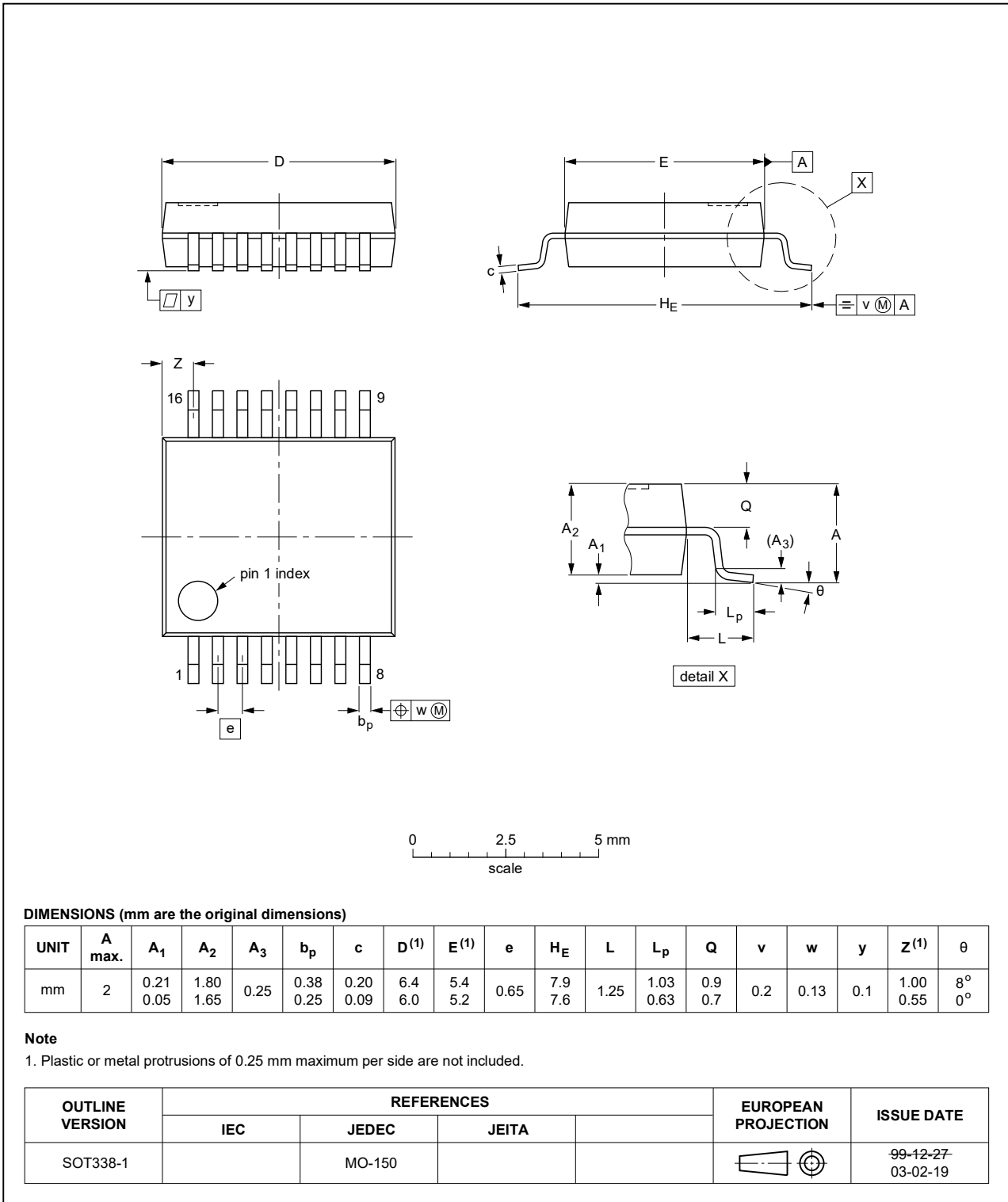


Fig. 9. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

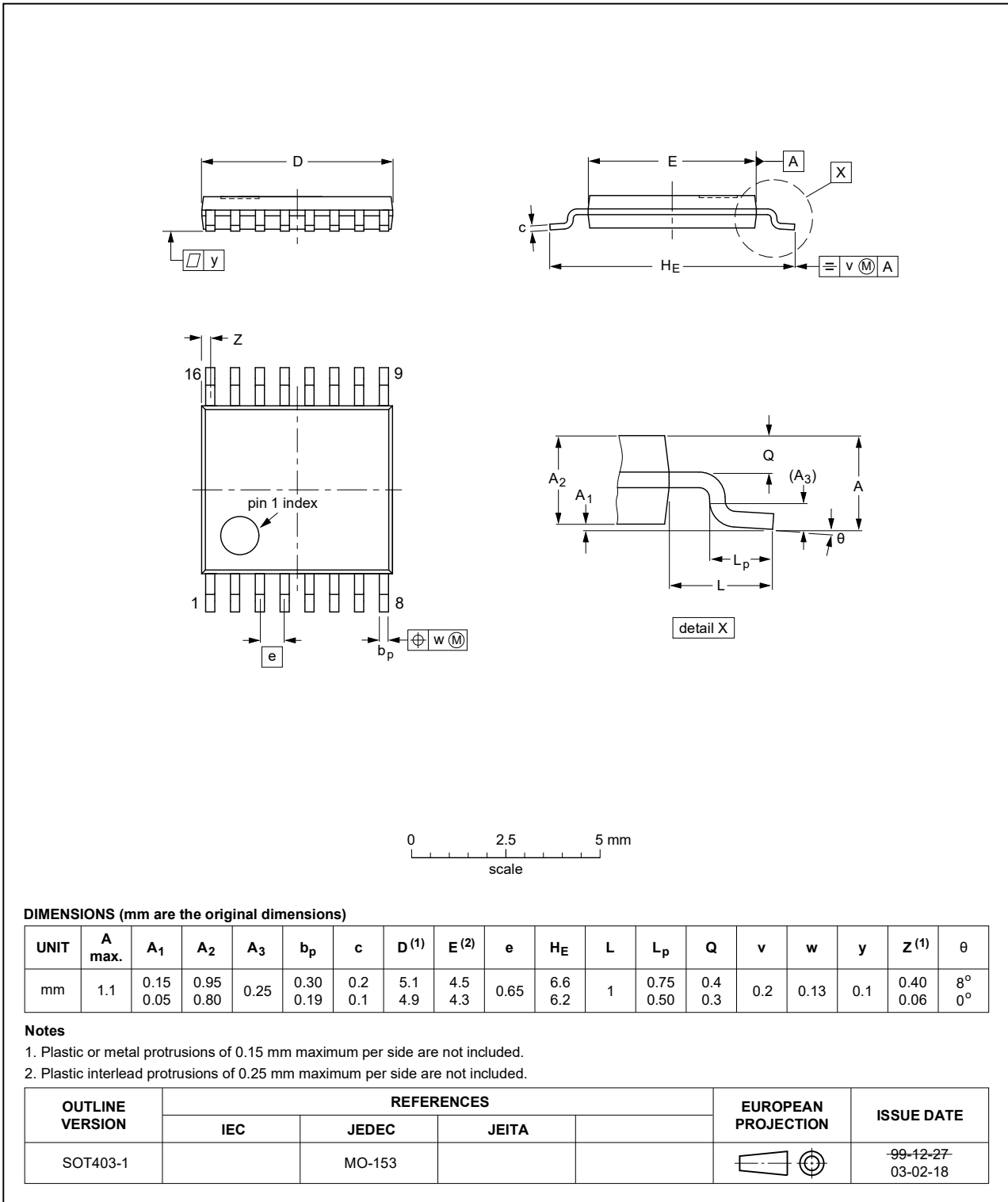


Fig. 10. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT151 v.8	20210318	Product data sheet	-	74HC_HCT151 v.7
Modifications:	<ul style="list-style-type: none"> Type number 74HC151DB (SOT338-1 / SSOP16) added. 			
74HC_HCT151 v.7	20210114	Product data sheet	-	74HC_HCT151 v.6
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC151DB and 74HCT151DB (SOT338-1 / SSOP16) removed. Section 7: Derating values for P_{tot} total power dissipation have been updated. 			
74HC_HCT151 v.6	20151228	Product data sheet	-	74HC_HCT151 v.5
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC151N and 74HCT151N (SOT38-4) removed. 			
74HC_HCT151 v.5	20150126	Product data sheet	-	74HC_HCT151 v.4
Modifications:	<ul style="list-style-type: none"> Table 7: Power dissipation capacitance condition for 74HCT151 is corrected. 			
74HC_HCT151 v.4	20130211	Product data sheet	-	74HC_HCT151 v.3
Modifications:	<ul style="list-style-type: none"> New descriptive title (errata). 			
74HC_HCT151 v.3	20120919	Product data sheet	-	74HC_HCT151_CNV v.2
74HC_HCT151_CNV v.2	19970827	Product specification	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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