

74HC251; 74HCT251

8-input multiplexer; 3-state

Rev. 6 — 8 February 2021

Product data sheet

1. General description

The 74HC251; 74HCT251 is an 8-bit multiplexer with eight binary inputs (I0 to I7), three select inputs (S0 to S2) and an output enable input (\overline{OE}). The select inputs select one of the eight binary inputs and route it to the complementary outputs (Y and \overline{Y}). A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC251: CMOS level
 - For 74HCT251: TTL level
- Non-inverting data path
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC251D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT251D				
74HC251PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT251PW				

4. Functional diagram

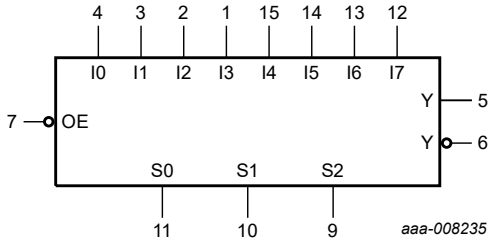


Fig. 1. Logic symbol

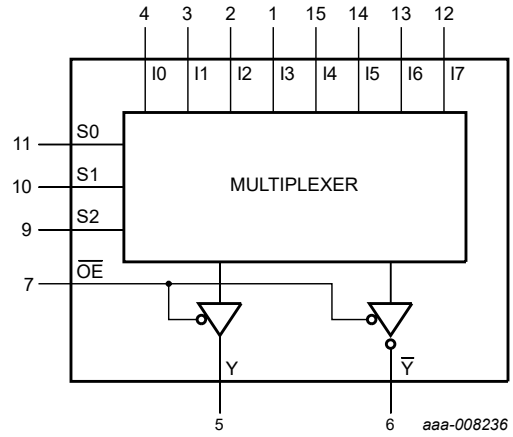


Fig. 2. Functional diagram

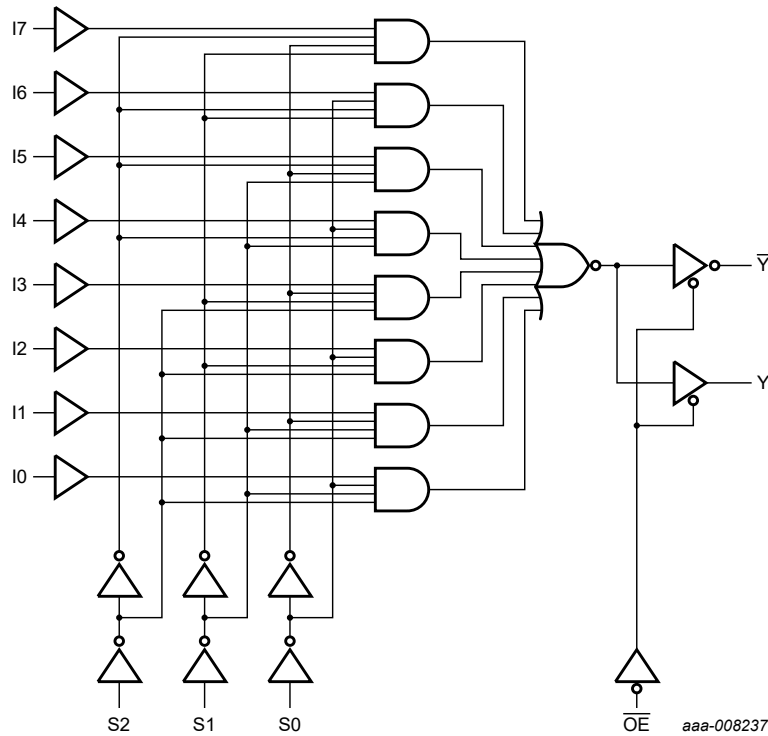
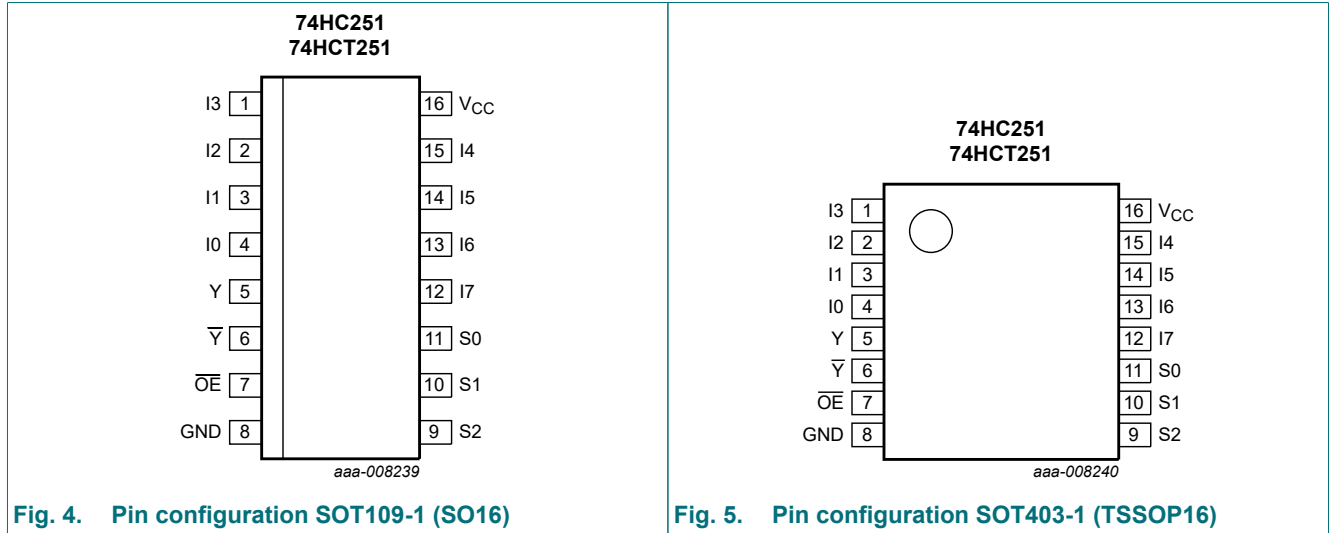


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
I0, I1, I2, I3, I4, I5, I6, I7	4, 3, 2, 1, 15, 14, 13, 12	data inputs
Y	5	multiplexer output
\bar{Y}	6	complementary multiplexer output
\overline{OE}	7	output enable input (active LOW)
GND	8	ground (0 V)
S0, S1, S2	11, 10, 9	common data select inputs
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input												Output	
OE	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	Y	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	[1]	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC251			74HCT251			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC251										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	± 0.1	-	± 1.0	-	± 1.0	μ A
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	± 0.5	-	± 5.0	-	± 10.0	μ A
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8.0	-	80	-	160	μ A
C_I	input capacitance		-	3.5	-					pF
74HCT251										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V								
		$I_O = -20$ μ A	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4$ mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V								
		$I_O = 20$ μ A	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0$ mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	± 0.1	-	± 1.0	-	± 1.0	μ A
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	± 0.5	-	± 5.0	-	± 10	μ A
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	μ A
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		per input pin; I_n inputs	-	100	360	-	450	-	490	μ A
		per input pin; \overline{OE} input	-	150	540	-	675	-	735	μ A
		per input pin; S_n input	-	150	540	-	675	-	735	μ A
C_I	input capacitance		-	3.5	-					pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

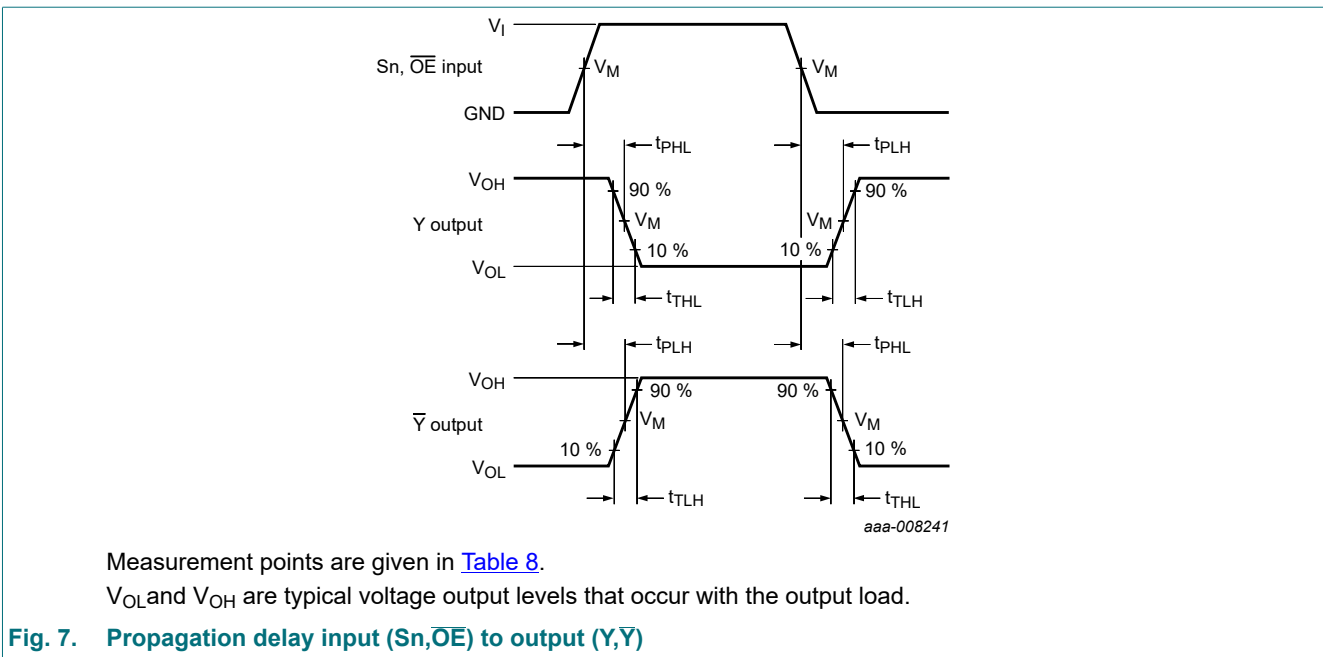
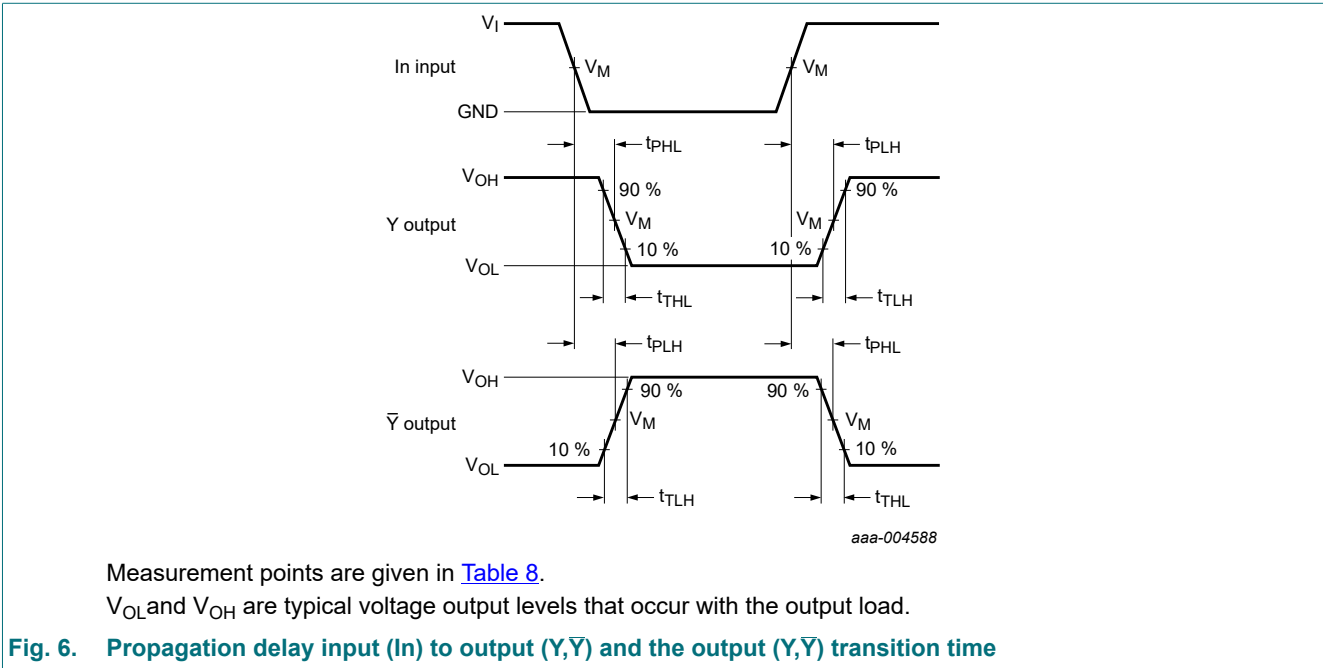
Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC251										
t_{pd}	propagation delay	In to Y; see Fig. 6 [1]								
		$V_{CC} = 2.0$ V	-	50	170	-	215	-	255	ns
		$V_{CC} = 4.5$ V	-	18	34	-	43	-	51	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	29	-	37	-	43	ns
		In to \bar{Y} ; see Fig. 6 [1]								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
		Sn to Y; see Fig. 7 [1]								
		$V_{CC} = 2.0$ V	-	66	205	-	255	-	310	ns
		$V_{CC} = 4.5$ V	-	24	41	-	51	-	62	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	20	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	19	35	-	43	-	53	ns
		Sn to \bar{Y} ; see Fig. 7 [1]								
$V_{CC} = 2.0$ V	-	69	205	-	255	-	310	ns		
$V_{CC} = 4.5$ V	-	25	41	-	51	-	62	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	21	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	20	35	-	43	-	53	ns		
t_{en}	enable time	\overline{OE} to Y, \bar{Y} ; see Fig. 8 [2]								
		$V_{CC} = 2.0$ V	-	36	140	-	175	-	210	ns
		$V_{CC} = 4.5$ V	-	13	28	-	35	-	42	ns
		$V_{CC} = 6.0$ V	-	10	24	-	30	-	36	ns
t_{dis}	disable time	\overline{OE} to Y, \bar{Y} ; see Fig. 8 [3]								
		$V_{CC} = 2.0$ V	-	39	140	-	170	-	210	ns
		$V_{CC} = 4.5$ V	-	14	28	-	35	-	42	ns
		$V_{CC} = 6.0$ V	-	11	24	-	30	-	36	ns
t_t	transition time	Y, \bar{Y} ; see Fig. 6 [4]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to V_{CC} [5]	-	44	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT251										
t_{pd}	propagation delay	In to Y; see Fig. 6 [1]								
		$V_{CC} = 4.5\text{ V}$	-	22	35	-	44	-	53	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	19	-	-	-	-	-	ns
		In to \bar{Y} ; see Fig. 6 [1]								
		$V_{CC} = 4.5\text{ V}$	-	22	35	-	44	-	53	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	19	-	-	-	-	-	ns
		Sn to Y; see Fig. 7 [1]								
		$V_{CC} = 4.5\text{ V}$	-	24	44	-	55	-	66	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	20	-	-	-	-	-	ns
		Sn to \bar{Y} ; see Fig. 7 [1]								
		$V_{CC} = 4.5\text{ V}$	-	25	44	-	55	-	66	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	21	-	-	-	-	-	ns
t_{en}	enable time	\overline{OE} to Y, \bar{Y} ; see Fig. 8 [2]								
		$V_{CC} = 4.5\text{ V}$	-	13	28	-	35	-	42	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	13	-	-	-	-	-	ns
t_{dis}	disable time	\overline{OE} to Y, \bar{Y} ; see Fig. 8 [3]								
		$V_{CC} = 4.5\text{ V}$	-	14	28	-	35	-	42	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	18	-	-	-	-	-	ns
t_t	transition time	Y, \bar{Y} ; see Fig. 6 [4]								
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	$C_L = 50\text{ pF}; f = 1\text{ MHz}; V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ [5]	-	46	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
 [2] t_{en} is the same as t_{PZH} and t_{PZL} .
 [3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .
 [4] t_t is the same as t_{THL} and t_{TLH} .
 [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



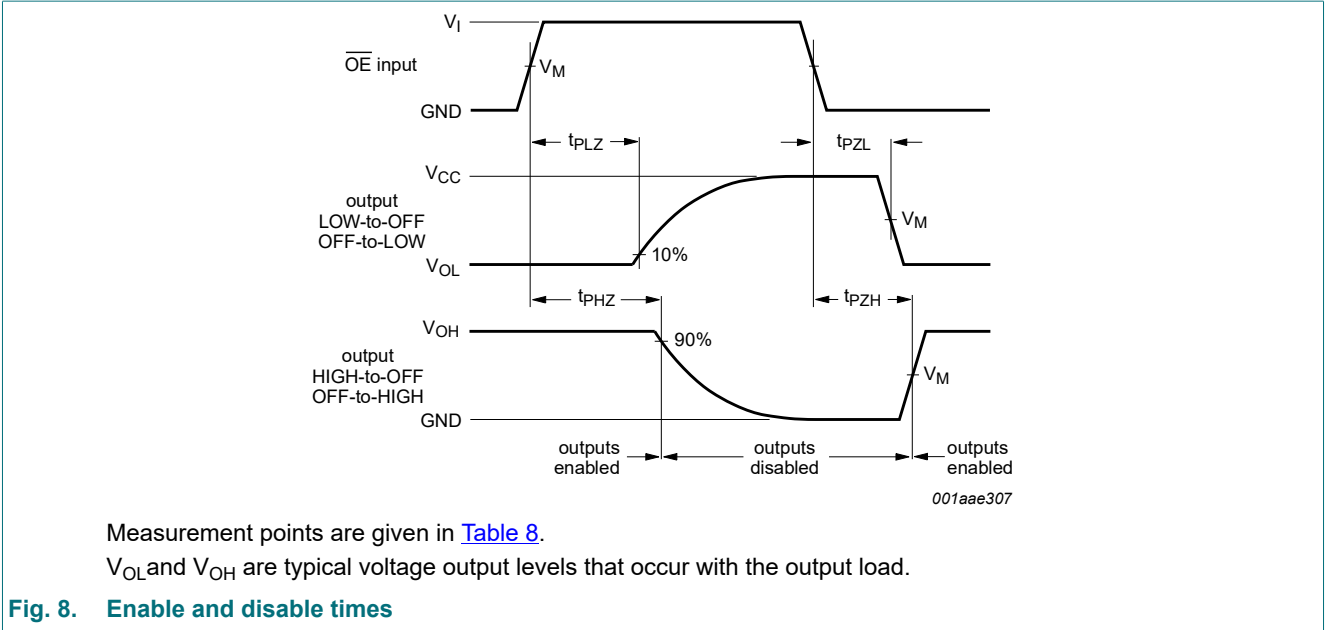


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC251	$0.5V_{CC}$	$0.5V_{CC}$
74HCT251	1.3 V	1.3 V

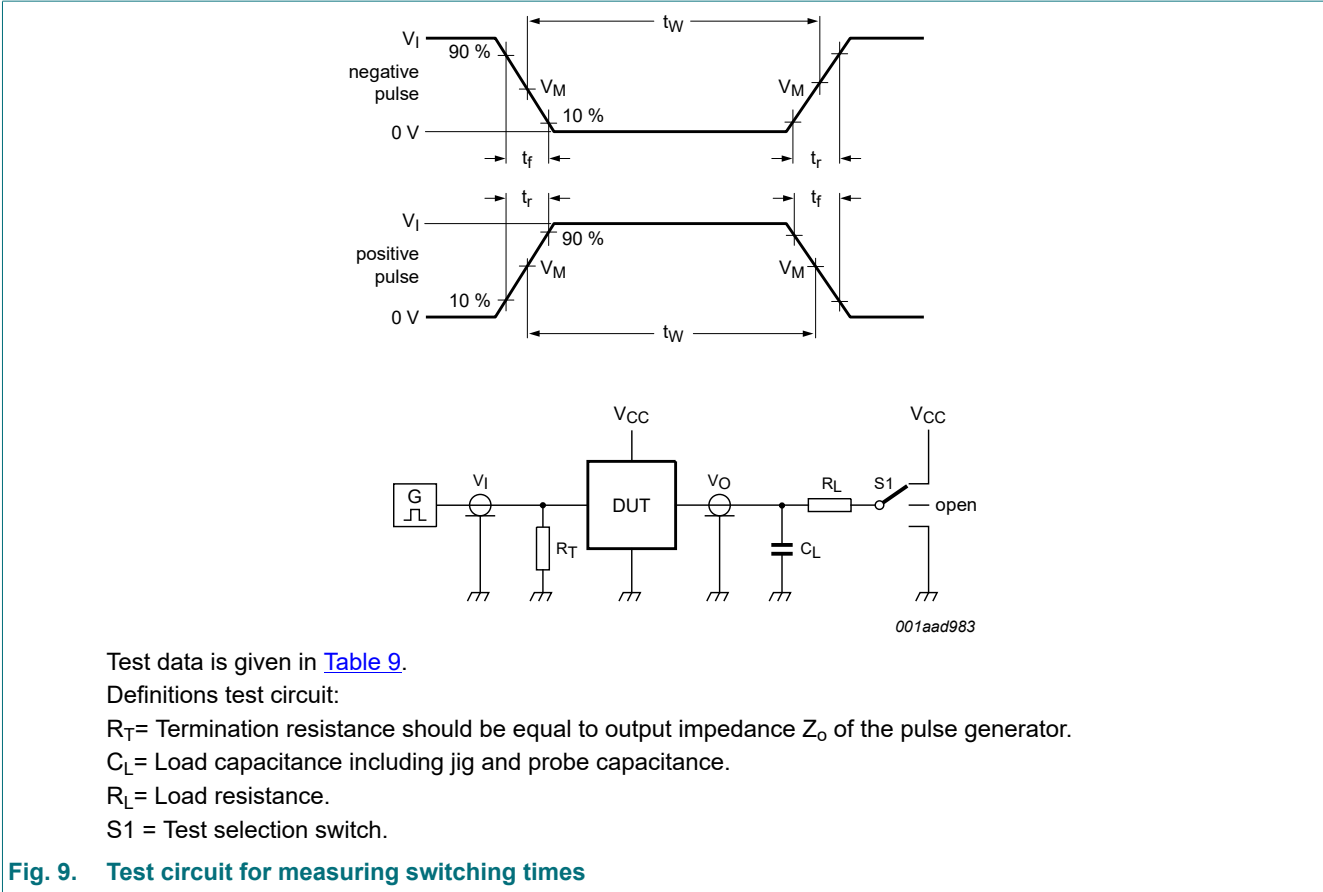


Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC251	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT251	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

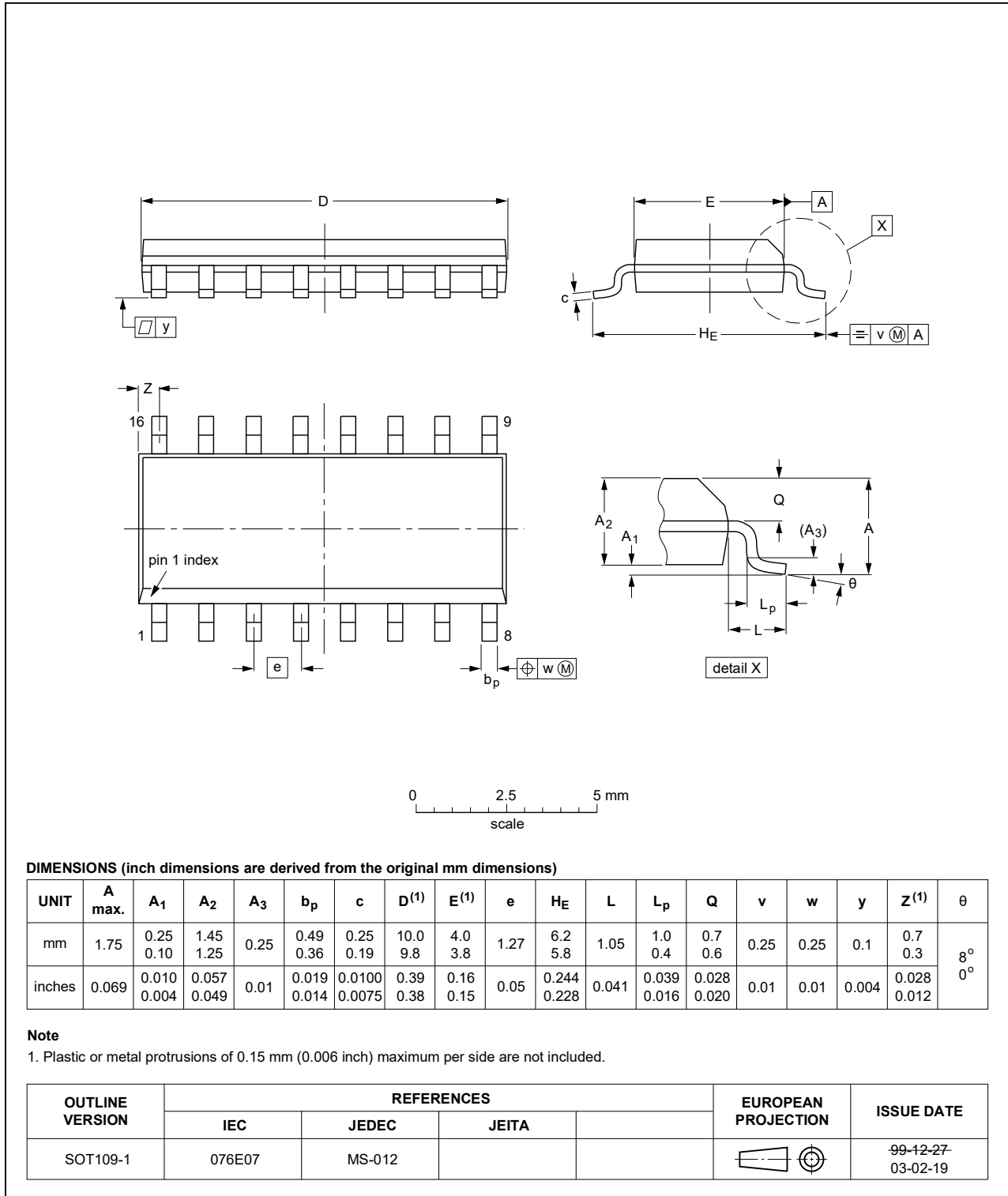


Fig. 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

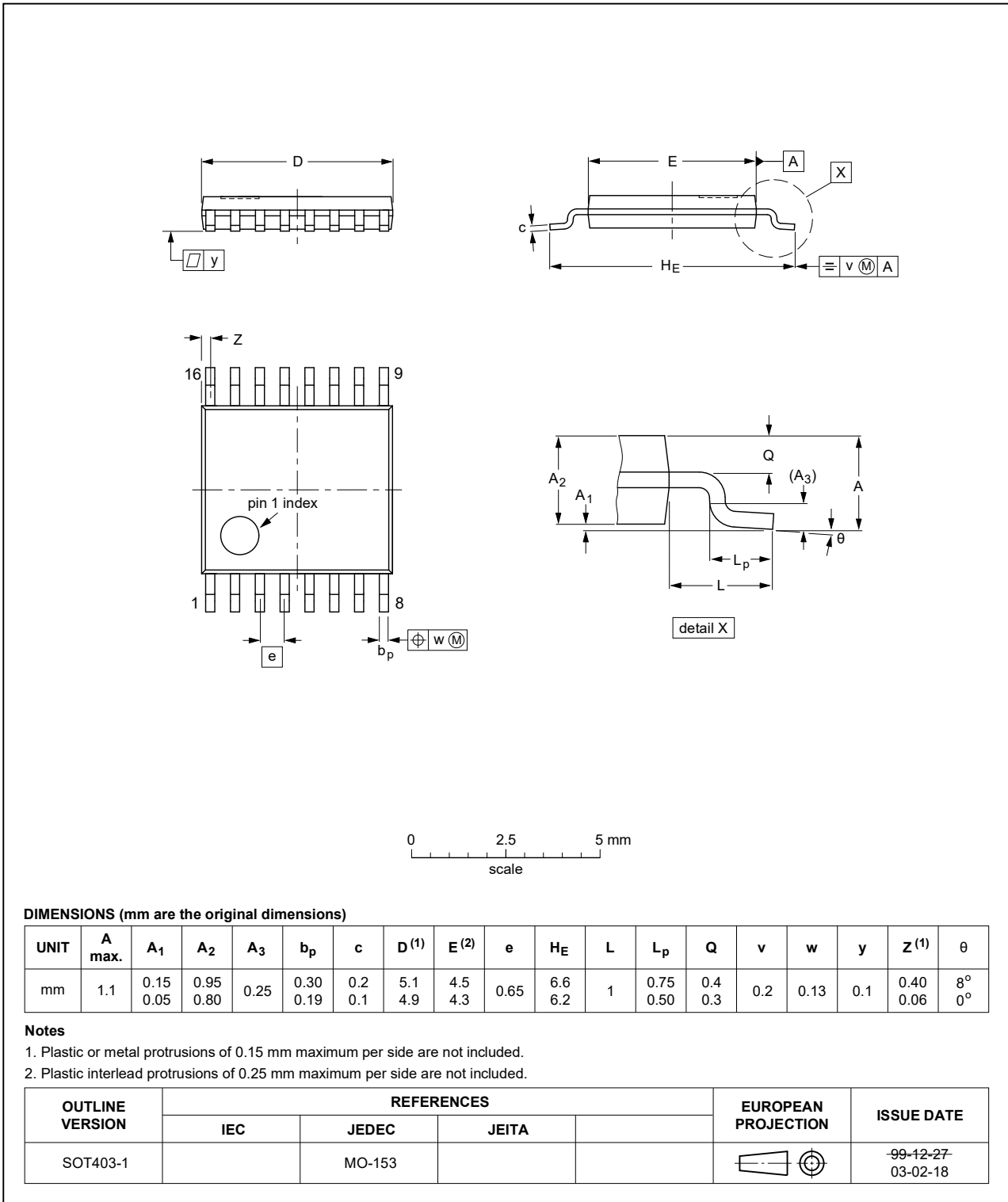


Fig. 11. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT251 v.6	20210208	Product data sheet	-	74HC_HCT251 v.5
Modifications:	<ul style="list-style-type: none"> • Section 2 updated. • Type numbers 74HC251DB and 74HCT251DB (SOT338-1 / SSOP16) removed. • Table 7: Conditions for C_{PD} have changed for 74HCT251. (errata) 			
74HC_HCT251 v.5	20190715	Product data sheet	-	74HC_HCT251 v.4
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 4: Derating values for P_{tot} total power dissipation have changed. 			
74HC_HCT251 v.4	20160201	Product data sheet	-	74HC_HCT251 v.3
Modifications:	<ul style="list-style-type: none"> • Type numbers 74HC251N and 74HCT251N (SOT38-4) removed. 			
74HC_HCT251 v.3	20130709	Product data sheet	-	74HC_HCT251_CNV v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT251_CNV v.2	19970828	Product specification	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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