74HC4351; 74HCT4351

8-channel analog multiplexer/demultiplexer with latch

Rev. 4 — 4 August 2021 **Product data sheet**

1. General description

The 74HC4351; 74HCT4351 is a single-pole octal-throw analog switch (SP8T) suitable for use in analog or digital 8:1 multiplexer/demultiplexer applications. The switch features three digital select inputs (S0 to S2), eight independent inputs/outputs (Yn), a common input/output (Z) and two digital enable inputs ($\overline{\text{E}}$1 and E2). With $\overline{\text{E}}$1 LOW and E2 HIGH, one of the eight switches is selected (low impedance ON-state) by S0 to S2. The data at the select inputs may be latched by using the latch enable input ($\overline{\text{LE}}$). When $\overline{\text{LE}}$ is HIGH the latch is transparent. When $\overline{\text{E}}$1 is HIGH or E2 is LOW all 8 analog switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide analog input voltage range from -5 V to +5 V
- Complies with JEDEC standard no. 7A
- Low ON resistance:
  - 80 Ω (typical) at V_{CC} - V_{EE} = 4.5 V
  - 70 Ω (typical) at V_{CC} - V_{EE} = 6.0 V
  - 60 Ω (typical) at V_{CC} - V_{EE} = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ±5 V analog signals
- Typical ‘break before make’ built-in
- Address latches provided
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4351D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT4351D				
74HC4351DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC4351PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

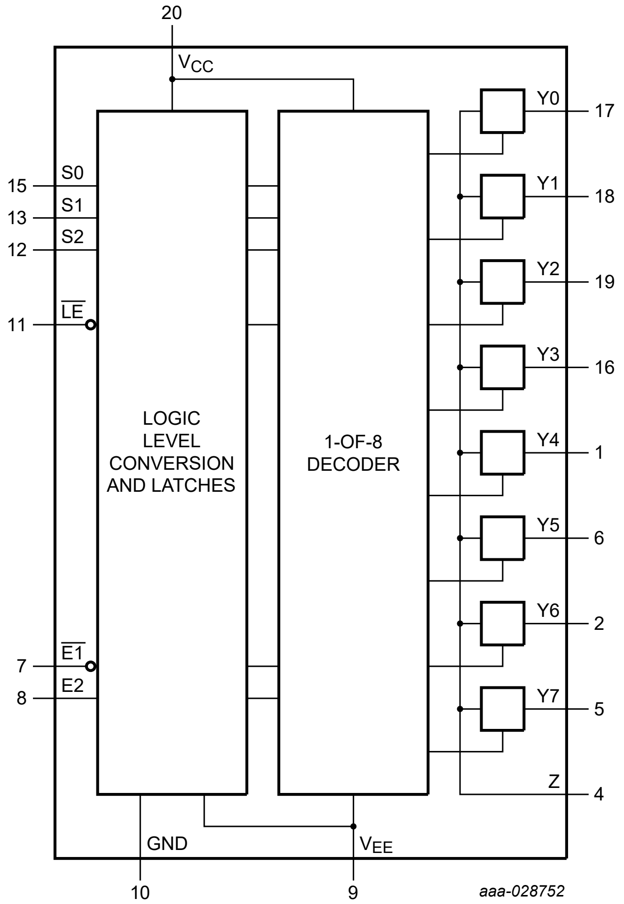


Fig. 1. Functional diagram

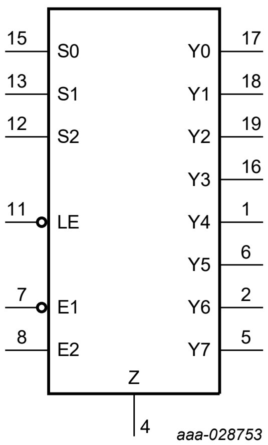


Fig. 2. Logic symbol

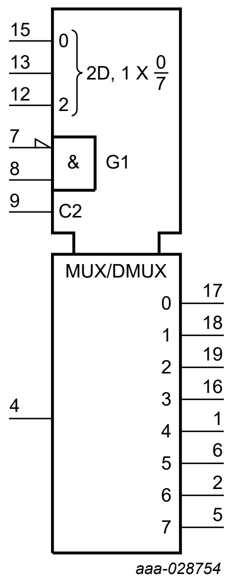


Fig. 3. IEC logic symbol

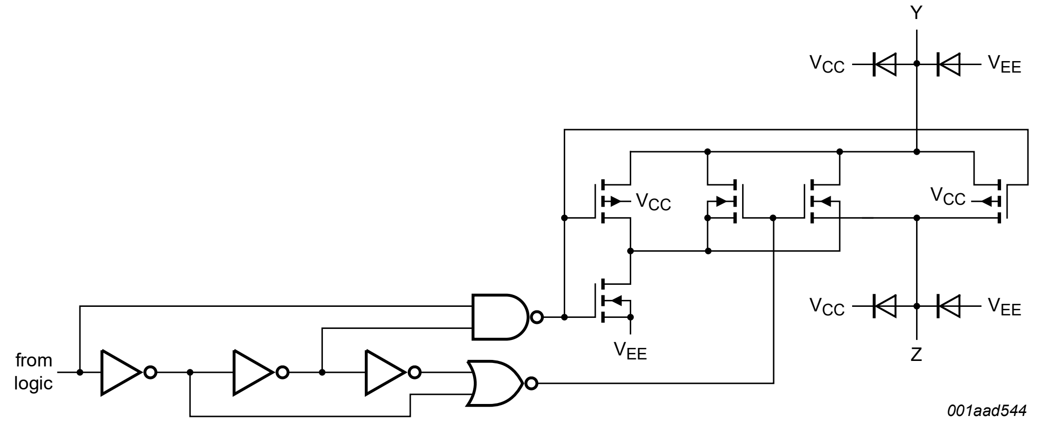


Fig. 4. Schematic diagram (one switch)

6. Pinning information

6.1. Pinning

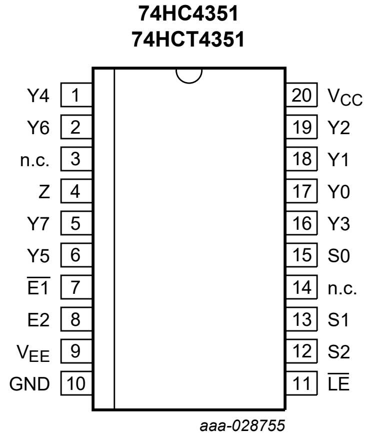


Fig. 5. Pin configuration SOT163-1 (SO20)

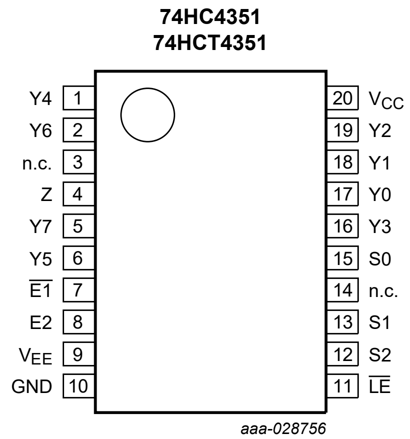


Fig. 6. Pin configuration SOT339-1 (SSOP20) and SOT360-1 (TSSOP20)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E1}$	7	enable input (active LOW)
E2	8	enable input (active HIGH)
$\overline{LE}$	11	latch enable input (active LOW)
S0, S1, S2	15, 13, 12	select inputs
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	17, 18, 19, 16, 1, 6, 2, 5	independent input or output
Z	4	common output or input
V_{EE}	9	supply voltage
GND	10	ground (0 V)
V_{CC}	20	supply voltage
n.c.	3, 14	not connected

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↓ = HIGH-to-LOW $\overline{LE}$ transition.

Input						Channel ON
$\overline{E1}$	E2	$\overline{LE}$	S2	S1	S0	
H	X	X	X	X	X	none
X	L	X	X	X	X	none
L	H	H	L	L	L	Y0
L	H	H	L	L	H	Y1
L	H	H	L	H	L	Y2
L	H	H	L	H	H	Y3
L	H	H	H	L	L	Y4
L	H	H	H	L	H	Y5
L	H	H	H	H	L	Y6
L	H	H	H	H	H	Y7
L	H	L	X	X	X	last selected channel "ON"
X	X	↓	X	X	X	select channels latched

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	[1]	-0.5	+11.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{SK}	switch clamping current	V_{SW} < -0.5 V or V_{SW} > V_{CC} + 0.5 V	-	±20	mA
I_{SW}	switch current	-0.5 V < V_{SW} < V_{CC} + 0.5 V	-	±25	mA
I_{EE}	supply current		-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	mW
P	power dissipation	per switch	-	100	mW

[1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows into terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Yn. In this case there is no limit for the voltage drop across the switch, but the voltages at Yn and Z may not exceed V_{CC} or V_{EE}.

[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT339-1 (SSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4351			74HCT4351			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage	see Fig. 7 and Fig. 8							
		V_{CC} - GND	2.0	5.0	10.0	4.5	5.0	5.5	V
		V_{CC} - V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	GND	-	V_{CC}	V
V_{SW}	switch voltage		V_{EE}	-	V_{CC}	V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
		V_{CC} = 10.0 V	-	-	31	-	-	-	ns/V

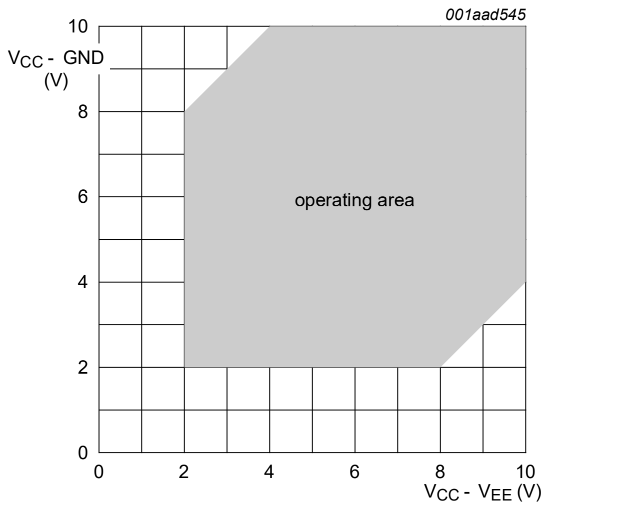


Fig. 7. Guaranteed operating area as a function of the supply voltages for 74HC4351

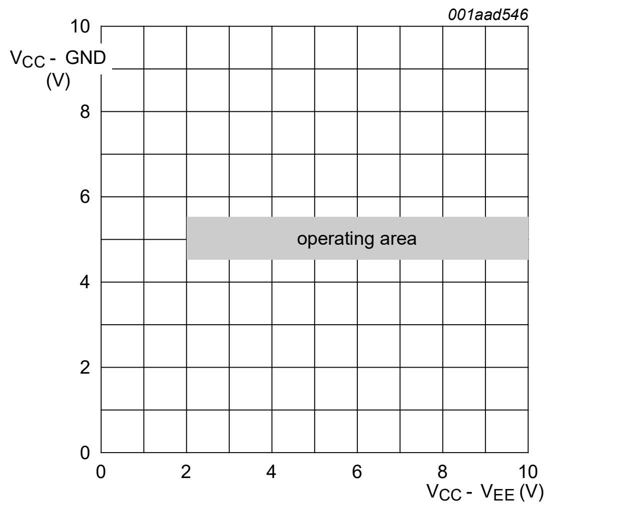


Fig. 8. Guaranteed operating area as a function of the supply voltages for 74HCT4351

10. Static characteristics

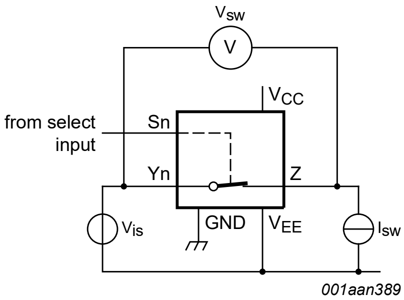
Table 6. R_{ON} resistance per latch for 74HC4351 and 74HCT4351

For test circuit, see Fig. 9

For 74HC4351: $V_I = V_{IH}$ or V_{IL}; V_{CC} - GND or V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.
For 74HCT4351: $V_I = V_{IH}$ or V_{IL}; V_{CC} - GND = 4.5 V and 5.5 V, V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to V_{EE} [1]								
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA [2]	-	-	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA	-	100	180	-	225	-	270	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA	-	90	160	-	200	-	240	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA	-	70	130	-	165	-	195	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$ [1]								
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA [2]	-	150	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA	-	80	140	-	175	-	210	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA	-	70	120	-	150	-	180	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA	-	60	105	-	130	-	160	Ω
		$V_{is} = V_{CC}$ [1]								
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA [2]	-	150	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA	-	90	160	-	200	-	240	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA	-	80	140	-	175	-	210	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA	-	65	120	-	150	-	180	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to V_{EE} [1]								
		V_{CC} = 2.0 V; V_{EE} = 0 V [2]	-	-	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	9	-	-	-	-	-	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	8	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	6	-	-	-	-	-	Ω

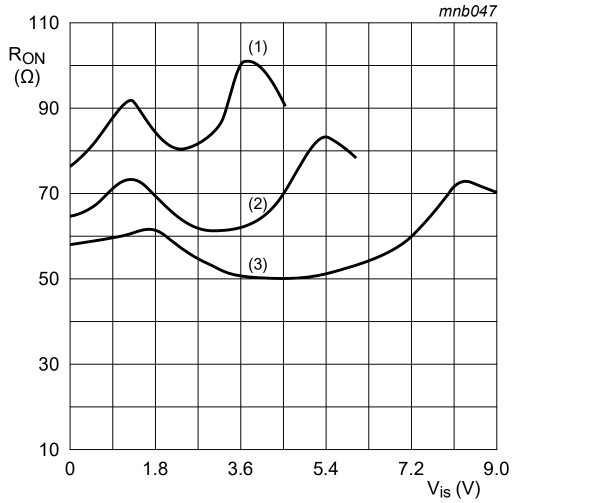
[1] V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
[2] When supply voltages (V_{CC} - V_{EE}) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.



V_{is} = 0 V to (V_{CC} - V_{EE})

$$R_{ON} = \frac{V_{sw}}{I_{sw}}$$

Fig. 9. Test circuit for measuring R_{ON}



V_{is} = 0 V to (V_{CC} - V_{EE})

(1) V_{CC} = 4.5 V

(2) V_{CC} = 6 V

(3) V_{CC} = 9 V

Fig. 10. Typical R_{ON} as a function of input voltage V_{is}

Table 7. Static characteristics

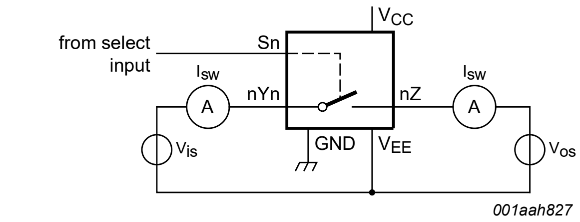
Voltages are referenced to GND (ground = 0 V);

V_{is} is the input voltage at pins Yn or Z, whichever is assigned as an input;

V_{os} is the output voltage at pins Z or Yn, whichever is assigned as an output.

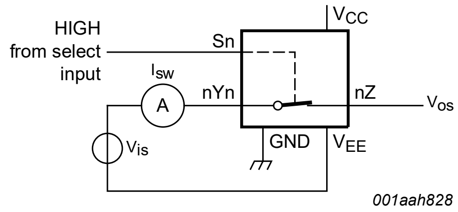
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4351										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
		V_{CC} = 9.0 V	6.3	4.7	-	6.3	-	6.3	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
		V_{CC} = 9.0 V	-	4.3	2.7	-	2.7	-	2.7	V
I_I	input leakage current	V_{EE} = 0 V; V_I = V_{CC} or GND								
		V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
		V_{CC} = 10.0 V	-	-	±0.2	-	±2.0	-	±2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 11								
		per channel	-	-	±0.1	-	±1.0	-	±1.0	μA
		all channels	-	-	±0.4	-	±4.0	-	±4.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 12	-	-	±0.4	-	±4.0	-	±4.0	μA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	V_{EE} = 0 V; V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}								
		V_{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	µA
		V_{CC} = 10.0 V	-	-	16.0	-	160.0	-	320.0	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
C_{sw}	switch capacitance	independent pins Yn	-	5	-	-	-	-	-	pF
		common pins Z	-	25	-	-	-	-	-	pF
74HCT4351										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 11								
		per channel	-	-	±0.1	-	±1.0	-	±1.0	µA
		all channels	-	-	±0.4	-	±4.0	-	±4.0	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 12	-	-	±0.4	-	±4.0	-	±4.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}								
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	8.0	-	80.0	-	160.0	µA
		V_{CC} = 5.0 V; V_{EE} = -5.0 V	-	-	16.0	-	160.0	-	320.0	µA
ΔI_{CC}	additional supply current	per input; other inputs at V_{CC} or GND; V_I = V_{CC} - 2.1 V; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V								
		inputs $\overline{E1}$, E2 and Sn	-	50	180	-	225	-	245	µA
		input $\overline{LE}$	-	150	540	-	675	-	735	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
C_{sw}	switch capacitance	independent pins Yn	-	5	-	-	-	-	-	pF
		common pins Z	-	25	-	-	-	-	-	pF



$V_{is} = V_{CC}$ and $V_{os} = V_{EE}$ or
$V_{is} = V_{EE}$ and $V_{os} = V_{CC}$

Fig. 11. Test circuit for measuring OFF-state current



$V_{is} = V_{CC}$ and V_{os} = open-circuit or
$V_{is} = V_{EE}$ and V_{os} = open-circuit

Fig. 12. Test circuit for measuring ON-state current

11. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; for test circuit see Fig. 16.
V_{is} is the input voltage at pins Yn or Z, whichever is assigned as an input;
V_{os} is the output voltage at pins Z or Yn, whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4351										
t_{pd}	propagation delay	V_{is} to V_{os}; R_L = ∞ Ω; see Fig. 13 [1]								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	4	10	-	13	-	15	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	4	8	-	10	-	12	ns
t_{on}	turn-ON time	$\overline{E1}$ to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	85	300	-	375	-	450	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	31	60	-	75	-	90	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	25	51	-	64	-	77	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	28	55	-	69	-	83	ns
		E2 to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	85	300	-	375	-	450	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	31	60	-	75	-	90	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	25	51	-	64	-	77	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	25	55	-	69	-	83	ns
		$\overline{LE}$ to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	91	300	-	375	-	450	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	33	60	-	75	-	90	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	26	51	-	64	-	77	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	27	55	-	69	-	83	ns
		Sn to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	88	300	-	375	-	450	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	32	60	-	75	-	90	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	26	51	-	64	-	77	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	25	50	-	63	-	75	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{off}	turn-OFF time	$\overline{E1}$ to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	69	250	-	315	-	375	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	25	50	-	63	-	75	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	20	43	-	54	-	64	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	20	40	-	50	-	60	ns
		E2 to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	72	250	-	315	-	375	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	26	50	-	63	-	75	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	21	43	-	54	-	64	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	19	40	-	50	-	60	ns
		$\overline{LE}$ to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	83	275	-	345	-	415	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	30	55	-	69	-	83	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	24	47	-	59	-	71	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	26	45	-	56	-	68	ns
		Sn to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	80	275	-	345	-	415	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	29	55	-	69	-	83	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	23	47	-	59	-	71	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	24	48	-	60	-	72	ns
t_{su}	set-up time	Sn to $\overline{LE}$; R_L = 1 kΩ; see Fig. 15								
		V_{CC} = 2.0 V; V_{EE} = 0 V	60	17	-	-	75	-	90	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	12	6	-	-	15	-	18	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	10	5	-	-	13	-	15	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	18	9	-	-	23	-	27	ns
t_{hold}	hold time	Sn to $\overline{LE}$; R_L = 1 kΩ; see Fig. 15								
		V_{CC} = 2.0 V; V_{EE} = 0 V	5	-8	-	-	5	-	5	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	5	-3	-	-	5	-	5	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	5	-2	-	-	5	-	5	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	5	-4	-	-	5	-	5	ns
$t_{WH(min)}$	minimum pulse width HIGH	$\overline{LE}$; R_L = 1 kΩ; see Fig. 15								
		V_{CC} = 2.0 V; V_{EE} = 0 V	100	11	-	-	125	-	150	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	20	1	-	-	25	-	30	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	17	3	-	-	21	-	26	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	25	7	-	-	31	-	38	ns
C_{pd}	power dissipation capacitance	per switch; V_I = GND to V_{CC} [2]	-	25	-	-	-	-	-	pF
C_{sw}	switch capacitance	maximum								
		independent (Yn)	-	5	-	-	-	-	-	pF
		common (Z)	-	25	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4351										
t_{pd}	propagation delay	V_{is} to V_{os}; $R_L = \infty\ \Omega$; see Fig. 13 [1]								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	6	12	-	15	-	18	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	4	8	-	10	-	12	ns
t_{on}	turn-ON time	$\overline{E1}$ to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	40	75	-	94	-	113	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	31	60	-	75	-	90	ns
		E2 to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	35	70	-	88	-	105	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	26	50	-	63	-	75	ns
		$\overline{LE}$ to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	42	75	-	94	-	113	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	37	60	-	75	-	90	ns
		Sn to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	39	75	-	94	-	113	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	30	60	-	75	-	90	ns
t_{off}	turn-OFF time	$\overline{E1}$ to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	27	55	-	69	-	83	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	20	40	-	50	-	60	ns
		E2 to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	32	60	-	75	-	90	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	26	50	-	63	-	75	ns
		$\overline{LE}$ to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	33	60	-	75	-	90	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	30	55	-	69	-	83	ns
		Sn to V_{os}; R_L = 1 kΩ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	33	65	-	81	-	98	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	29	55	-	69	-	83	ns
t_{su}	set-up time	Sn to $\overline{LE}$; R_L = 1 kΩ; see Fig. 15								
		V_{CC} = 4.5 V; V_{EE} = 0 V	12	6	-	-	15	-	18	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	14	7	-	-	18	-	21	ns
t_{hold}	hold time	Sn to $\overline{LE}$; R_L = 1 kΩ; see Fig. 15								
		V_{CC} = 4.5 V; V_{EE} = 0 V	5	-1	-	-	5	-	5	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	5	-2	-	-	5	-	5	ns
$t_{WH(min)}$	minimum pulse width HIGH	$\overline{LE}$; R_L = 1 kΩ; see Fig. 15								
		V_{CC} = 4.5 V; V_{EE} = 0 V	25	13	-	-	31	-	38	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	25	13	-	-	31	-	38	ns
C_{pd}	power dissipation capacitance	per switch; V_I = GND to V_{CC} - 1.5 V [2]	-	25	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{sw}	switch capacitance	maximum								
		independent (Yn)	-	5	-	-	-	-	-	pF
		common (Z)	-	25	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma\{(C_L + C_{sw}) \times V_{CC}{}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
N = number of inputs switching;
$\Sigma\{(C_L + C_{sw}) \times V_{CC}{}^2 \times f_o\}$ = sum of outputs;
C_L = output load capacitance in pF;
C_{sw} = switch capacitance in pF;
V_{CC} = supply voltage in V.

11.1. Waveforms and test circuit

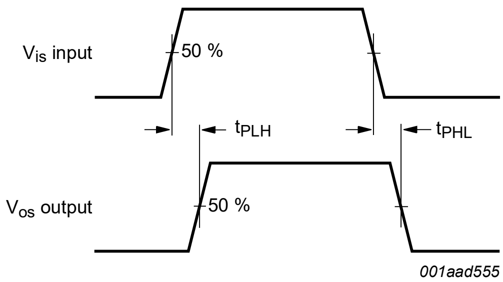
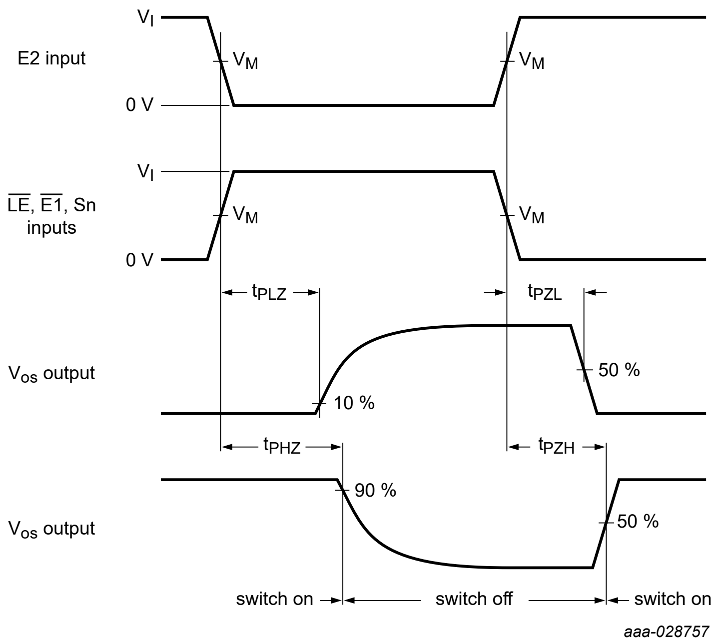
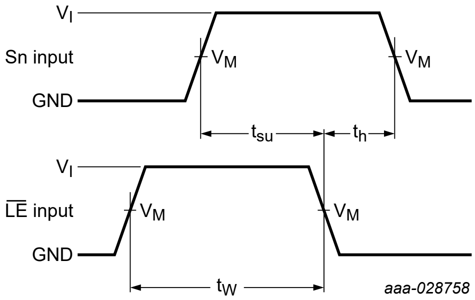


Fig. 13. Input (V_{is}) to output (V_{os}) propagation delays



Measurement points are given in Table 9

Fig. 14. Turn-ON and turn-OFF times

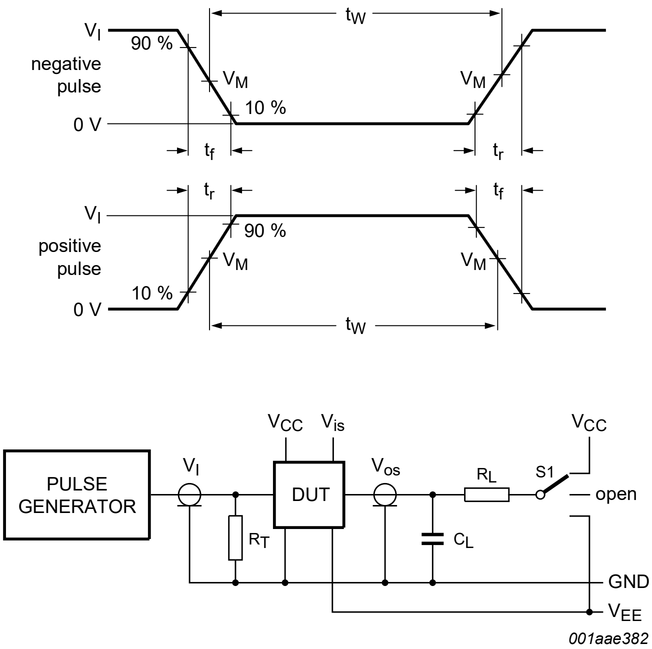


Measurement points are given in Table 9

Fig. 15. Set-up and hold times from Sn inputs to $\overline{LE}$ input, and minimum pulse width of $\overline{LE}$.

Table 9. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC4351	GND to V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}
74HCT4351	GND to 3 V	1.3 V	1.3 V



Definitions for test circuit; see Table 10:

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig. 16. Test circuit for measuring switching times

Table 10. Test data

Test	Input				Load		S1 position
	V_I	V_{is}	t_r, t_f		C_L	R_L	
			at f_{max}	other [1]			
t_{PZH}, t_{PHZ}	[2]	V_{CC}	< 2 ns	6 ns	50 pF	1 kΩ	V_{EE}
t_{PZL}, t_{PLZ}	[2]	V_{EE}	< 2 ns	6 ns	50 pF	1 kΩ	V_{CC}
Other	[2]	pulse	< 2 ns	6 ns	50 pF	1 kΩ	open

[1] $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

[2] V_I values:
For 74HC4351: $V_I = V_{CC}$
For 74HCT4351: $V_I = 3$ V

11.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C; C_L = 50 pF unless stated otherwise.
V_{is} is the input voltage at pins Yn or Z, whichever is assigned as an input.
V_{os} is the output voltage at pins Yn or Z, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d_{sin}	sine-wave distortion	f_i = 1 kHz; R_L = 10 kΩ; see Fig. 17				
		V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	0.04	-	%
		V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	0.02	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see Fig. 17				
		V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	0.12	-	%
		V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	0.06	-	%
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; f_i = 1 MHz; see Fig. 18				
		V_{CC} = 2.25 V; V_{EE} = -2.25 V [1]	-	-50	-	dB
		V_{CC} = 4.5 V; V_{EE} = -4.5 V [1]	-	-50	-	dB
V_{ct}	crosstalk voltage	between control and any switch (peak-to-peak value); R_L = 600 Ω; f_i = 1 MHz; $\overline{E1}$, E2 or Sn square wave between V_{CC} and GND; t_r = t_f = 6 ns; see Fig. 19				
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	120	-	mV
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	220	-	mV
$f_{(-3dB)}$	-3 dB frequency response	R_L = 50 Ω; C_L = 10 pF see Fig. 20				
		V_{CC} = 2.25 V; V_{EE} = -2.25 V [2]	-	160	-	MHz
		V_{CC} = 4.5 V; V_{EE} = -4.5 V [2]	-	170	-	MHz

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

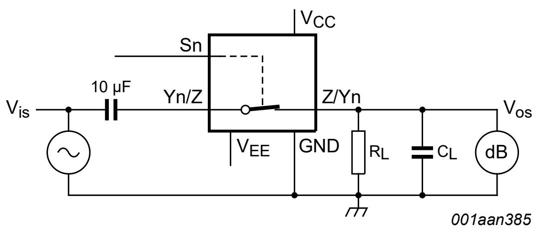
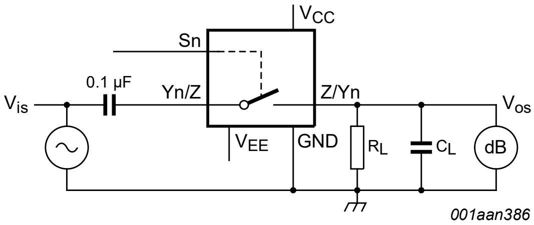
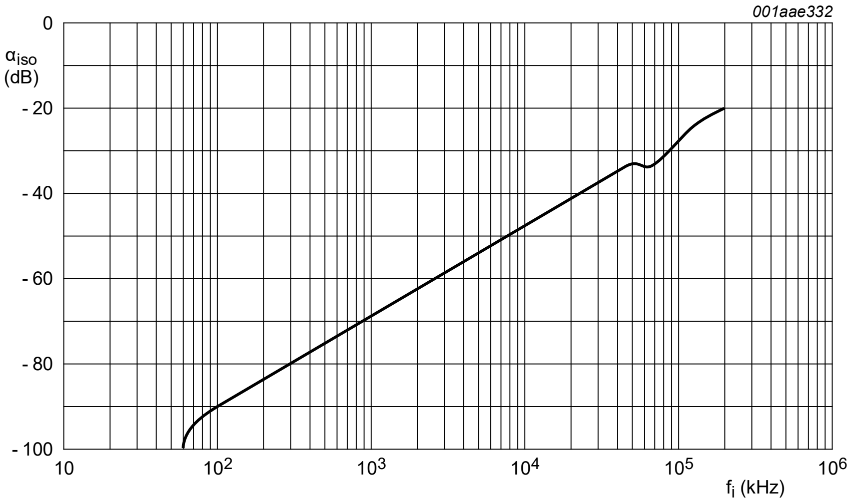


Fig. 17. Test circuit for measuring sine-wave distortion



V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 600 Ω; R_S = 1 kΩ

a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Fig. 18. Test circuit for measuring isolation (OFF-state)

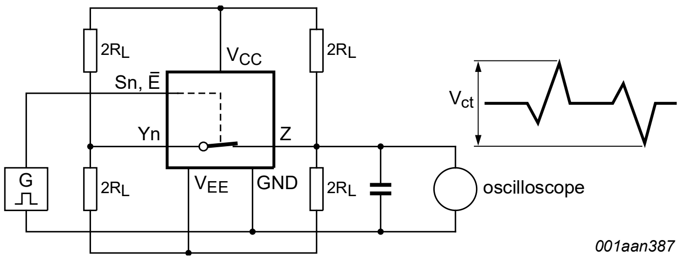
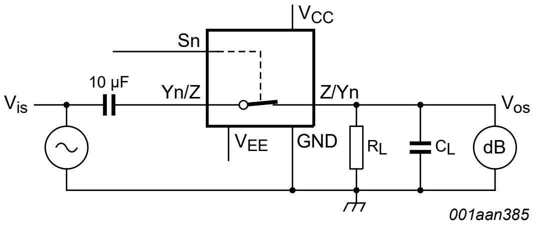
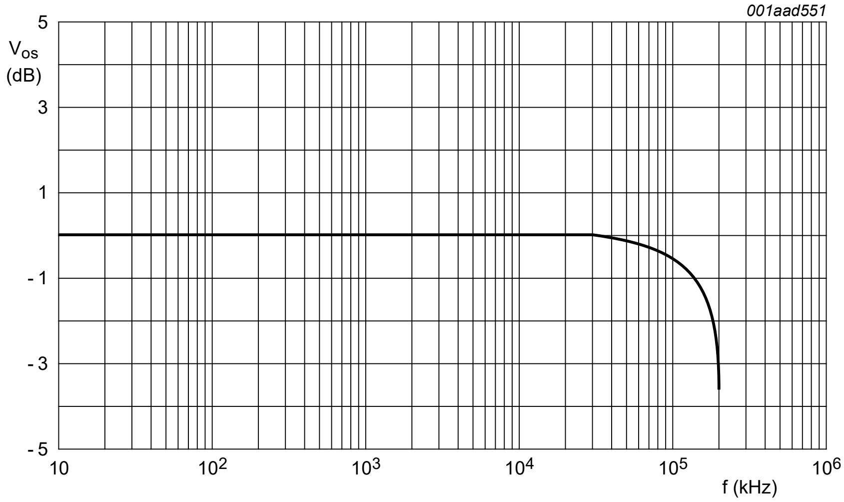


Fig. 19. Test circuit for measuring crosstalk between control input and any switch



V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 50 Ω; R_S = 1 kΩ

a. Test circuit

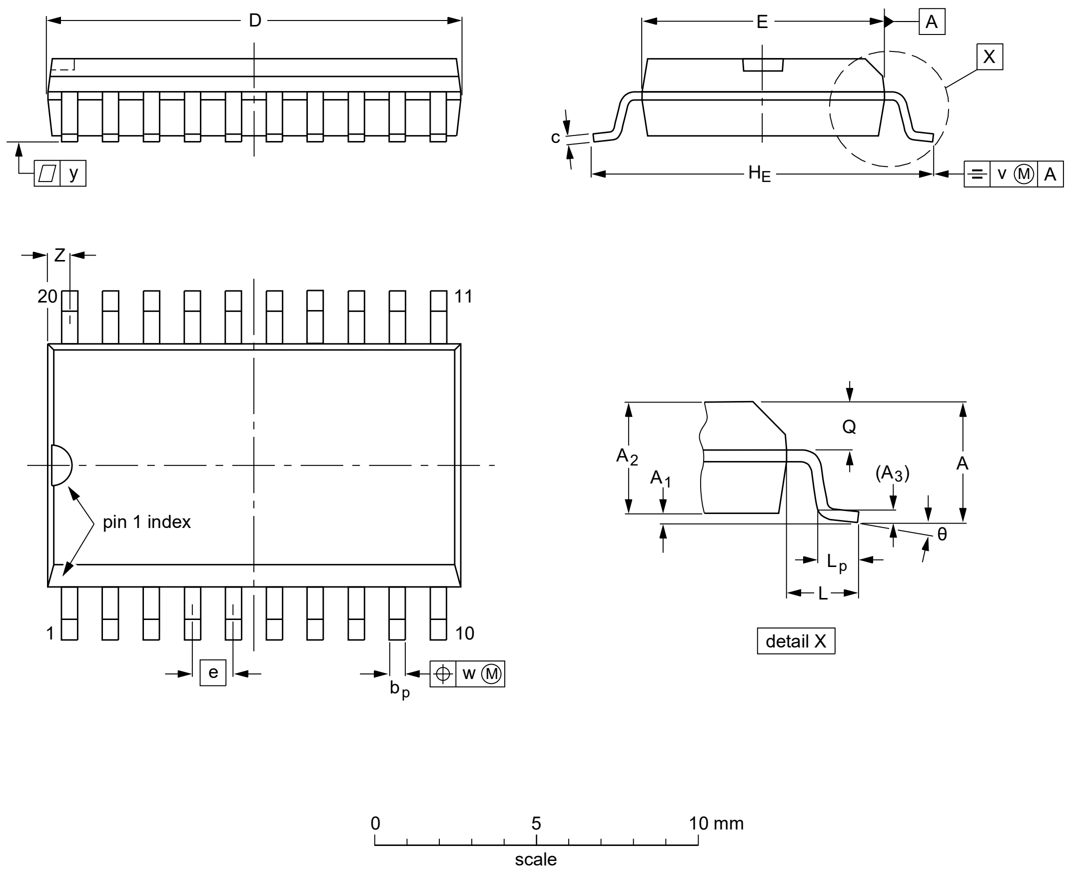


b. Typical frequency response

Fig. 20. Test circuit for frequency response

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

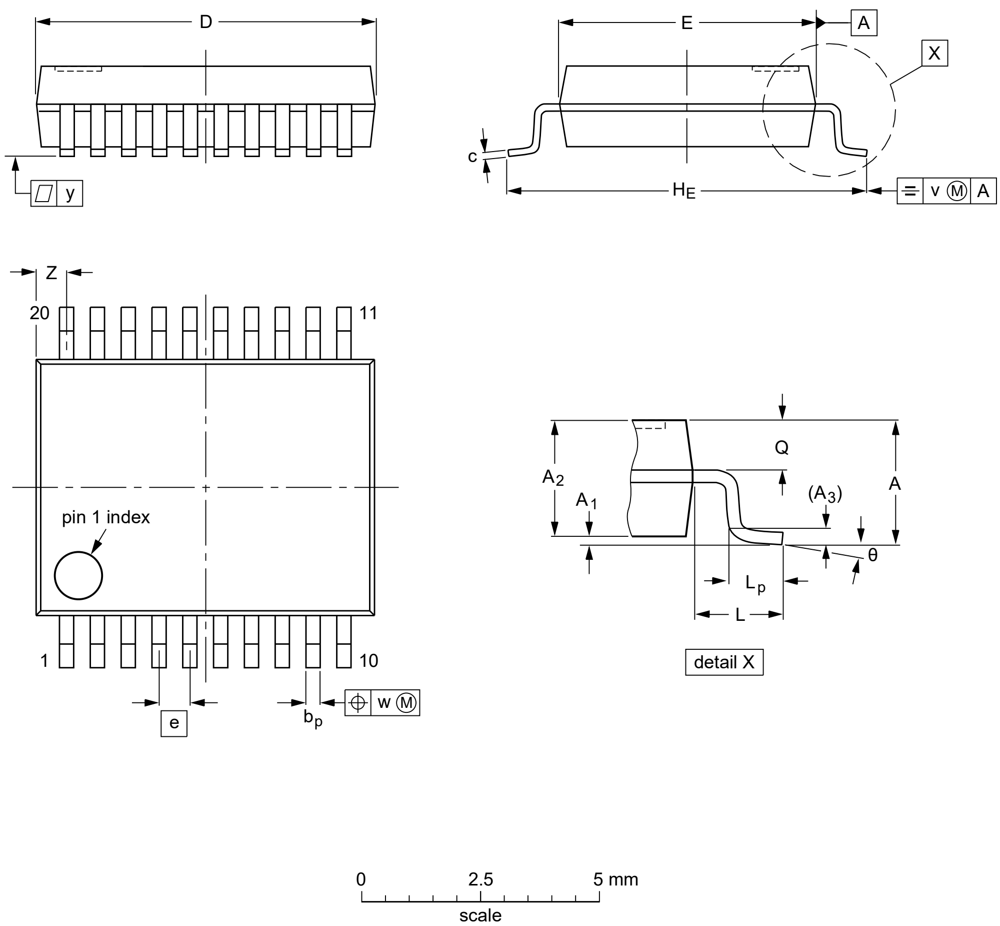
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 21. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

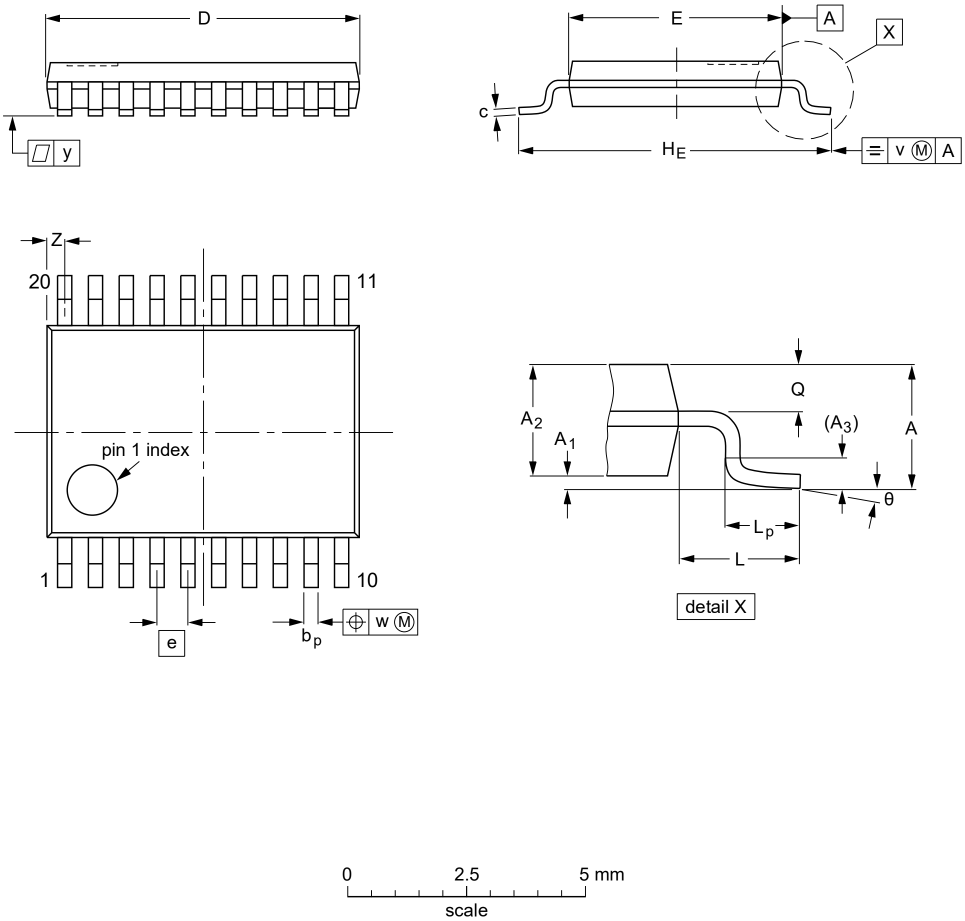
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 22. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 23. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4351 v.4	20210804	Product data sheet	-	74HC_HCT4351 v.3
Modifications:	• Type number 74HC4351PW (SOT360-1/TSSOP20) added. • Type number 74HCT4351DB (SOT339-1/SSOP20) removed. • Section 8: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT4351 v.3	20180709	Product data sheet	-	74HC_HCT4351 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC4351N (SOT146-1) and 74HCT4351N (SOT146-1) removed.			
74HC_HCT4351 v.2	19901201	Product specification	-	74HC_HCT4351 v.1

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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