

# 74HC574; 74HCT574

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 8 — 30 July 2021

Product data sheet

## 1. General description

The 74HC574; 74HCT574 is an 8-bit positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable ( $\overline{OE}$ ) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For 74HC574: CMOS level
  - For 74HCT574: TTL level
- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC574D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT574D				
74HC574PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT574PW				

### 4. Functional diagram

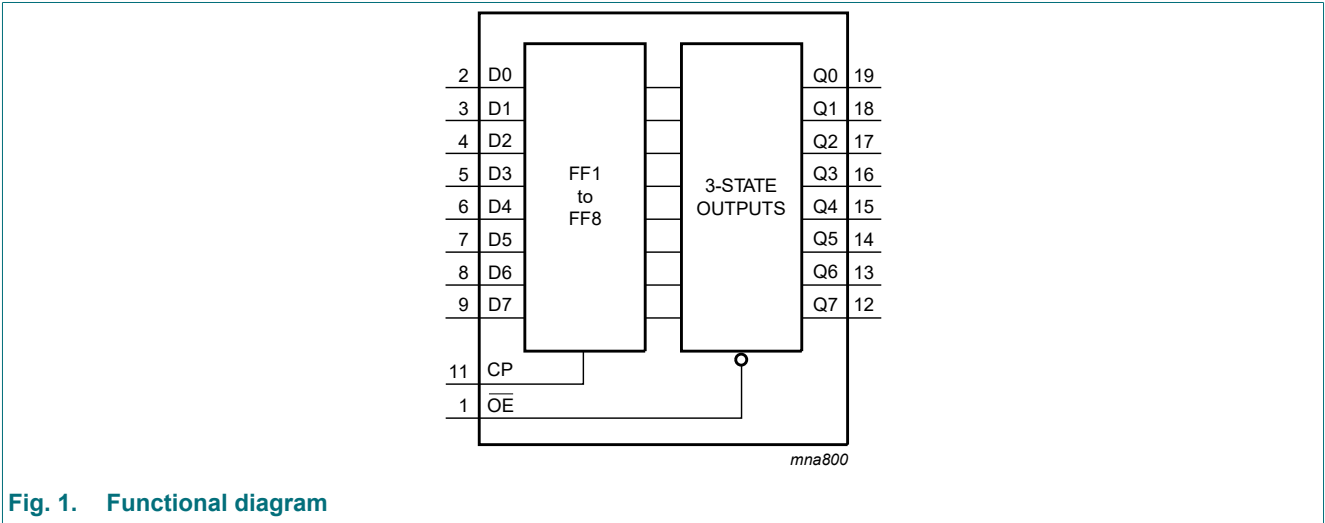


Fig. 1. Functional diagram

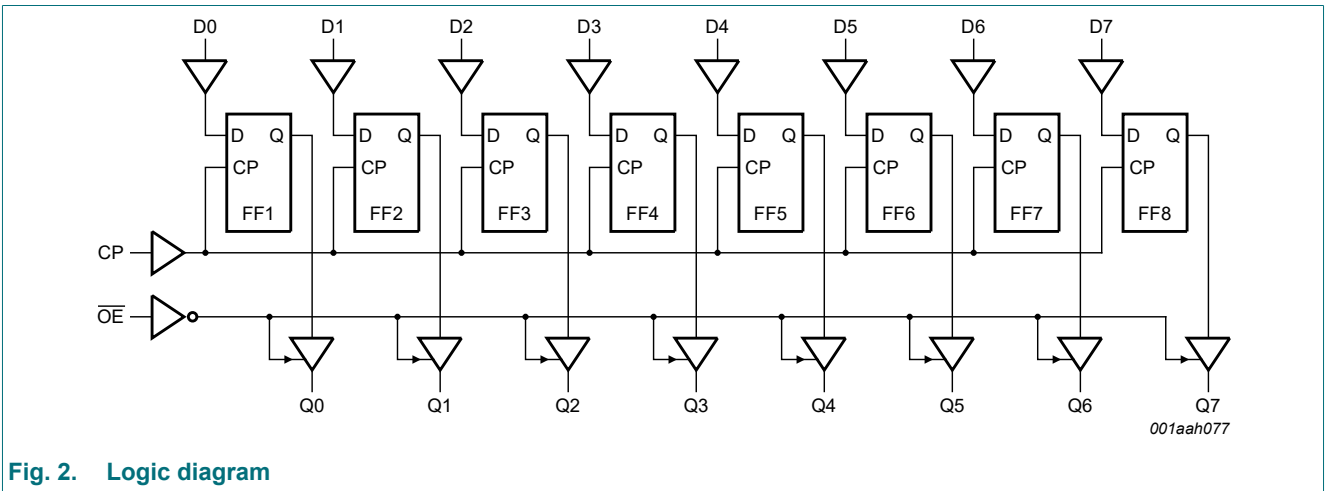


Fig. 2. Logic diagram

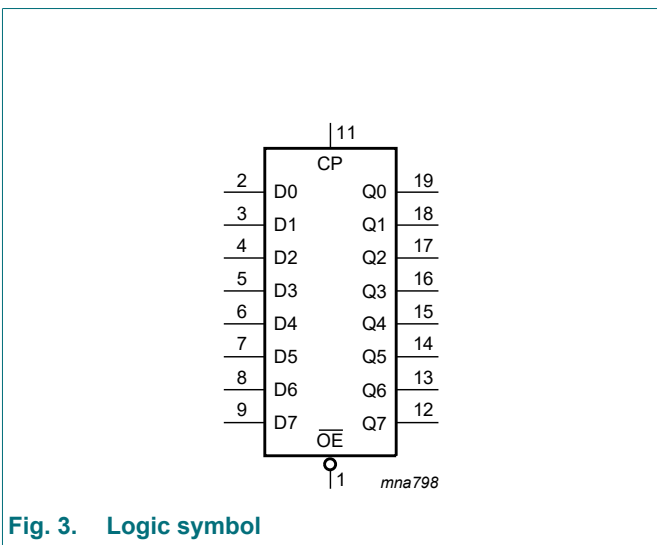


Fig. 3. Logic symbol

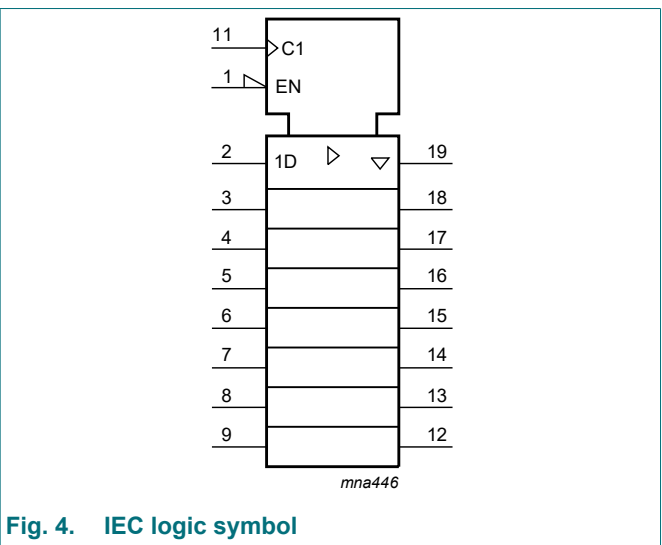


Fig. 4. IEC logic symbol

## 5. Pinning information

### 5.1. Pinning

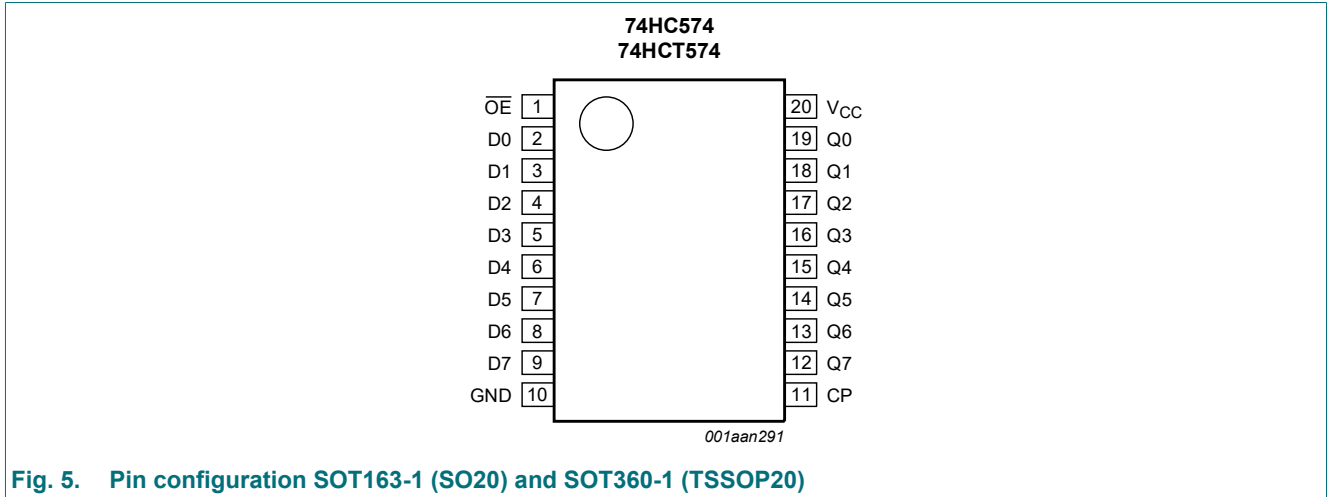


Fig. 5. Pin configuration SOT163-1 (SO20) and SOT360-1 (TSSOP20)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data inputs
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop outputs
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one setup time prior to the HIGH-to-LOW CP transition;

L = LOW voltage level; l = LOW voltage level one setup time prior to the HIGH-to-LOW CP transition;

Z = high-impedance OFF-state;  $\uparrow$  = LOW-to-HIGH clock transition.

Operating mode	Input			Internal flip-flop	Output
	$\overline{OE}$	CP	Dn		Qn
Load and read register	L	$\uparrow$	l	L	L
	L	$\uparrow$	h	H	H
Load register and disable output	H	$\uparrow$	l	L	Z
	H	$\uparrow$	h	H	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	$\pm 35$	mA
$I_{CC}$	supply current		-	+70	mA
$I_{GND}$	ground current		-	-70	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	[1]	-	500	mW

- [1] For SOT163-1 (SO20) package:  $P_{tot}$  derates linearly with 12.3 mW/K above 109 °C.  
For SOT360-1 (TSSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC574			74HCT574			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC574</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

## Octal D-type flip-flop; positive edge-trigger; 3-state

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -7.8 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 6.0 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±0.5	-	±5.0	-	±10.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT574</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±0.5	-	±5.0	-	±10	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		per input pin; Dn inputs	-	50	180	-	225	-	245	µA
		per input pin; $\overline{OE}$ input	-	125	450	-	563	-	613	µA
		per input pin; CP input	-	150	540	-	675	-	735	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC574</b>										
$t_{pd}$	propagation delay	CP to Qn; see Fig. 6 [1]								
		$V_{CC} = 2.0$ V	-	47	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	17	30	-	35	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
$t_{en}$	enable time	OE to Qn; see Fig. 8 [2]								
		$V_{CC} = 2.0$ V	-	44	140	-	175	-	210	ns
		$V_{CC} = 4.5$ V	-	16	28	-	35	-	42	ns
		$V_{CC} = 6.0$ V	-	13	24	-	30	-	36	ns
$t_{dis}$	disable time	OE to Qn; see Fig. 8 [3]								
		$V_{CC} = 2.0$ V	-	39	125	-	155	-	190	ns
		$V_{CC} = 4.5$ V	-	14	25	-	31	-	38	ns
		$V_{CC} = 6.0$ V	-	11	21	-	26	-	32	ns
$t_t$	transition time	Qn; see Fig. 6 [4]								
		$V_{CC} = 2.0$ V	-	14	60	-	75	-	90	ns
		$V_{CC} = 4.5$ V	-	5	12	-	15	-	18	ns
		$V_{CC} = 6.0$ V	-	4	10	-	13	-	15	ns
$t_W$	pulse width	CP HIGH or LOW; see Fig. 7								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
$t_{su}$	set-up time	Dn to CP; see Fig. 7								
		$V_{CC} = 2.0$ V	60	6	-	75	-	90	-	ns
		$V_{CC} = 4.5$ V	12	2	-	15	-	18	-	ns
		$V_{CC} = 6.0$ V	10	2	-	13	-	15	-	ns
$t_h$	hold time	Dn to CP; see Fig. 7								
		$V_{CC} = 2.0$ V	5	0	-	5	-	5	-	ns
		$V_{CC} = 4.5$ V	5	0	-	5	-	5	-	ns
		$V_{CC} = 6.0$ V	5	0	-	5	-	5	-	ns
$f_{max}$	maximum frequency	CP; see Fig. 6								
		$V_{CC} = 2.0$ V	6.0	37	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5$ V	30	112	-	24	-	20	-	MHz
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	123	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V	35	133	-	28	-	24	-	MHz
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ [5]	-	22	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT574</b>										
t <sub>pd</sub>	propagation delay	CP to Qn; see Fig. 6 [1]								
		V <sub>CC</sub> = 4.5 V	-	18	33	-	41	-	50	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	15	-	-	-	-	-	ns
t <sub>en</sub>	enable time	OE to Qn; see Fig. 8 [2]								
		V <sub>CC</sub> = 4.5 V	-	19	33	-	41	-	50	ns
t <sub>dis</sub>	disable time	OE to Qn; see Fig. 8 [3]								
		V <sub>CC</sub> = 4.5 V	-	16	28	-	35	-	42	ns
t <sub>t</sub>	transition time	Qn; see Fig. 6 [4]								
		V <sub>CC</sub> = 4.5 V	-	5	12	-	15	-	18	ns
t <sub>w</sub>	pulse width	CP HIGH or LOW; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	16	7	-	20	-	24	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	12	3	-	15	-	18	-	ns
t <sub>h</sub>	hold time	Dn to CP; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	5	-1	-	5	-	5	-	ns
f <sub>max</sub>	maximum frequency	CP; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	30	69	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	76	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V [5]	-	25	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[2] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.

[3] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[4] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

[5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

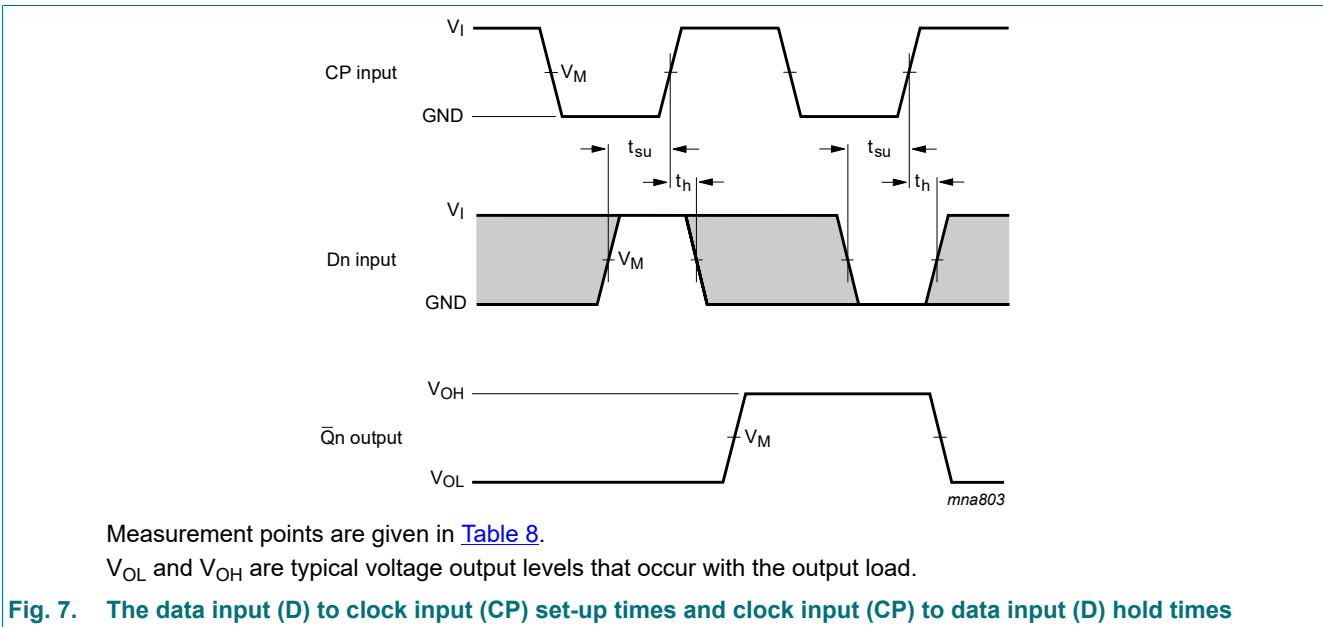
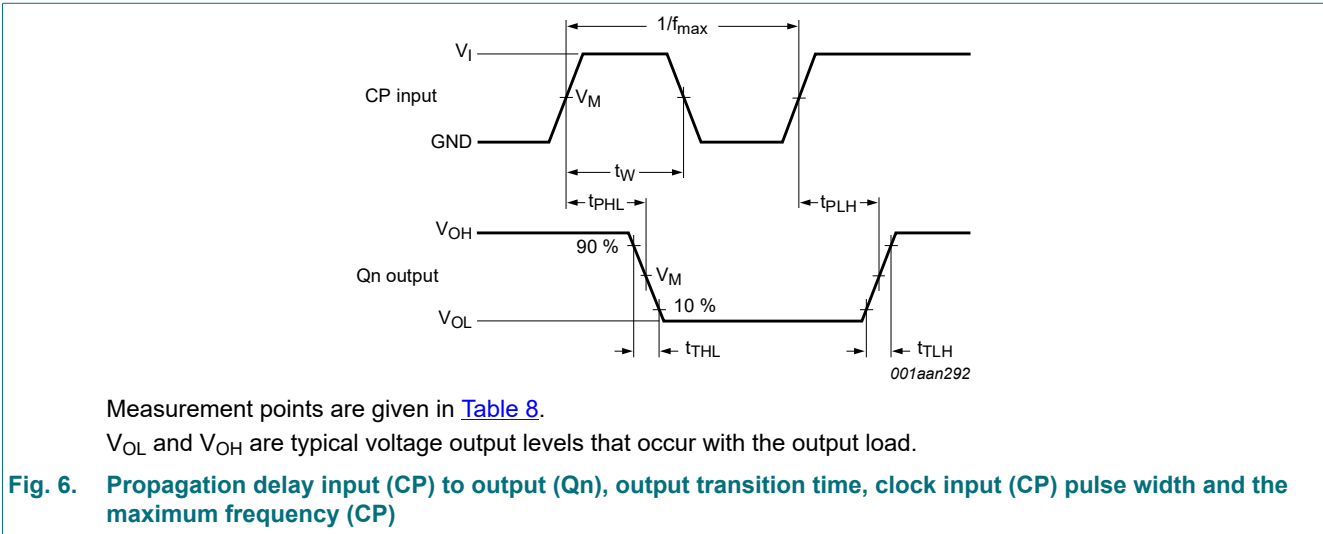
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

10.1. Waveforms and test circuit





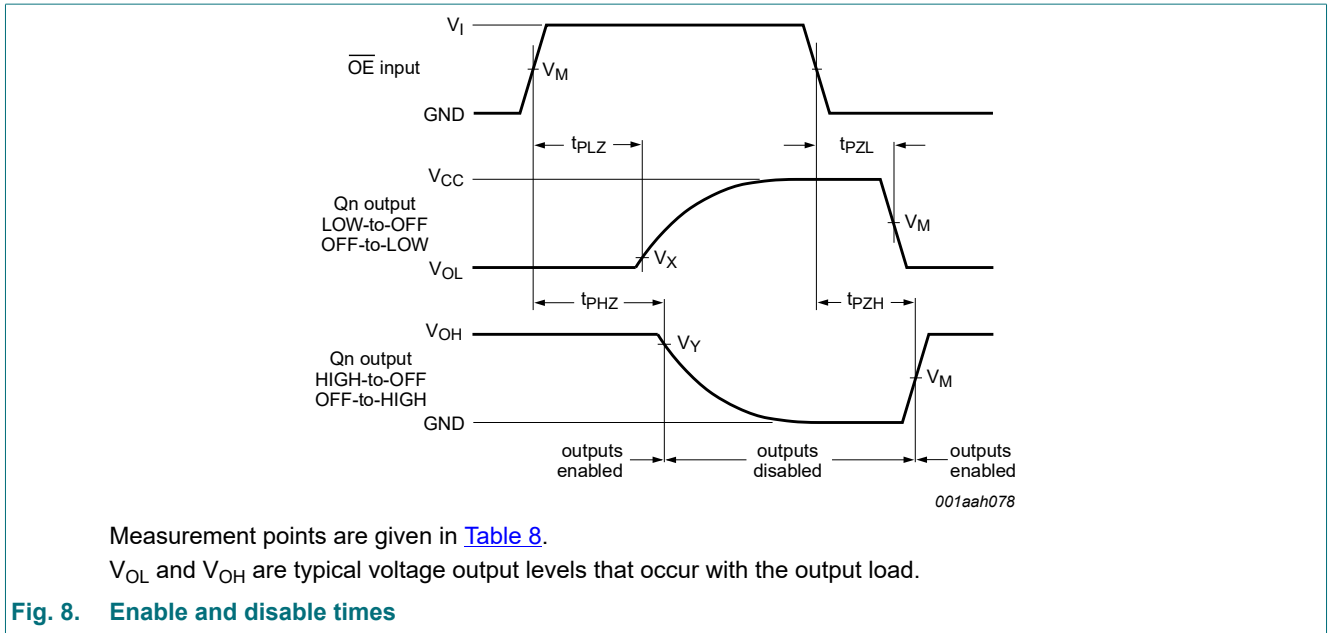


Table 8. Measurement points

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74HC574	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT574	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

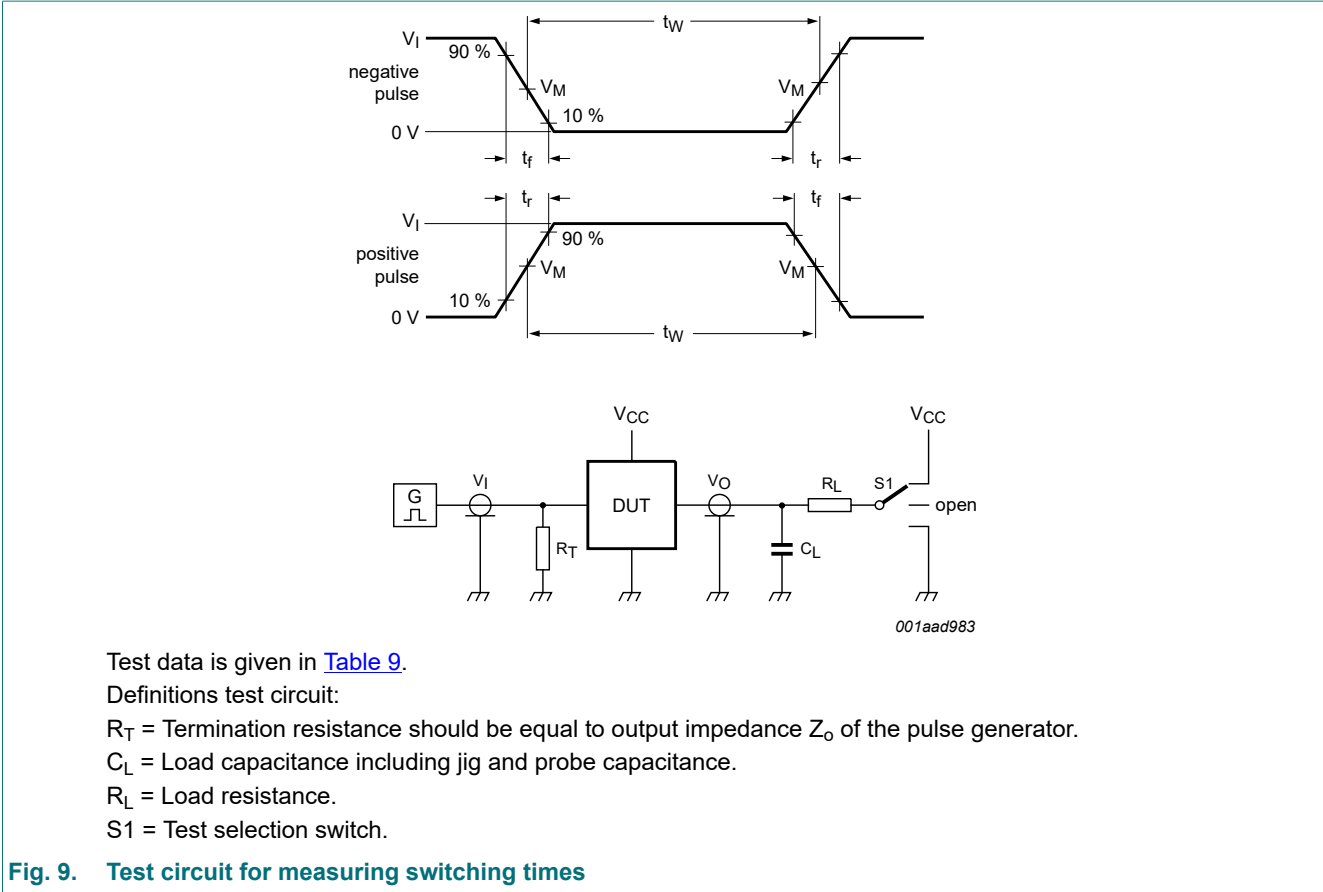


Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC574	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT574	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

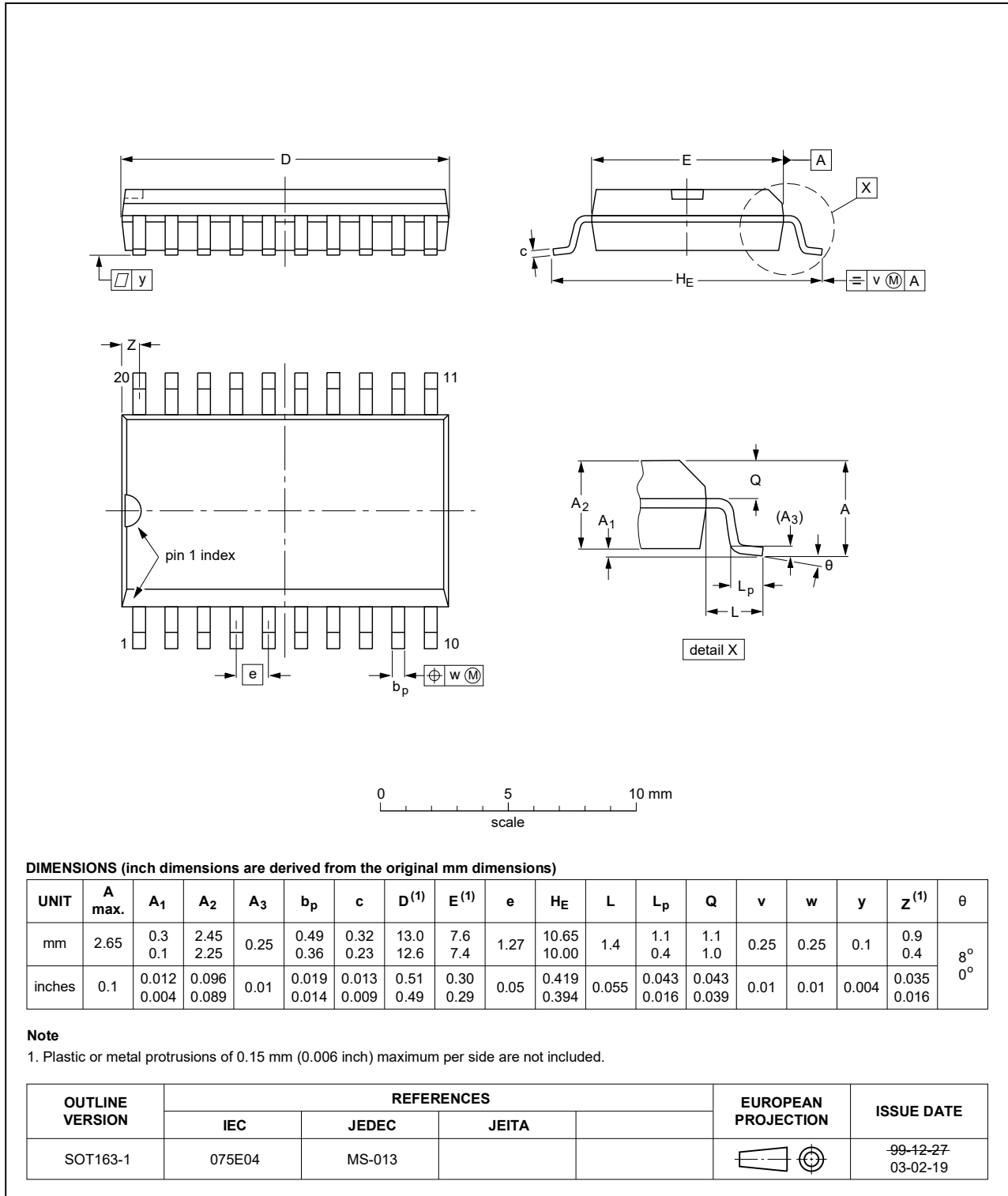


Fig. 10. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

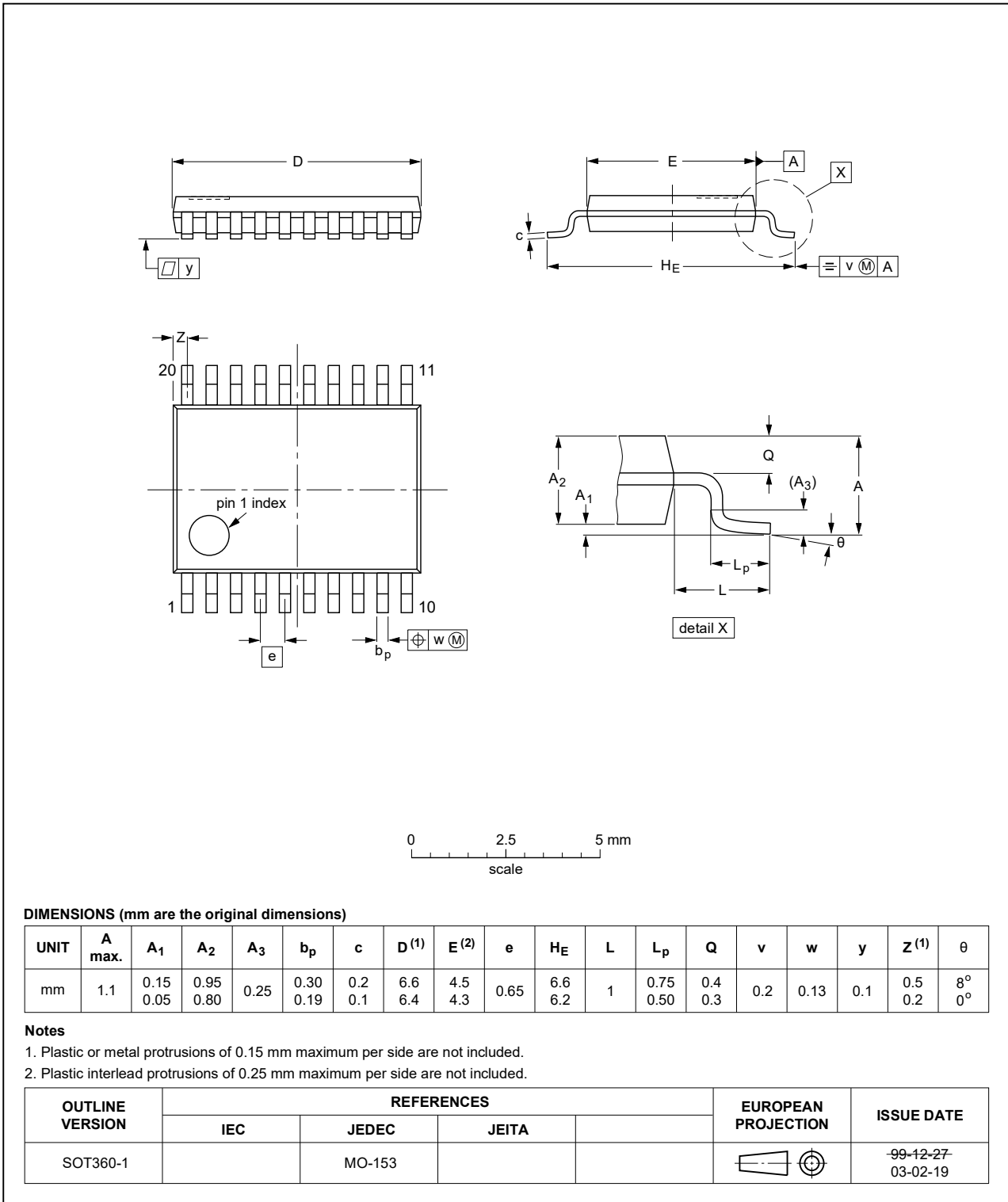


Fig. 11. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT574 v.8	20210730	Product data sheet	-	74HC_HCT574 v.7
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC574DB and 74HCT574DB (SOT339-1/SSOP20) removed.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74HC_HCT574 v.7	20160304	Product data sheet	-	74HC_HCT574 v.6
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC574N and 74HCT574N (SOT146-1) removed.</li> </ul>			
74HC_HCT574 v.6	20150126	Product data sheet	-	74HC_HCT574 v.5
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 7</a>: Power dissipation capacitance condition for 74HCT574 is corrected.</li> </ul>			
74HC_HCT574 v.5	20120425	Product data sheet	-	74HC_HCT574 v.4
Modifications:	<ul style="list-style-type: none"> <li><math>V_X</math> and <math>V_Y</math> measurement points added to <a href="#">Table 8</a>.</li> </ul>			
74HC_HCT574 v.4	20111219	Product data sheet	-	74HC_HCT574 v.3
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74HC_HCT574 v.3	20101215	Product data sheet	-	74HC_HCT574_CNV v.2
74HC_HCT574_CNV v.2	19970827	Product specification	-	-

## Octal D-type flip-flop; positive edge-trigger; 3-state

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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