

# 74LV4052-Q100

Dual 4-channel analog multiplexer/demultiplexer

Rev. 4 — 24 September 2021

Product data sheet

## 1. General description

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The 74LV4052-Q100 is a dual single-pole quad-throw analog switch suitable for use in 4:1 multiplexer/demultiplexer applications. Each switch features four independent inputs/outputs (nY0, nY1, nY2 and nY3) and a common input/output (nZ). A digital enable input (E) and two digital select inputs (S0, S1) are common to both switches. When E is HIGH, the switches are turned off. Digital inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess  $V_{CC}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.0 to 6.0 V
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Optimized for low-voltage applications: 1.0 V to 6.0 V
- Accepts TTL input levels between  $V_{CC} = 2.7\text{ V}$  and  $V_{CC} = 3.6\text{ V}$
- Low ON resistance:
  - 145  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 2.0\text{ V}$
  - 90  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 3.0\text{ V}$
  - 60  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 4.5\text{ V}$
- Logic level translation:
  - To enable 3 V logic to communicate with  $\pm 3\text{ V}$  analog signals
- Typical 'break before make' built in
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- nESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LV4052D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4052PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 4. Functional diagram

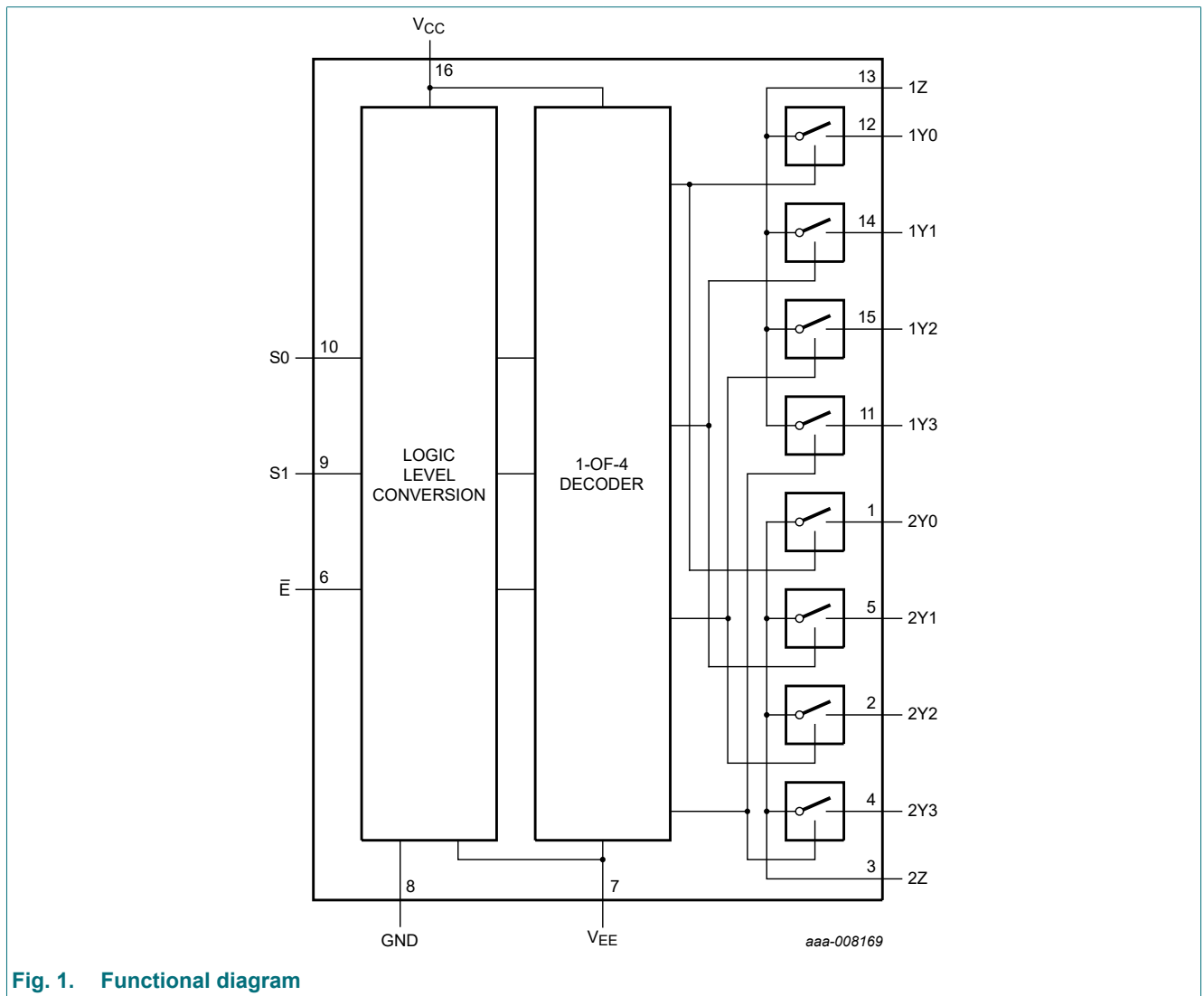


Fig. 1. Functional diagram

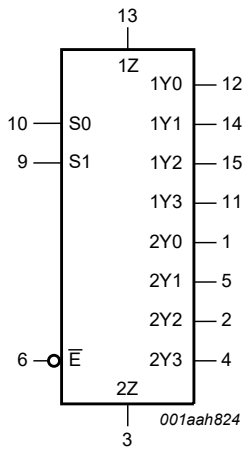


Fig. 2. Logic symbol

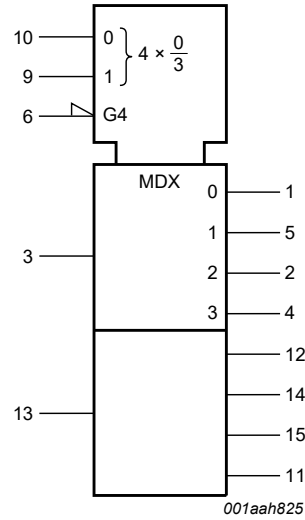


Fig. 3. IEC logic symbol

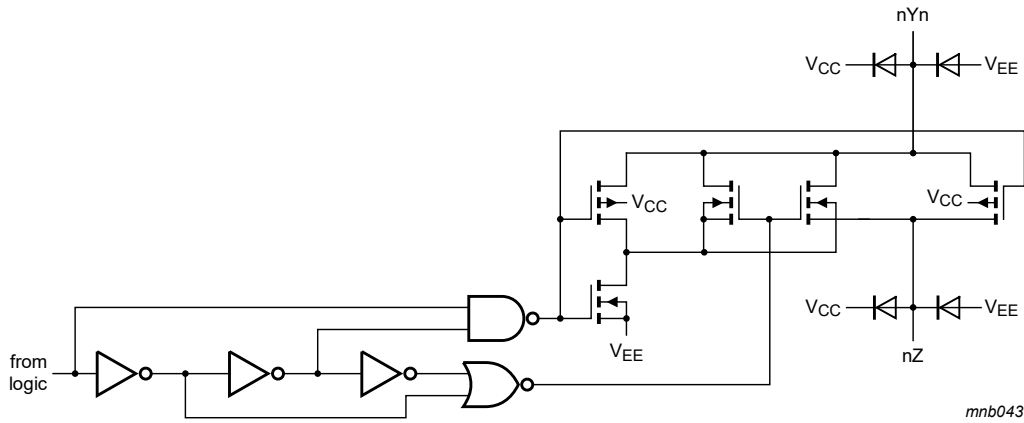


Fig. 4. Schematic diagram (one switch)

## 5. Pinning information

### 5.1. Pinning

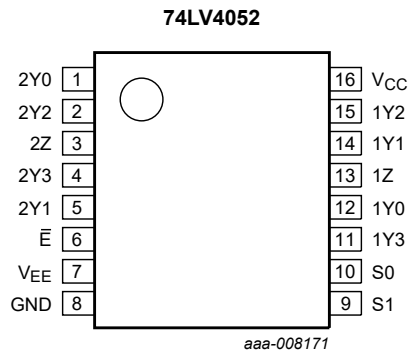


Fig. 5. Pin configuration SOT109-1 (SO16) and SOT403-1 (TSSOP16)

## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0, 2Y1, 2Y2, 2Y3	1, 5, 2, 4	independent input or output
$\bar{E}$	6	enable input (active LOW)
$V_{EE}$	7	negative supply voltage
GND	8	ground (0 V)
S0, S1	10, 9	select logic input
1Y0, 1Y1, 1Y2, 1Y3	12, 14, 15, 11	independent input or output
1Z, 2Z	13, 3	common input or output
$V_{CC}$	16	positive supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input			Channel on
$\bar{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage	[1]	-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [2]	-	$\pm 20$	mA
$I_{SK}$	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V [2]	-	$\pm 20$	mA
$I_{SW}$	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current [2]	-	$\pm 25$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [3]	-	500	mW

- [1] To avoid drawing  $V_{CC}$  current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no  $V_{CC}$  current flows out of terminals nYn. In this case, there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .
- [2] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [3] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	see Fig. 6 [1]	1	3.3	6	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{SW}$	switch voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }6.0\text{ V}$	-	-	100	ns/V

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V to }6.0\text{ V}$ . However, LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

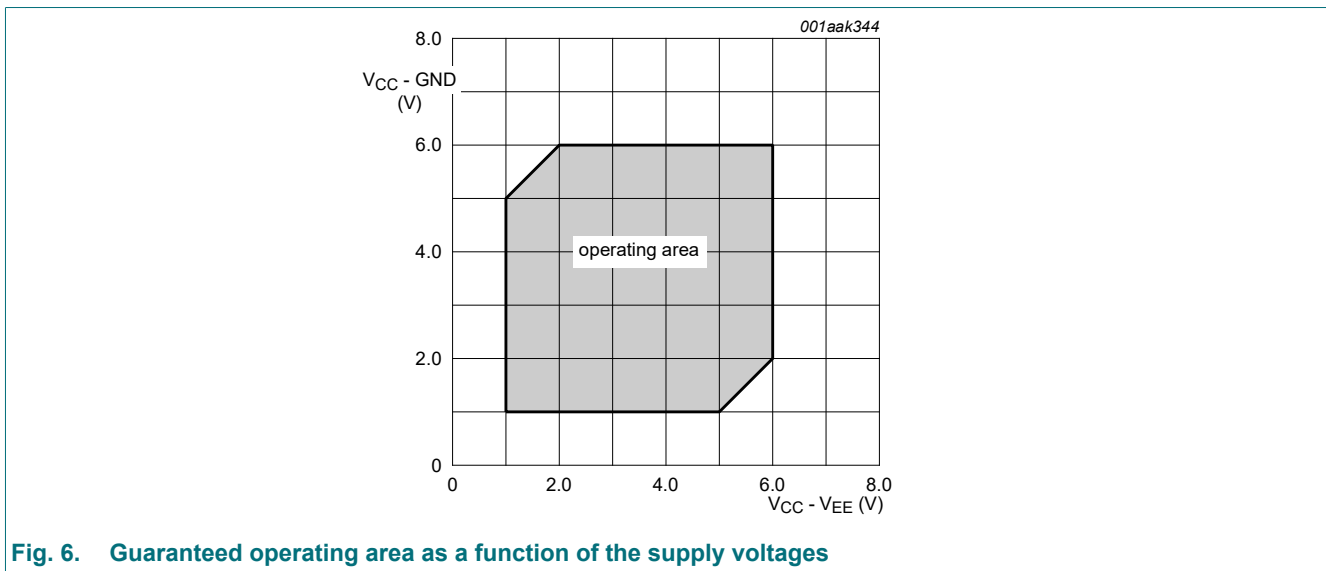


Fig. 6. Guaranteed operating area as a function of the supply voltages

## 9. Static characteristics

Table 6. Static characteristics

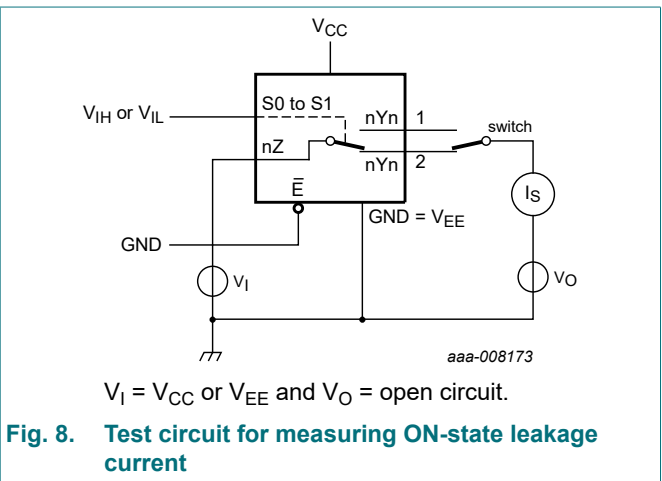
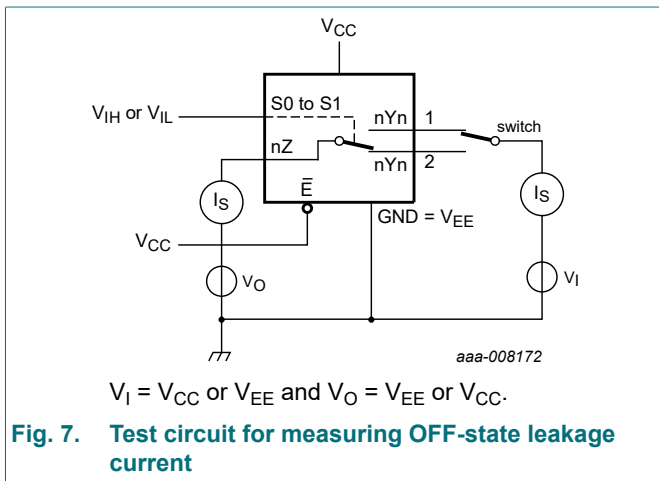
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	0.9	-	-	0.9	-	V
		$V_{CC} = 2.0\text{ V}$	1.4	-	-	1.4	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.20	-	-	4.20	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.3	-	0.3	V
		$V_{CC} = 2.0\text{ V}$	-	-	0.6	-	0.6	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.80	-	1.80	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	µA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	µA
I <sub>S(OFF)</sub>	OFF-state leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; see Fig. 7						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	µA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	µA
I <sub>S(ON)</sub>	ON-state leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; see Fig. 8						
		V <sub>CC</sub> = 3.6 V	-	-	1.0	-	1.0	µA
		V <sub>CC</sub> = 6.0 V	-	-	2.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A						
		V <sub>CC</sub> = 3.6 V	-	-	20	-	40	µA
		V <sub>CC</sub> = 6.0 V	-	-	40	-	80	µA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF
C <sub>sw</sub>	switch capacitance	independent pins nYn	-	5	-	-	-	pF
		common pins nZ	-	12	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

### 9.1. Test circuits



## 9.2. ON resistance

**Table 7. ON resistance**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit and graph see [Fig. 9](#) and [Fig. 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R <sub>ON(peak)</sub>	ON resistance (peak)	V <sub>I</sub> = 0 V to V <sub>CC</sub> - V <sub>EE</sub>						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 μA [2]	-	-	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 μA	-	145	325	-	375	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 μA	-	90	200	-	235	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 μA	-	80	180	-	210	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 μA	-	60	135	-	160	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 μA	-	55	125	-	145	Ω
ΔR <sub>ON</sub>	ON resistance mismatch between channels	V <sub>I</sub> = 0 V to V <sub>CC</sub> - V <sub>EE</sub>						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 μA [2]	-	-	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 μA	-	5	-	-	-	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 μA	-	4	-	-	-	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 μA	-	4	-	-	-	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 μA	-	3	-	-	-	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 μA	-	2	-	-	-	Ω
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = GND						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 μA [2]	-	225	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 μA	-	110	235	-	270	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 μA	-	70	145	-	165	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 μA	-	60	130	-	150	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 μA	-	45	100	-	115	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 μA	-	40	85	-	100	Ω
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = V <sub>CC</sub> - V <sub>EE</sub>						
		V <sub>CC</sub> = 1.2 V; I <sub>SW</sub> = 100 μA [2]	-	250	-	-	-	Ω
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 1000 μA	-	120	320	-	370	Ω
		V <sub>CC</sub> = 2.7 V; I <sub>SW</sub> = 1000 μA	-	75	195	-	225	Ω
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>SW</sub> = 1000 μA	-	70	175	-	205	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> = 1000 μA	-	50	130	-	150	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> = 1000 μA	-	45	120	-	135	Ω

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

[2] When supply voltages (V<sub>CC</sub> - V<sub>EE</sub>) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, only use these devices for transmitting digital signals.

9.3. On resistance test circuit and graph

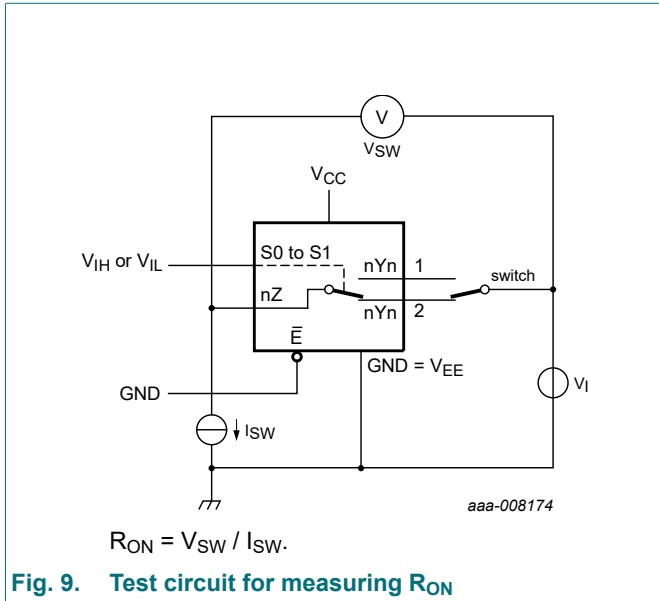


Fig. 9. Test circuit for measuring  $R_{ON}$

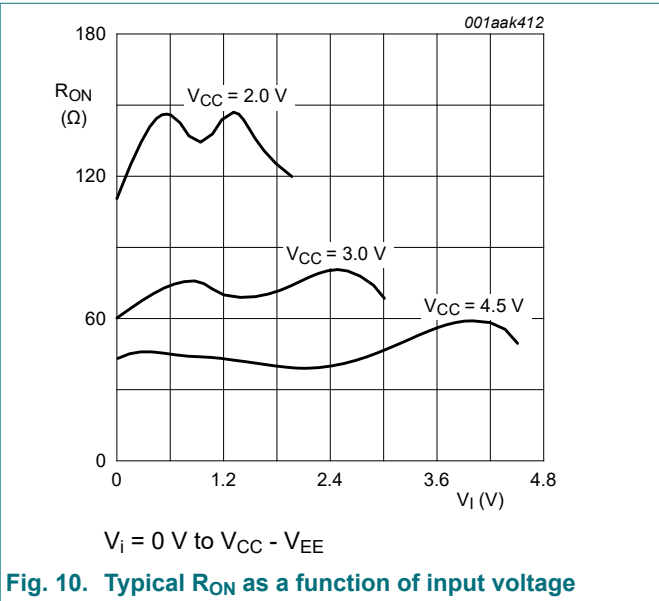


Fig. 10. Typical  $R_{ON}$  as a function of input voltage

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 13.

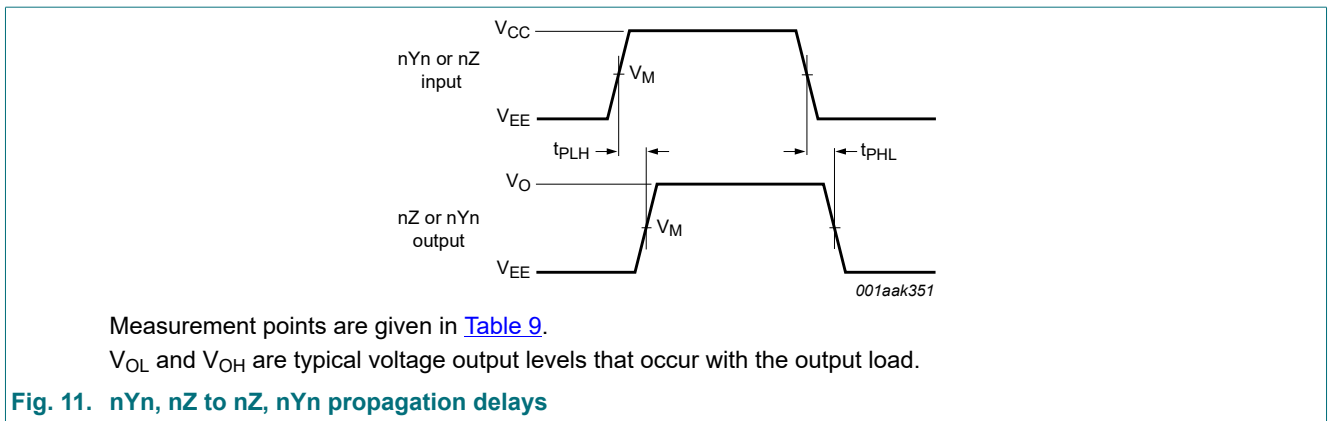
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{pd}$	propagation delay	nYn to nZ, nZ to nYn; see Fig. 11 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	25	-	-	-	ns
		$V_{CC} = 2.0 \text{ V}$	-	9	17	-	20	ns
		$V_{CC} = 2.7 \text{ V}$	-	6	13	-	15	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ [3]	-	5	10	-	12	ns
		$V_{CC} = 4.5 \text{ V}$	-	4	9	-	10	ns
		$V_{CC} = 6.0 \text{ V}$	-	3	7	-	8	ns
$t_{en}$	enable time	E, Sn to nYn, nZ; see Fig. 12 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	190	-	-	-	ns
		$V_{CC} = 2.0 \text{ V}$	-	65	121	-	146	ns
		$V_{CC} = 2.7 \text{ V}$	-	48	89	-	108	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; C_L = 15 \text{ pF}$ [3]	-	30	-	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ [3]	-	36	71	-	86	ns
		$V_{CC} = 4.5 \text{ V}$	-	32	60	-	73	ns
$V_{CC} = 6.0 \text{ V}$	-	25	46	-	56	ns		



Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>dis</sub>	disable time	$\bar{E}$ , Sn to nYn, nZ; see Fig. 12 [2]						
		V <sub>CC</sub> = 1.2 V	-	125	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	43	80	-	95	ns
		V <sub>CC</sub> = 2.7 V	-	33	59	-	71	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF [3]	-	22	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [3]	-	26	48	-	57	ns
		V <sub>CC</sub> = 4.5 V	-	23	41	-	49	ns
		V <sub>CC</sub> = 6.0 V	-	18	32	-	38	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	57	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [3] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V).
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma((C_L + C_{sw}) \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 C<sub>sw</sub> = maximum switch capacitance in pF;  
 V<sub>CC</sub> = supply voltage in Volts  
 N = number of inputs switching  
 Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

### 10.1. Waveforms and test circuit



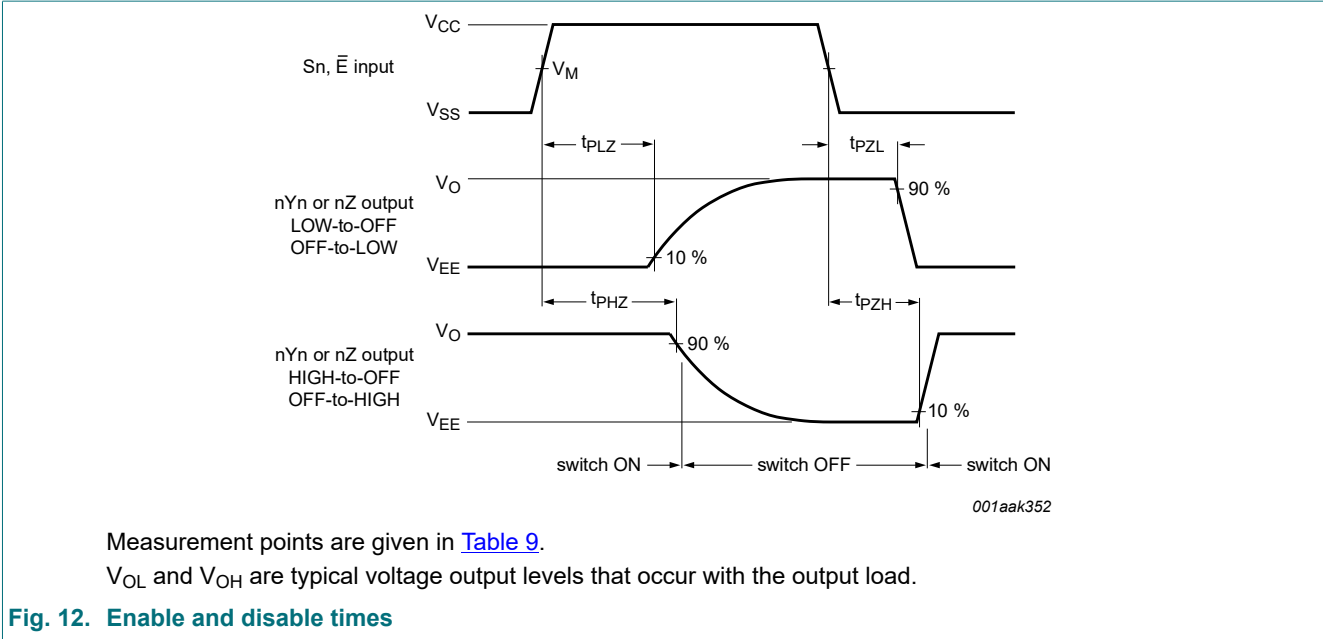
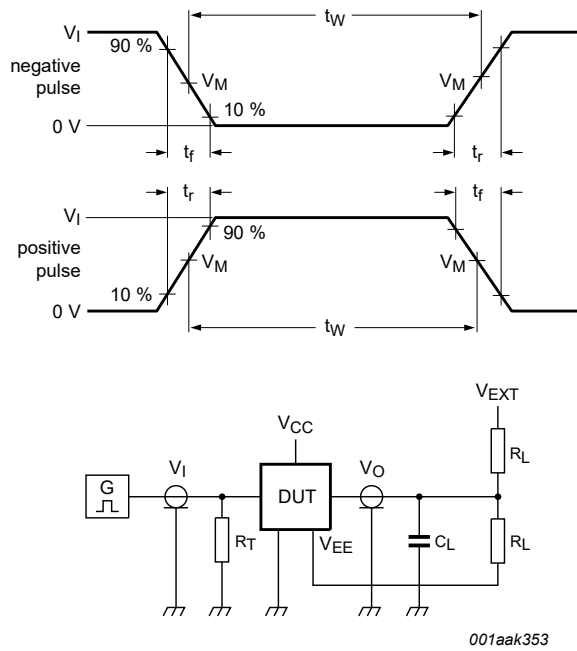


Table 9. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
> 3.6 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 13. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
< 2.7 V	$V_{CC}$	$\leq 6$ ns	50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	$\leq 6$ ns	15 pF, 50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$
> 3.6 V	$V_{CC}$	$\leq 6$ ns	50 pF	1 k $\Omega$	open	$V_{EE}$	$2V_{CC}$

## 10.2. Additional dynamic parameters

**Table 11. Additional dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $V_I = GND$  or  $V_{CC}$  (unless otherwise specified);  $t_r = t_f \leq 6.0$  ns;  $T_{amb} = 25$  °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1$ kHz; $C_L = 50$ pF; $R_L = 10$ k $\Omega$ ; see <a href="#">Fig. 14</a>				
		$V_{CC} = 3.0$ V; $V_I = 2.75$ V (p-p)	-	0.8	-	%
		$V_{CC} = 6.0$ V; $V_I = 5.5$ V (p-p)	-	0.4	-	%
		$f_i = 10$ kHz; $C_L = 50$ pF; $R_L = 10$ k $\Omega$ ; see <a href="#">Fig. 14</a>				
		$V_{CC} = 3.0$ V; $V_I = 2.75$ V (p-p)	-	2.4	-	%
		$V_{CC} = 6.0$ V; $V_I = 5.5$ V (p-p)	-	1.2	-	%
$f_{(-3dB)}$	-3 dB frequency response	$C_L = 50$ pF; $R_L = 50$ $\Omega$ ; see <a href="#">Fig. 15</a> and <a href="#">Fig. 16</a> [1]				
		$V_{CC} = 3.0$ V	-	180	-	MHz
		$V_{CC} = 6.0$ V	-	200	-	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{iso}$	isolation (OFF-state)	$f_i = 1 \text{ MHz}$ ; $C_L = 50 \text{ pF}$ ; $R_L = 600 \text{ }\Omega$ ; see Fig. 17 and Fig. 18				
		$V_{CC} = 3.0 \text{ V}$	-	-50	-	dB
		$V_{CC} = 6.0 \text{ V}$	-	-50	-	dB
$V_{ct}$	crosstalk voltage	between digital inputs and switch; $f_i = 1 \text{ MHz}$ ; $C_L = 50 \text{ pF}$ ; $R_L = 600 \text{ }\Omega$ ; see Fig. 19				
		$V_{CC} = 3.0 \text{ V}$	-	0.11	-	V
		$V_{CC} = 6.0 \text{ V}$	-	0.12	-	V
Xtalk	crosstalk	between switches; $f_i = 1 \text{ MHz}$ ; $C_L = 50 \text{ pF}$ ; $R_L = 600 \text{ }\Omega$ ; [2] see Fig. 20				
		$V_{CC} = 3.0 \text{ V}$	-	-60	-	dB
		$V_{CC} = 6.0 \text{ V}$	-	-60	-	dB

- [1] To obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50  $\Omega$ ), adjust  $f_i$  voltage.
- [2] To obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600  $\Omega$ ), adjust  $f_i$  voltage.

10.2.1. Test circuits

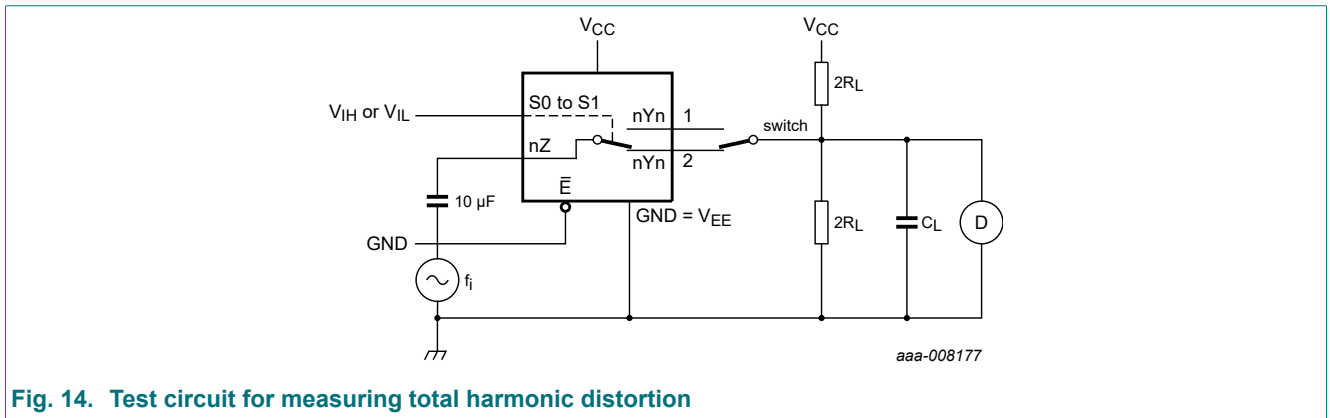


Fig. 14. Test circuit for measuring total harmonic distortion

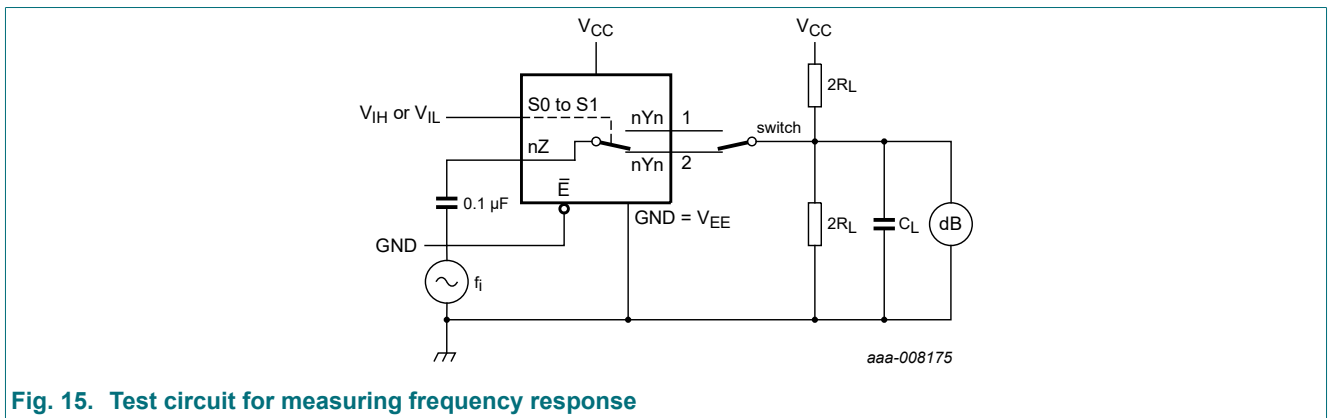
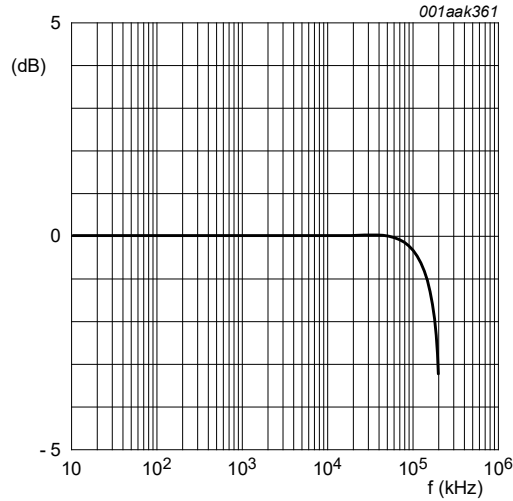


Fig. 15. Test circuit for measuring frequency response



$V_{CC} = 3.0\text{ V}$ ;  $GND = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$ ;  $R_L = 50\ \Omega$ ;  $R_{SOURCE} = 1\text{ k}\Omega$ .

Fig. 16. Typical frequency response

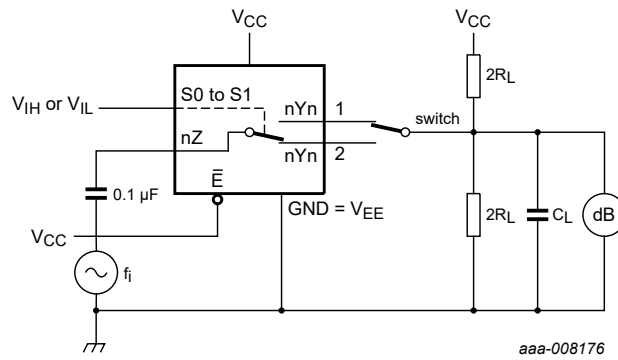
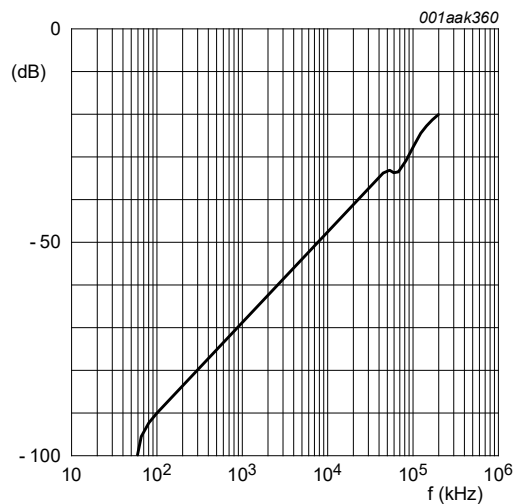
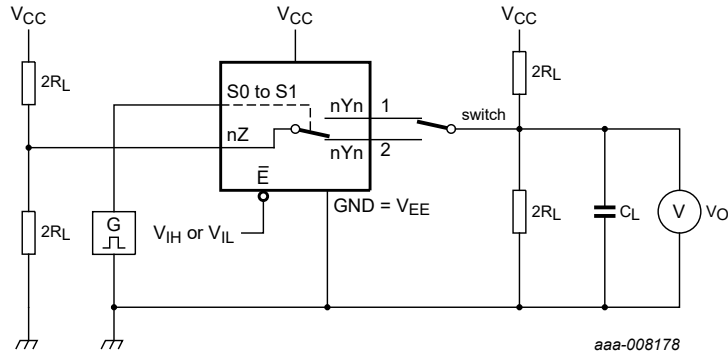


Fig. 17. Test circuit for measuring isolation (OFF-state)

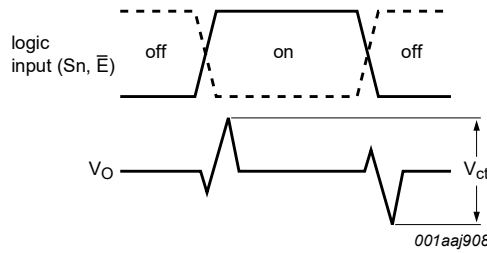


$V_{CC} = 3.0\text{ V}$ ;  $GND = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$ ;  $R_L = 50\ \Omega$ ;  $R_{SOURCE} = 1\text{ k}\Omega$ .

Fig. 18. Typical isolation (OFF-state) as function of frequency

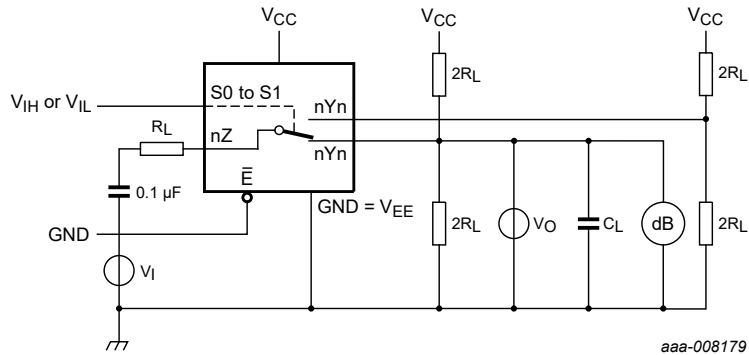


a. Test circuit

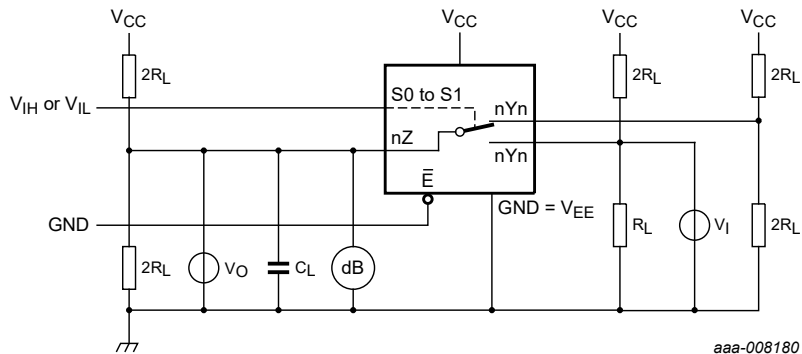


b. Input and output pulse definitions  
 $V_I$  may be connected to  $S_n$  or  $\bar{E}$ .

**Fig. 19. Test circuit for measuring crosstalk voltage between digital inputs and switch**



a. Switch on channel.



b. Switch off channel.

**Fig. 20. Test circuit for measuring crosstalk between switches**

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

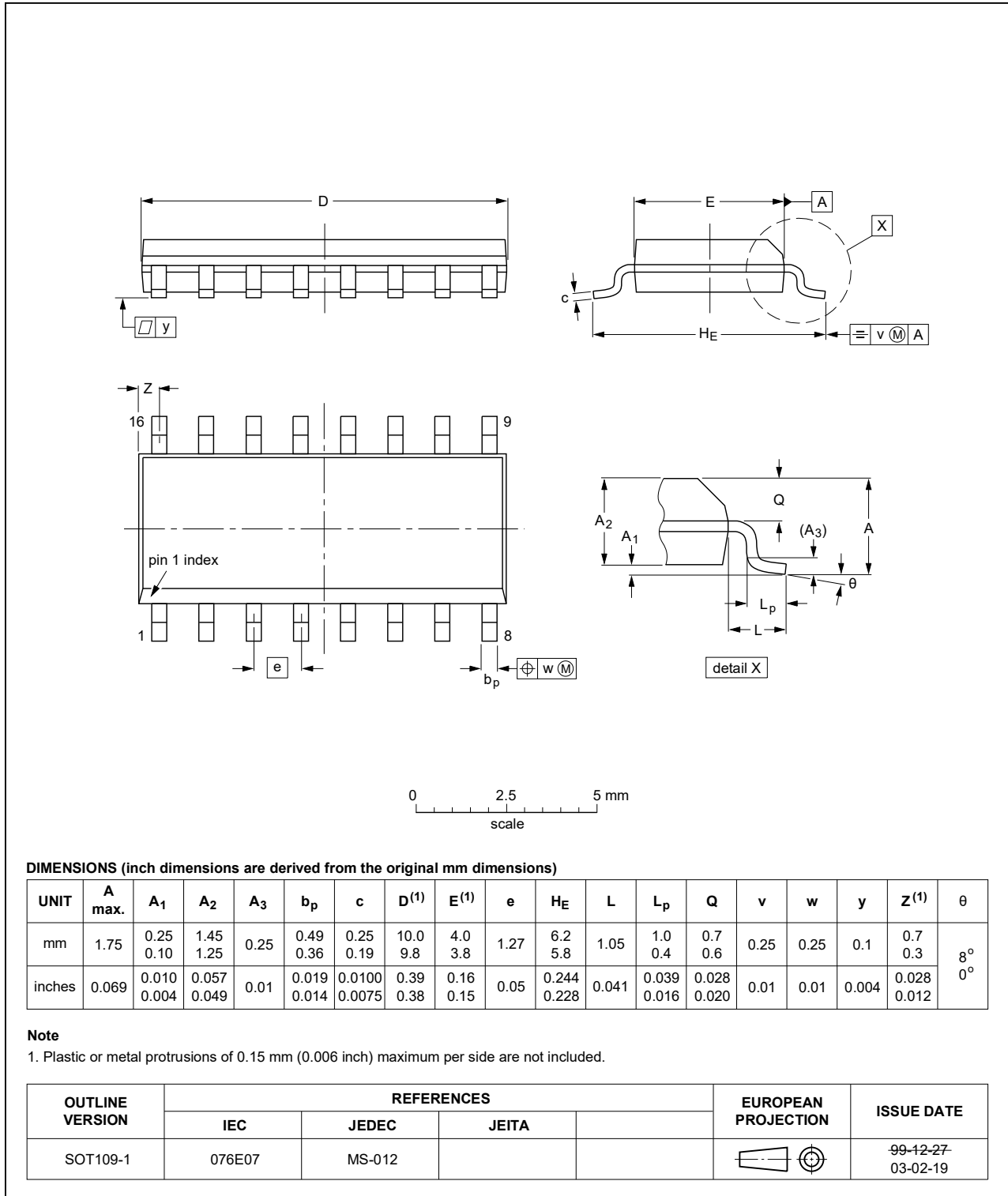


Fig. 21. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

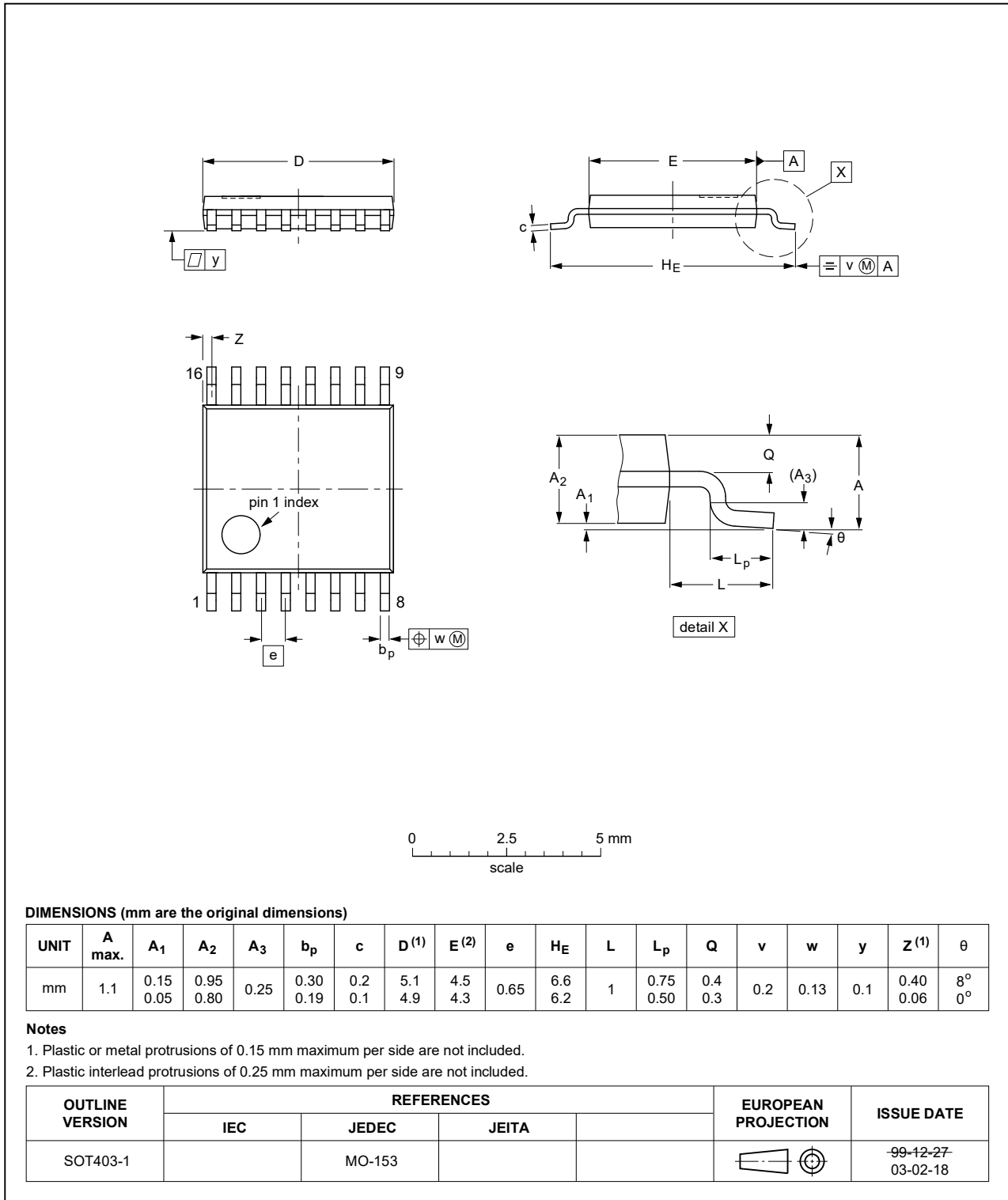


Fig. 22. Package outline SOT403-1 (TSSOP16)



## 12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4052_Q100 v.4	20210924	Product data sheet	-	74LV4052_Q100 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74LV4052_Q100 v.3	20151022	Product data sheet	-	74LV4052_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>Descriptive title corrected (errata)</li> </ul>			
74LV4052_Q100 v.2	20140915	Product data sheet	-	74LV4052_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD protection: MIL-STD-833 changed to MIL-STD883</li> <li><a href="#">Table 1</a>: Typo in type number corrected.</li> </ul>			
74LV4052_Q100 v.1	20130722	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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