74LV74-Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 2 — 24 March 2021 Product data sheet

1. General description

The 74LV74-Q100 is a dual positive edge triggered D-type flip-flop with individual data (nD), clock (nCP), set (n \overline{SD}) and reset (n \overline{RD}) inputs, and complementary nQ and n \overline{Q} outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the nQ output. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications from 1.0 V to 3.6 V
- · CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Direct interface with TTL levels (2.7 V to 3.6 V)
- ESD protection:
 - MIL-STD-833, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

3. Ordering information

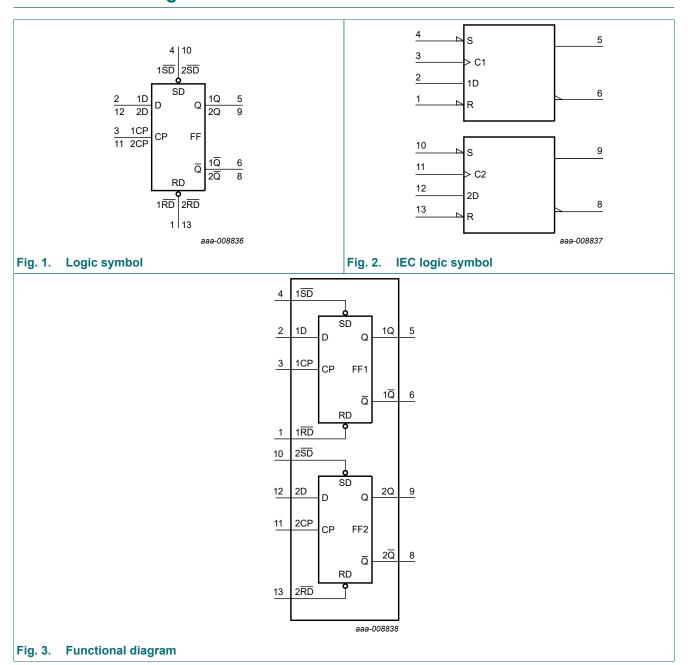
Table 1. Ordering information

Type number	Package									
	Temperature range	Name	Description	Version						
74LV74D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1						
74LV74PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1						

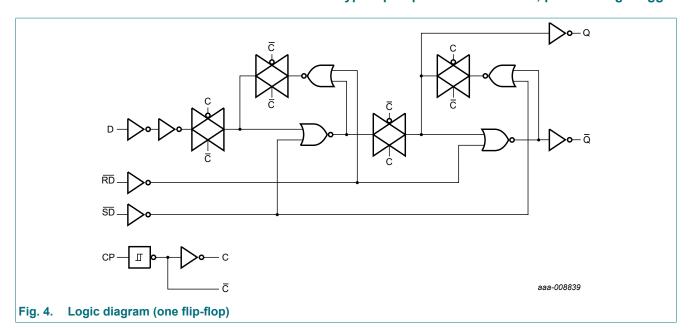


Dual D-type flip-flop with set and reset; positive-edge trigger

4. Functional diagram

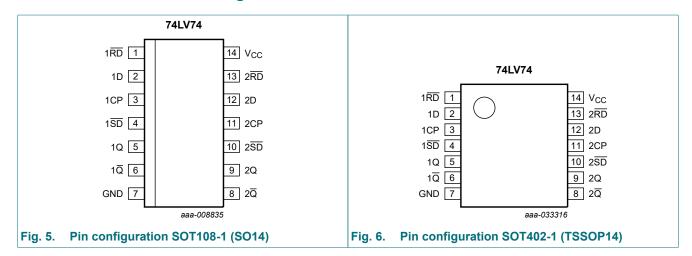


Dual D-type flip-flop with set and reset; positive-edge trigger



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD, 2RD	1, 13	asynchronous reset-direct input (active-LOW)
1D, 2D	2, 12	data inputs
1CP, 2CP	3, 11	clock input (LOW-to-HIGH), edge-triggered)
1 <u>SD</u> , 2 <u>SD</u>	4, 10	asynchronous set-direct input (active-LOW)
1Q, 2Q	5, 9	true flip-flop outputs
1Q, 2Q	6, 8	complement flip-flop outputs
GND	7	ground (0 V)
V _{CC}	14	supply voltage

Dual D-type flip-flop with set and reset; positive-edge trigger

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care;$

 \uparrow = LOW-to-HIGH clock transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition

Input				Output				
nSD	nRD	nCP	nD	nQ	nQ	Q _{n+1}	nQ _{n+1}	
L	Н	Х	Х	Н	L	-	-	
Н	L	Х	Х	L	Н	-	-	
L	L	Х	Х	Н	Н	-	-	
Н	Н	↑	L	-	-	L	Н	
Н	Н	↑	Н	-	-	Н	L	

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage	[1]	-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	-	20	mA
VI	input voltage	[1]	-0.5	+7	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
Io	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	±50	mA
I _{GND}	ground current		-	±50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$ [2]	-	500	

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

Dual D-type flip-flop with set and reset; positive-edge trigger

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage [1]		1.0	3.3	5.5	V
VI	input voltage		0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.0 V to 2.0 V	0	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	0	-	200	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	100	ns/V
		V _{CC} = 3.6 V to 5.5 V	0	-	50	ns/V

^{[1] 74}LV74 is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V.

Dual D-type flip-flop with set and reset; positive-edge trigger

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 1.2 V	0.9	-	-	0.9	-	٧
	input voltage	V _{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	٧
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	٧
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	٧
V _{IL}	LOW-level	V _{CC} = 1.2 V	-	-	0.3	-	0.3	٧
	input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.6	٧
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	٧
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $I_O = -100 \mu A$						
	output voltage	V _{CC} = 1.2 V	-	1.2		-		
		V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	٧
		V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	٧
		V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	٧
		V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	٧
		standard outputs: V _I = V _{IH} or V _{IL}						
		V _{CC} = 3.0 V; I _O = -6 mA	2.40	2.82	-	2.20	-	٧
		V _{CC} = 4.5 V; I _O = -12 mA	3.60	4.20	-	3.50	-	٧
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $I_O = 100 \mu A$						
	output voltage	V _{CC} = 1.2 V	-	0	-	-	-	
		V _{CC} = 2.0 V	-	0	0.2		0.2	V
		V _{CC} = 2.7 V	-	0	0.2		0.2	٧
		V _{CC} = 3.0 V	-	0	0.2		0.2	٧
		V _{CC} = 4.5 V	-	0	0.2		0.2	٧
		standard outputs: V _I = V _{IH} or V _{IL}						
		V _{CC} = 3.0 V; I _O = 6 mA	-	0.25	0.40	-	0.50	V
		V _{CC} = 4.5 V; I _O = 12 mA	-	0.35	0.55	-	0.65	٧
lı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1	-	±1	μA
lcc	supply current	$V_{I} = V_{CC}$ or GND; $I_{O} = 0$ A; $V_{CC} = 5.5$ V	-	-	20	-	80	μΑ
ΔI _{CC}	additional supply current	$V_1 = V_{CC} - 0.6 \text{ V}; V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	500	-	850	μA
Cı	input capacitance		-	3.5	-			pF

^[1] Typical values are measured at T_{amb} = 25 °C.

Dual D-type flip-flop with set and reset; positive-edge trigger

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see Fig. 9

Symbol	Parameter	Conditions		-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation	nCP to nQ, nQ; see Fig. 7	[2]						
	delay	V _{CC} = 1.2 V		-	70	-	-	-	ns
		V _{CC} = 2.0 V		-	24	44	-	56	ns
		V _{CC} = 2.7 V		-	18	28	-	41	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	13	26	-	33	ns
		V _{CC} = 3.3 V; C _L = 15 pF		-	11	-	-	-	ns
		V _{CC} = 4.5 V to 5.5 V	[4]	-	9.5	17	-	23	ns
		nSD to nQ, nQ; see Fig. 8							
		V _{CC} = 1.2 V		-	90	-	-	-	ns
		V _{CC} = 2.0 V		-	31	46	-	58	ns
		V _{CC} = 2.7 V		-	23	34	-	43	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	17	27	-	34	ns
		V _{CC} = 3.3 V; C _L = 15 pF		-	14	-	-	-	ns
		V _{CC} = 4.5 V to 5.5 V	[4]	-	12	19	-	24	ns
		nRD to nQ, nQ; see Fig. 8							
		V _{CC} = 1.2 V		-	90	-	-	-	ns
		V _{CC} = 2.0 V		-	31	46	-	58	ns
		V _{CC} = 2.7 V		-	23	34	-	43	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	17	27	-	34	ns
		V _{CC} = 3.3 V; C _L = 15 pF		-	14	-	-	-	ns
		V _{CC} = 4.5 V to 5.5 V	[4]	-	12	19	-	24	ns
t _W	pulse width	nCP input HIGH to LOW; see Fig. 7							
		V _{CC} = 2.0 V		34	10	-	41	-	ns
		V _{CC} = 2.7 V		25	8	-	30	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	20	7	-	24	-	ns
		V _{CC} = 4.5 V to 5.5 V	[4]	15	6	-	18	-	ns
		nSD or nRD pulse width LOW; see Fig. 8							
		V _{CC} = 2.0 V		34	10	-	41	-	ns
		V _{CC} = 2.7 V		25	8	-	30	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	20	7	-	24	-	ns
		V _{CC} = 4.5 V to 5.5 V	[4]	15	6	-	18	-	ns
t _{rec}	recovery time	nRD; see Fig. 8							
		V _{CC} = 1.2 V		-	5	-	-	-	ns
		V _{CC} = 2.0 V		14	2	-	15	-	ns
		V _{CC} = 2.7 V		10	1	-	11	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	8	1	-	9	-	ns
		V _{CC} = 4.5 V to 5.5 V	[4]	6	1	-	7	_	ns

7 / 15

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions		-40	°C to +8	5°C	-40 °C to	+125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t _{su}	set-up time	nD to nCP; see Fig. 7							
		V _{CC} = 1.2 V		-	10	-	-	-	ns
		V _{CC} = 2.0 V		22	4	-	26	-	ns
		V _{CC} = 2.7 V		12	3	-	15	-	ns
		V _{CC} = 3.0 V to 3.6 V	3]	8	2	-	10	-	ns
		V _{CC} = 4.5 V to 5.5 V	ij	6	1	-	8	-	ns
t _h	hold time	nD to nCP; see Fig. 7							
		V _{CC} = 1.2 V		-	-10	-	-	-	ns
		V _{CC} = 2.0 V		3	-2	-	3	-	ns
		V _{CC} = 2.7 V		3	-2	-	3	-	ns
		V _{CC} = 3.0 V to 3.6 V	3]	3	-2	-	3	-	ns
		V _{CC} = 4.5 V to 5.5 V	ij	3	-2	-	3	-	ns
f _{max}	maximum	nCP; see Fig. 7							
	frequency	V _{CC} = 2.0 V		14	40	-	12	-	MHz
		V _{CC} = 2.7 V		50	90	-	40	-	MHz
		V _{CC} = 3.0 V to 3.6 V	3]	60	100	-	48	-	MHz
		V _{CC} = 4.5 V to 5.5 V	ij	70	110	-	56	-	MHz
C _{PD}	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}$ [5	5]	-	24	-	-	-	pF

- Typical values are measured at T_{amb} = 25 °C. [1]
- t_{pd} is the same as t_{PHL} and t_{PLH} . Typical value measured at V_{CC} = 3.3 V. [2] [3]
- Typical values are measured at $V_{CC} = 5.0 \text{ V}$.
- C_{PD} is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ ($P_D = P_D \times V_{CC}^2 \times f_o = 0$), where: f_i = input frequency in MHz;

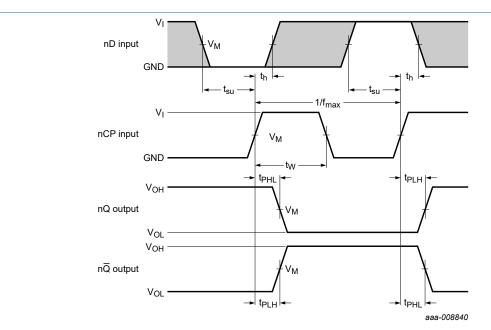
f_o = output frequency in MHz;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs; C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

Dual D-type flip-flop with set and reset; positive-edge trigger

10.1. Waveforms and test circuit

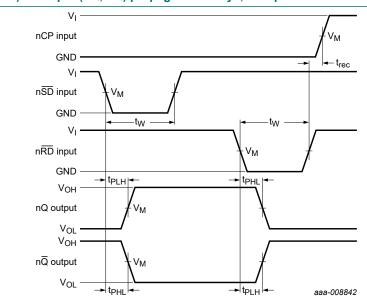


Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 7. Clock pulse (nCP) to output (nQ, $n\overline{Q}$) propagation delays, nCP pulse width and maximum frequency



Measurement points are given in Table 8.

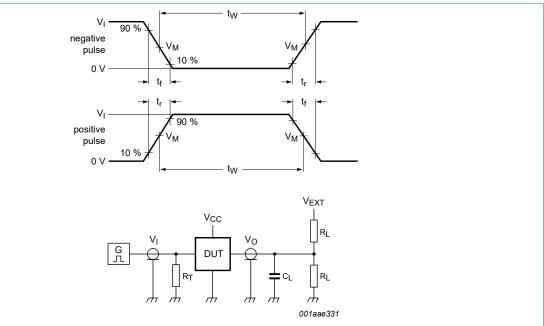
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. The set (nSD) and reset (nRD) input to output (nQ, nQ) propagation delays, the set and reset pulse widths and the nRD to nCP recovery time

Dual D-type flip-flop with set and reset; positive-edge trigger

Table 8. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
< 2.7 V	0.5V _{CC}	0.5V _{CC}
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	0.5V _{CC}	0.5V _{CC}



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_{T} = Termination resistance should be equal to output impedance Z_{o} of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

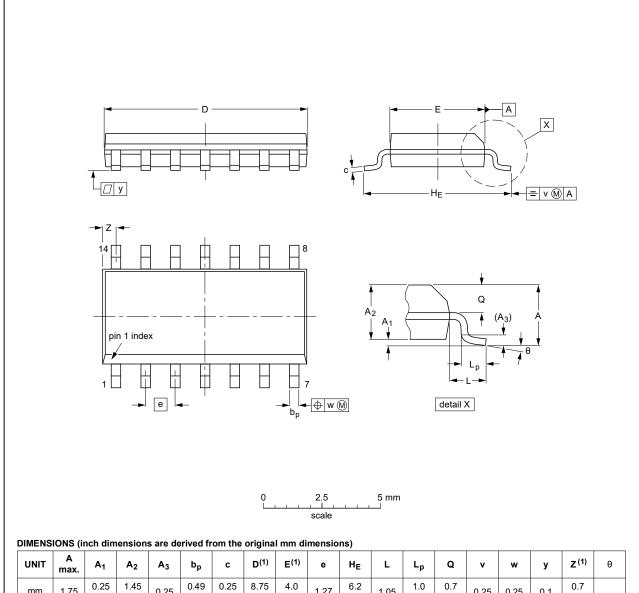
Supply voltage	Input		Load	Load			
	V _I	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}		
< 2.7 V	V _{CC}	2.5 ns	50 pF	1 kΩ	open		
2.7 V to 3.6 V	2.7 V	2.5 ns	50 pF, 15 pF	1 kΩ	open		
≥ 4.5 V	V _{CC}	2.5 ns	50 pF	1 kΩ	open		

Dual D-type flip-flop with set and reset; positive-edge trigger

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

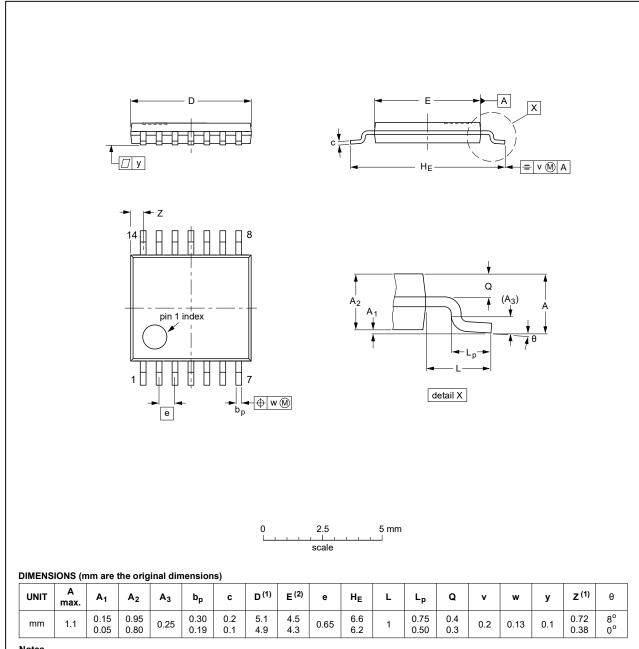
OUTLINE	OUTLINE REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig. 10. Package outline SOT108-1 (SO14)

Dual D-type flip-flop with set and reset; positive-edge trigger

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				99-12-27 03-02-18

Fig. 11. Package outline SOT402-1 (TSSOP14)

Dual D-type flip-flop with set and reset; positive-edge trigger

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
	rtorougo unto	Data on our clarac	Gridingo nodioo	•	
74LV74_Q100 v.2	20210324	Product data sheet	-	74LV74_Q100 v.1	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Section 7: Derating values for Ptot total power dissipation updated. 				
74LV74_Q100 v.1	20130923	Product data sheet	-	-	

Dual D-type flip-flop with set and reset; positive-edge trigger

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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74LV74_Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	3
5.1. Pinning	3
5.2. Pin description	3
6. Functional description	4
7. Limiting values	4
8. Recommended operating conditions	5
9. Static characteristics	е
10. Dynamic characteristics	7
10.1. Waveforms and test circuit	9
11. Package outline	1 1
12. Abbreviations	13
13. Revision history	13
14. Legal information	14

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