

# 74LVC157A

## Quad 2-input multiplexer

Rev. 10 — 20 September 2021

Product data sheet

## 1. General description

The 74LVC157A is a quad 2-input multiplexer. The device features select (S) and enable  $\bar{E}$  inputs. A HIGH on S selects data source 1, a LOW data source 0. A HIGH on  $\bar{E}$  forces all the outputs (1Y to 4Y) LOW. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

## 2. Features and benefits

- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC157AD	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC157APW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC157ABQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 4. Functional diagram

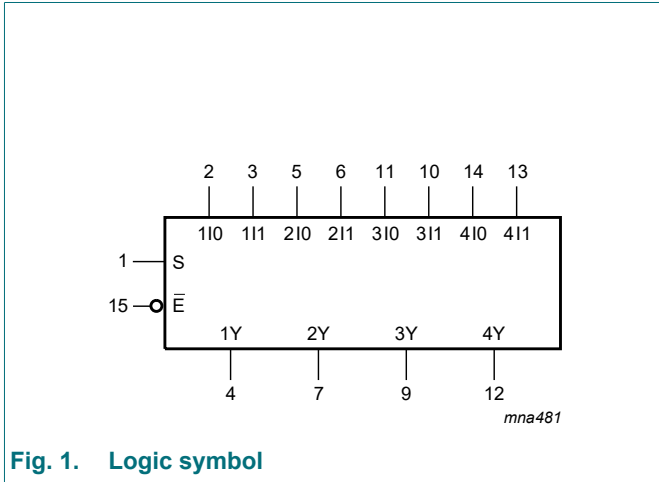


Fig. 1. Logic symbol

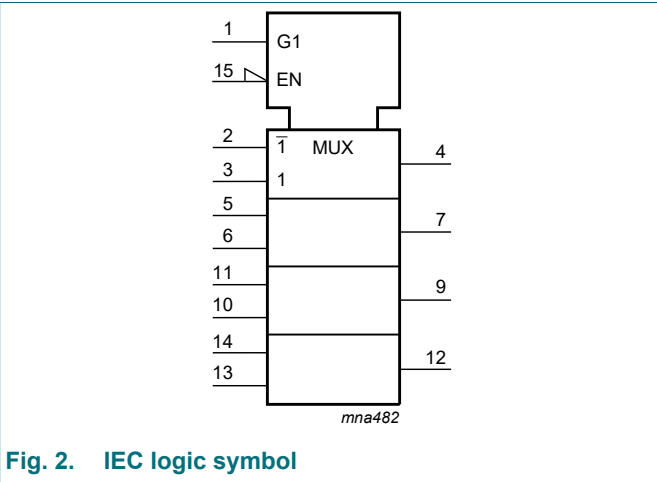


Fig. 2. IEC logic symbol

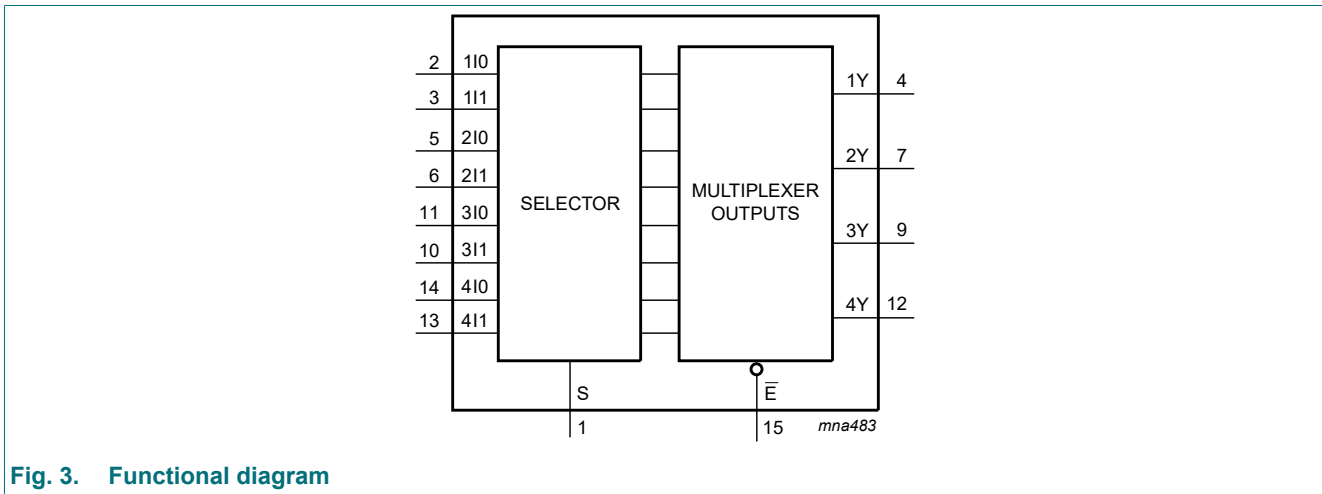


Fig. 3. Functional diagram

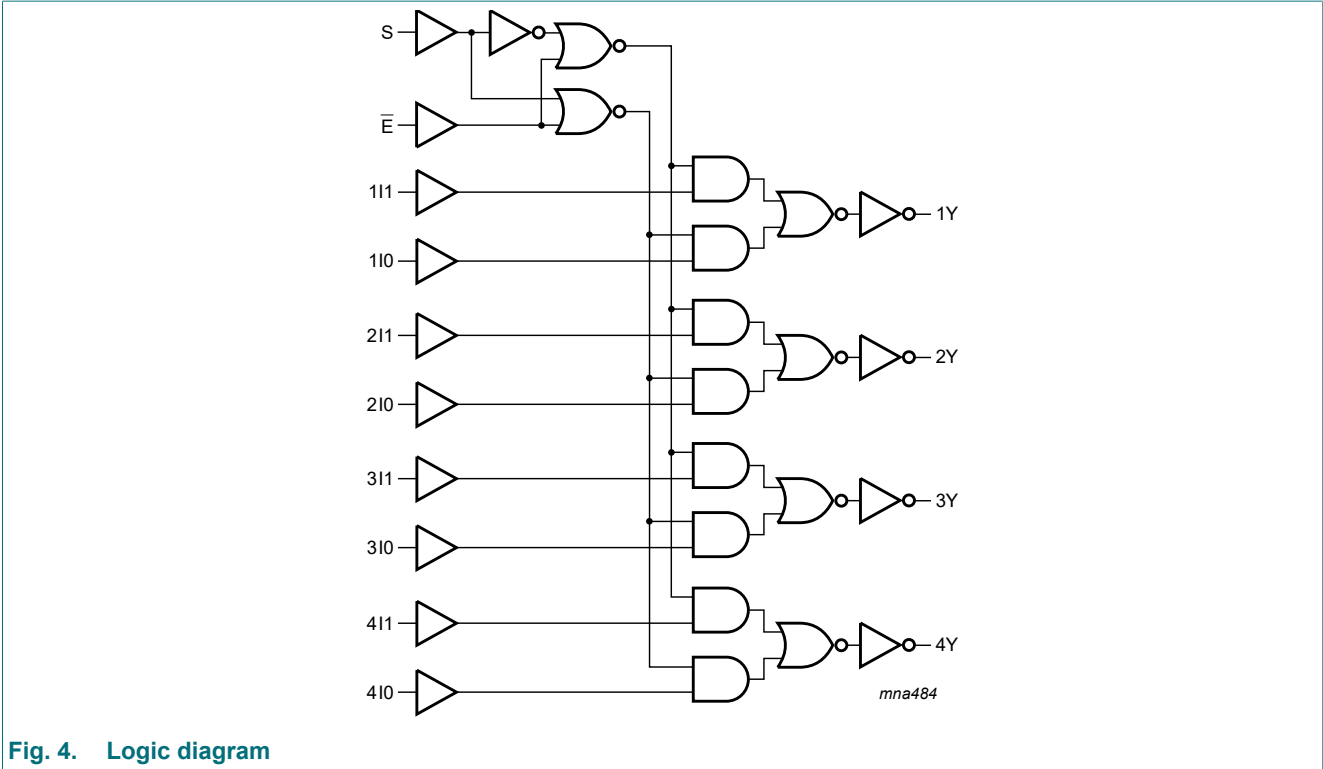


Fig. 4. Logic diagram

## 5. Pinning information

### 5.1. Pinning

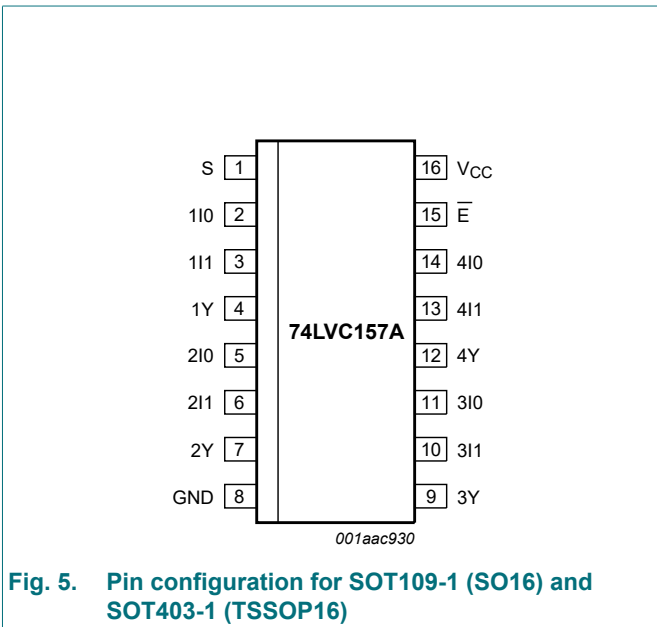


Fig. 5. Pin configuration for SOT109-1 (SO16) and SOT403-1 (TSSOP16)

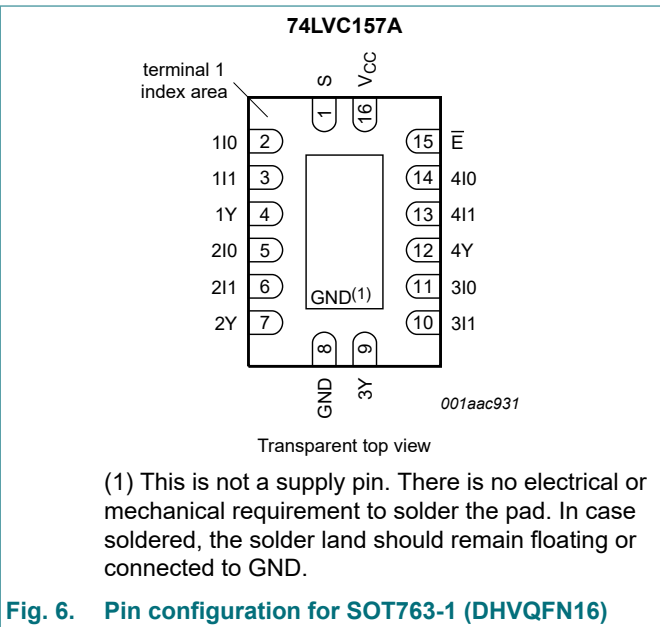


Fig. 6. Pin configuration for SOT763-1 (DHVQFN16)

## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0	2	data input from source 0
1I1	3	data input from source 1
1Y	4	multiplexer output
2I0	5	data input from source 0
2I1	6	data input from source 1
2Y	7	multiplexer output
GND	8	ground (0 V)
3Y	9	multiplexer output
3I1	10	data input from source 1
3I0	11	data input from source 0
4Y	12	multiplexer output
4I1	13	data input from source 1
4I0	14	data input from source 0
$\bar{E}$	15	enable input (active LOW)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input				Output
$\bar{E}$	S	nI0	nI1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	$\pm 50$	mA
$V_O$	output voltage	[2]	-0.5	$V_{CC} + 0.5$	V
$I_O$	output current	$V_O = 0\text{ V to }V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$ [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 x V <sub>CC</sub>	-	-	0.65 x V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 x V <sub>CC</sub>	-	0.35 x V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nI0, nI1 to nY; see Fig. 7 [2]						
		V <sub>CC</sub> = 1.2 V	-	16	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	4.8	10.2	1.0	11.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	2.8	5.8	1.5	6.7	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.9	5.9	1.0	7.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	5.2	1.0	6.5	ns
		$\bar{E}$ to nY; see Fig. 8 [2]						
		V <sub>CC</sub> = 1.2 V	-	17	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.5	4.8	12.8	0.5	14.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	2.8	7.2	1.5	8.3	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.9	7.8	1.0	10.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.6	6.5	1.0	8.5	ns
		S to nY; see Fig. 7 [2]						
		V <sub>CC</sub> = 1.2 V	-	16	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	5.1	12.4	1.0	14.3	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	3.0	7.0	1.5	8.1	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.1	7.3	1.0	9.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.7	6.3	1.0	8.0	ns
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V [3]	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub> [4]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	9.4	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	12.8	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	15.9	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

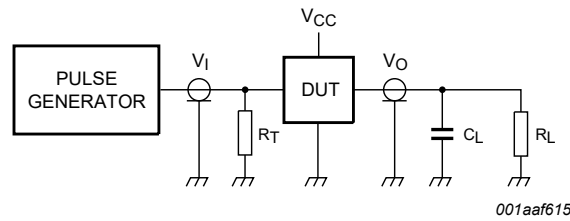
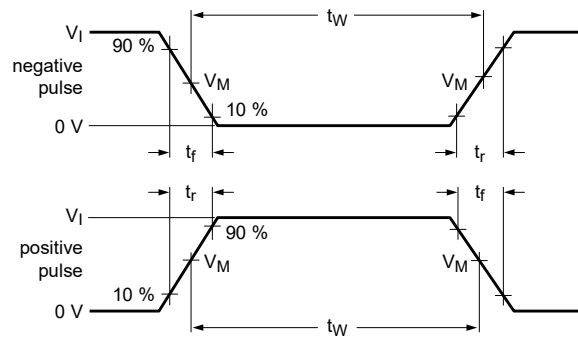
V<sub>CC</sub> = supply voltage in V

N = number of inputs switching

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs







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Test data is given in [Table 8](#). Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

**Fig. 9. Test circuit for measuring switching times**

**Table 8. Test data**

Supply voltage	Input		Load	
	$V_I$	$t_r, t_f$	$C_L$	$R_L$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$

### 11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

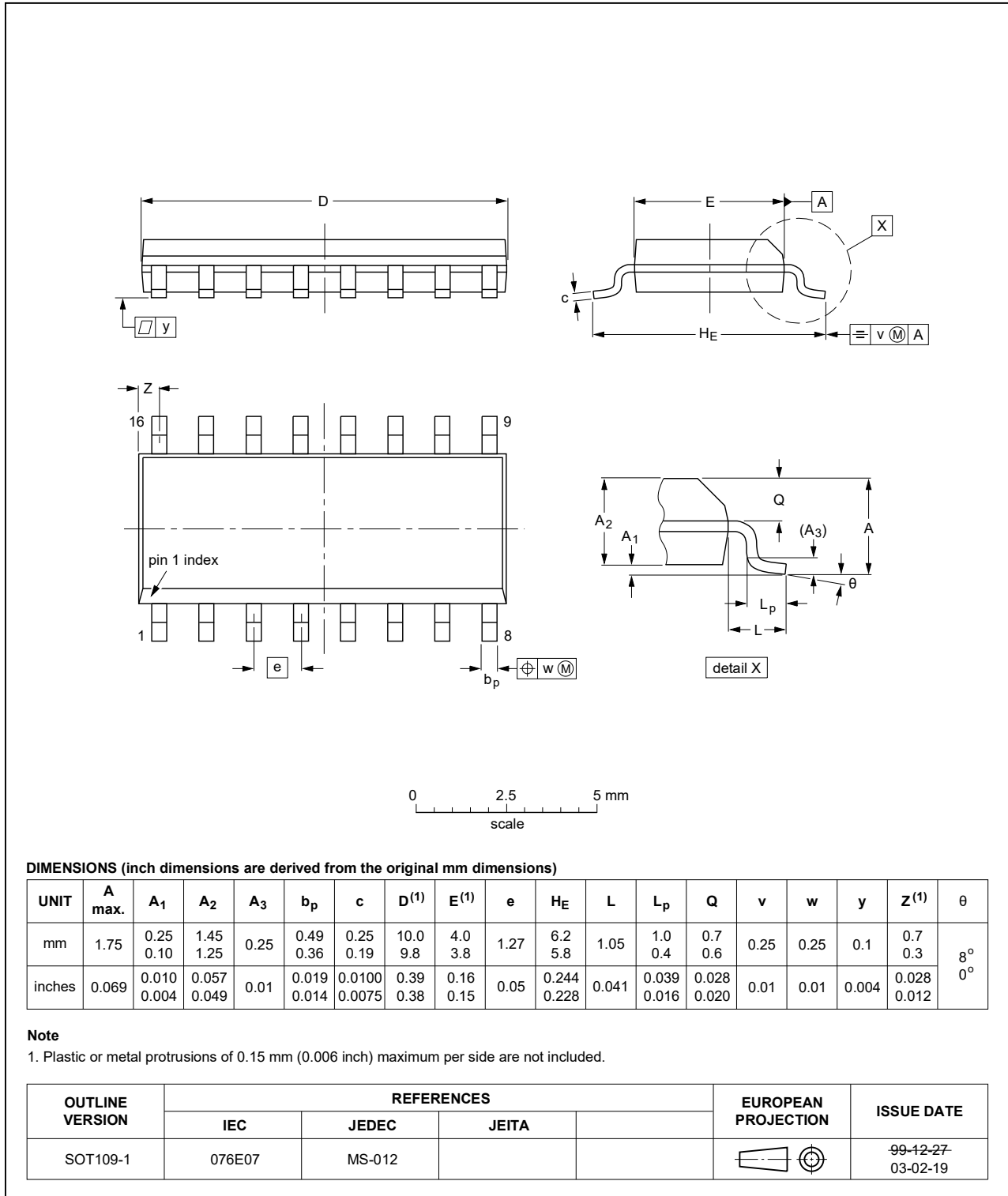


Fig. 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

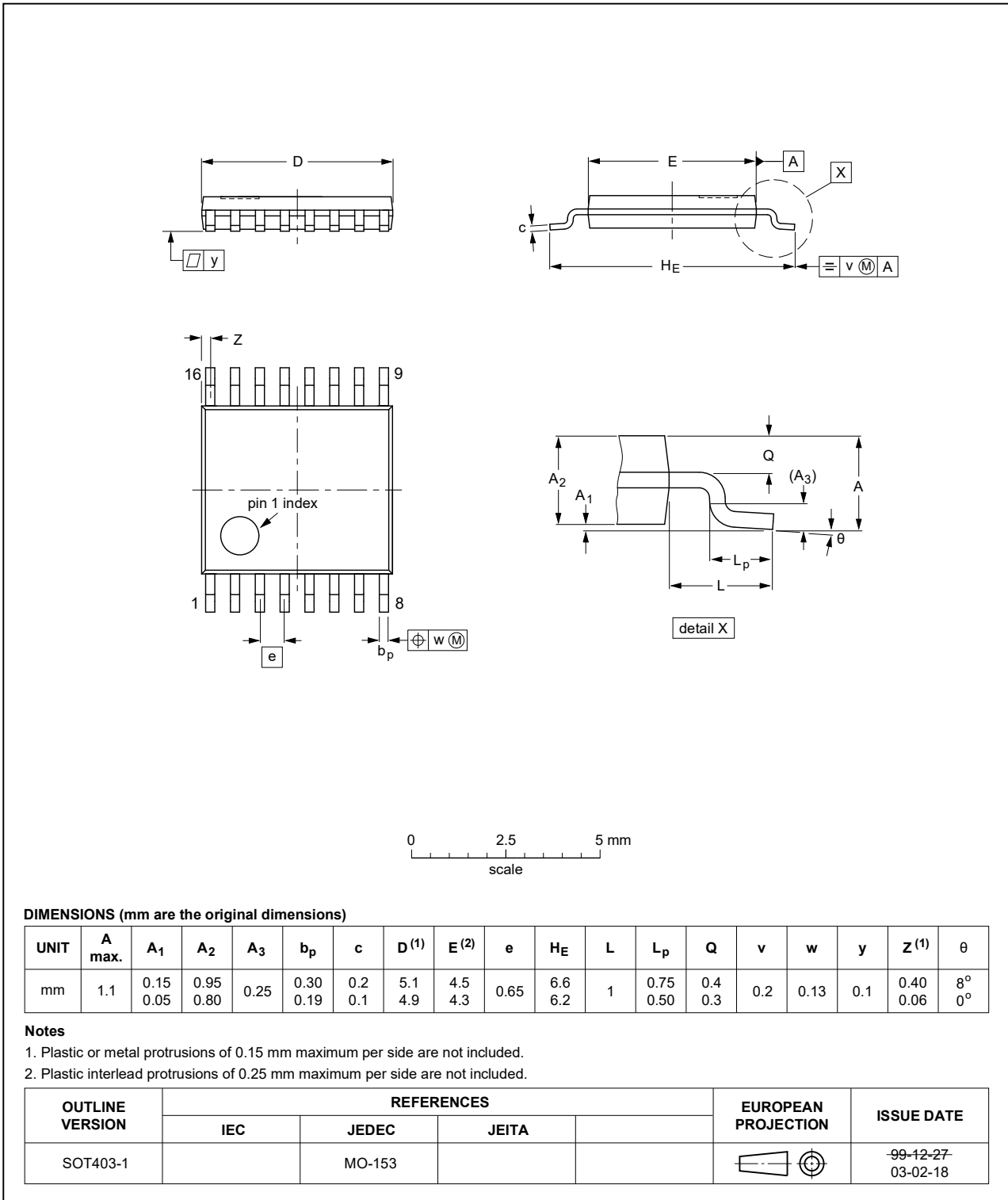


Fig. 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

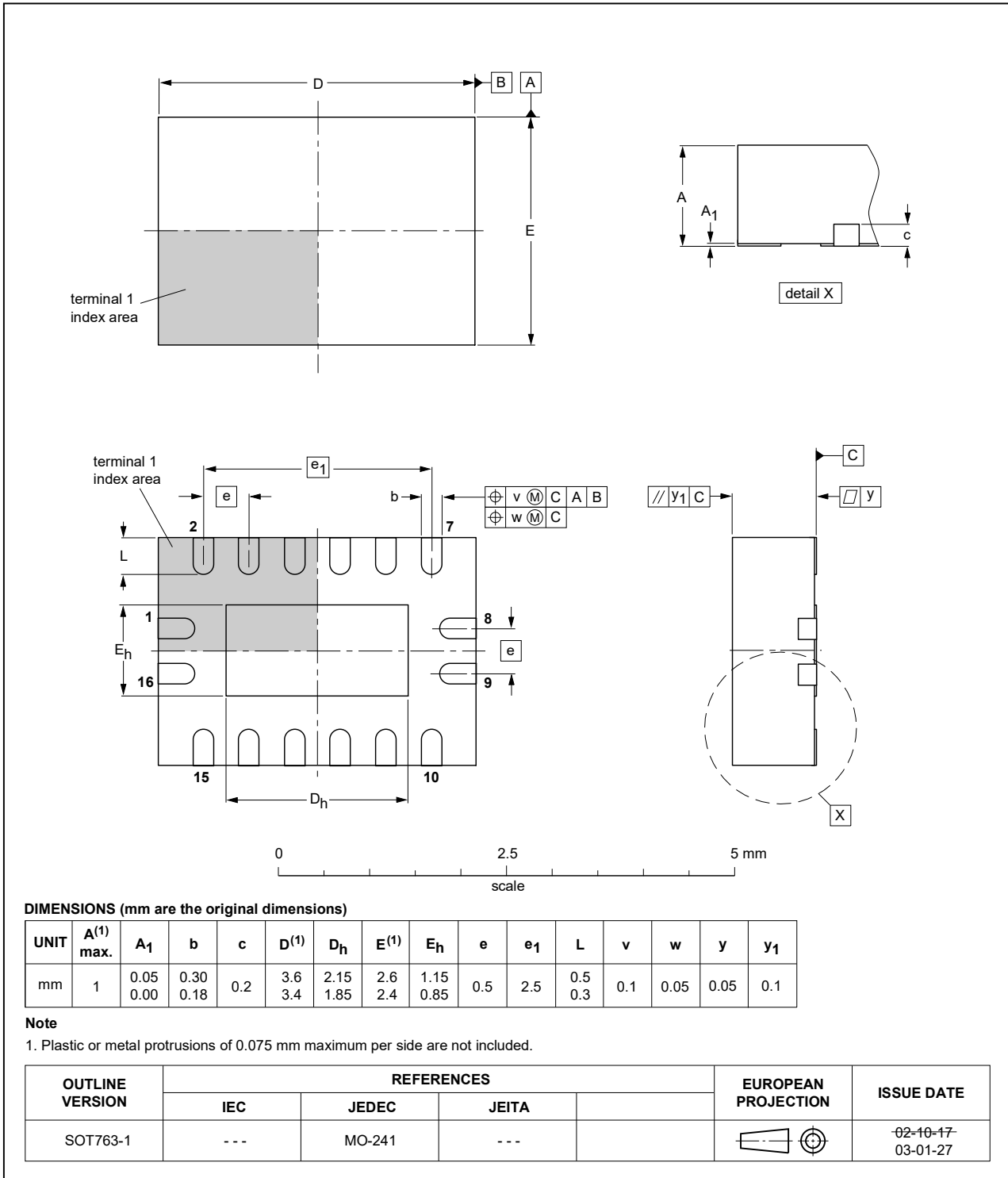


Fig. 12. Package outline SOT763-1 (DHVQFN16)

## 12. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC157A v.10	20210920	Product data sheet	-	74LVC157A v.9
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVC157ADB (SOT338-1/SSOP16) removed.</li> <li><a href="#">Section 1</a> updated.</li> </ul>			
74LVC157A v.9	20200319	Product data sheet	-	74LVC157A v.8
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74LVC157A v.8	20171011	Product data sheet	-	74LVC157A v.7
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LVC157A v.7	20111125	Product data sheet	-	74LVC157A v.6
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: maximum values for lower voltage ranges changed (errata).</li> </ul>			
74LVC157A v.6	20111027	Product data sheet	-	74LVC157A v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, and <a href="#">Table 8</a>: values added for lower voltage ranges.</li> </ul>			
74LVC157A v.5	031202	Product specification	-	74LVC157A v.4
74LVC157A v.4	030617	Product specification	-	74LVC157A v.3
74LVC157A v.3	020315	Product specification	-	74LVC157A v.2
74LVC157A v.2	980729	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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