

# 74LVC16245A-Q100; 74LVCH16245A-Q100

16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Rev. 3 — 24 September 2021

Product data sheet

## 1. General description

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The 74LVC16245A-Q100; 74LVCH16245A-Q100 is a 16-bit transceiver with 3-state outputs. The device can be used as two 8-bit transceivers or one 16-bit transceiver. The device features two output enables (1OE and 2OE) each controlling eight outputs, and two send/receive (1DIR and 2DIR) inputs for direction control. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power dissipation
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16245A-Q100 only)
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
  - CDM ANSI/ESDA/Jedec JS-002 exceeds 1000 V

### 3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74LVC16245ADGG-Q100	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16245ADGG-Q100				
74LVC16245ADGV-Q100	-40 °C to +125 °C	TVSOP48	plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm	SOT480-1
74LVCH16245ADGV-Q100				

### 4. Functional diagram

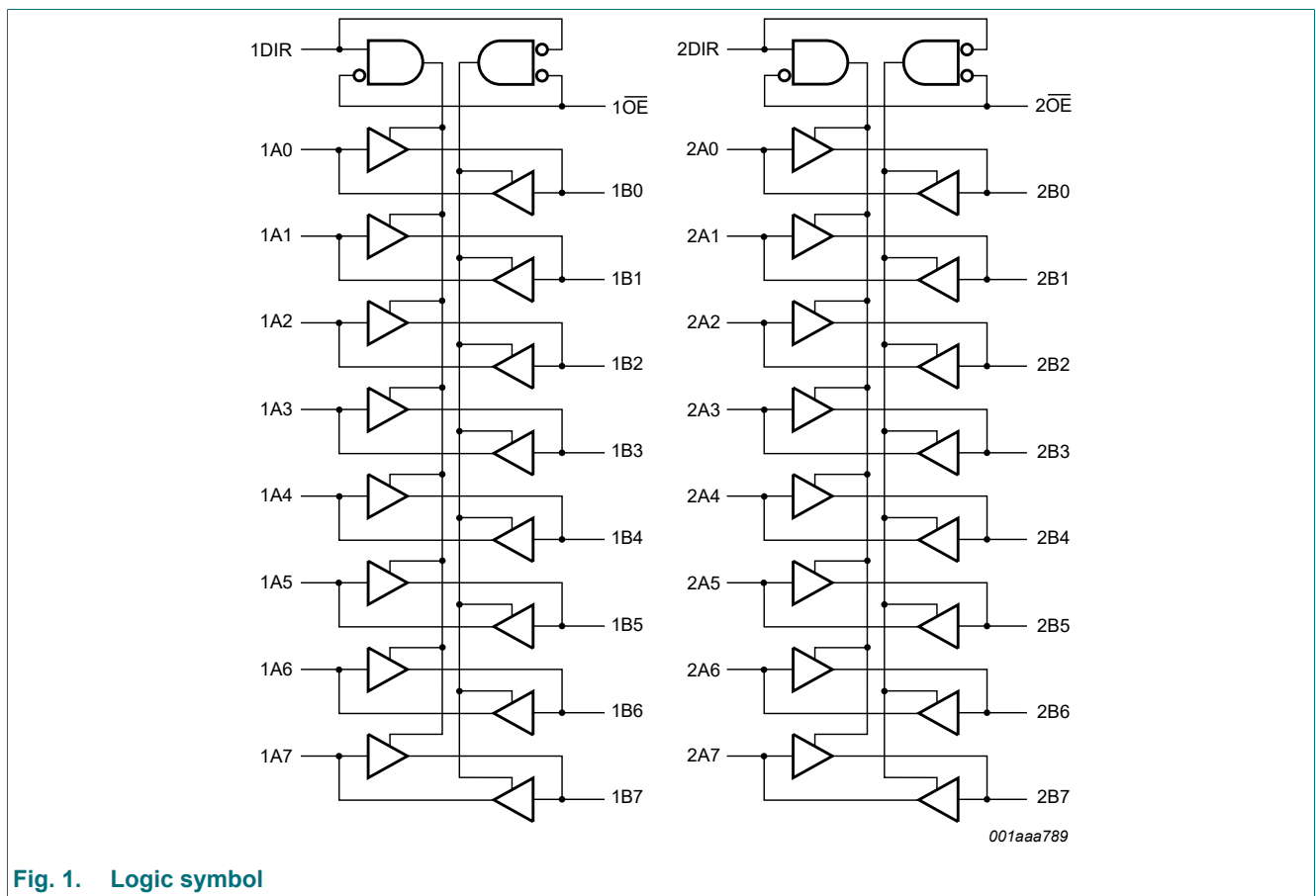


Fig. 1. Logic symbol

16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

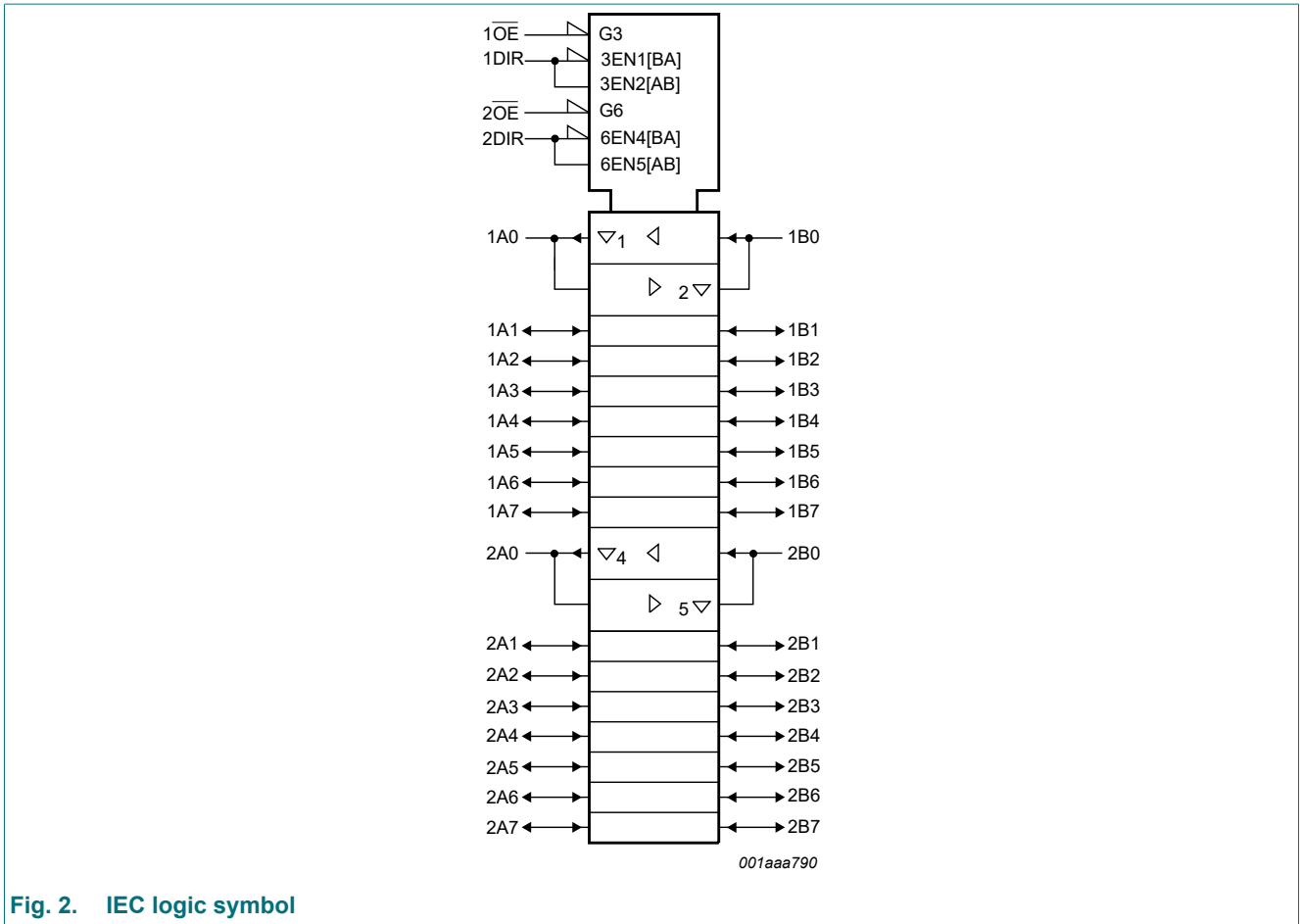


Fig. 2. IEC logic symbol

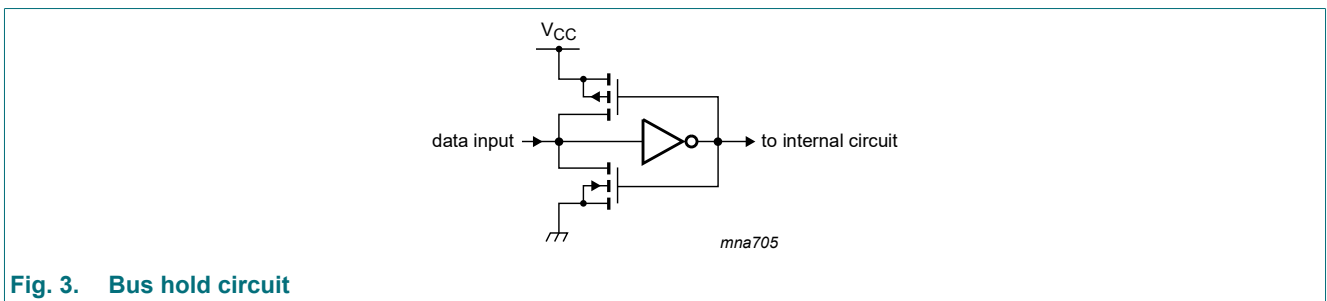


Fig. 3. Bus hold circuit

## 5. Pinning information

### 5.1. Pinning

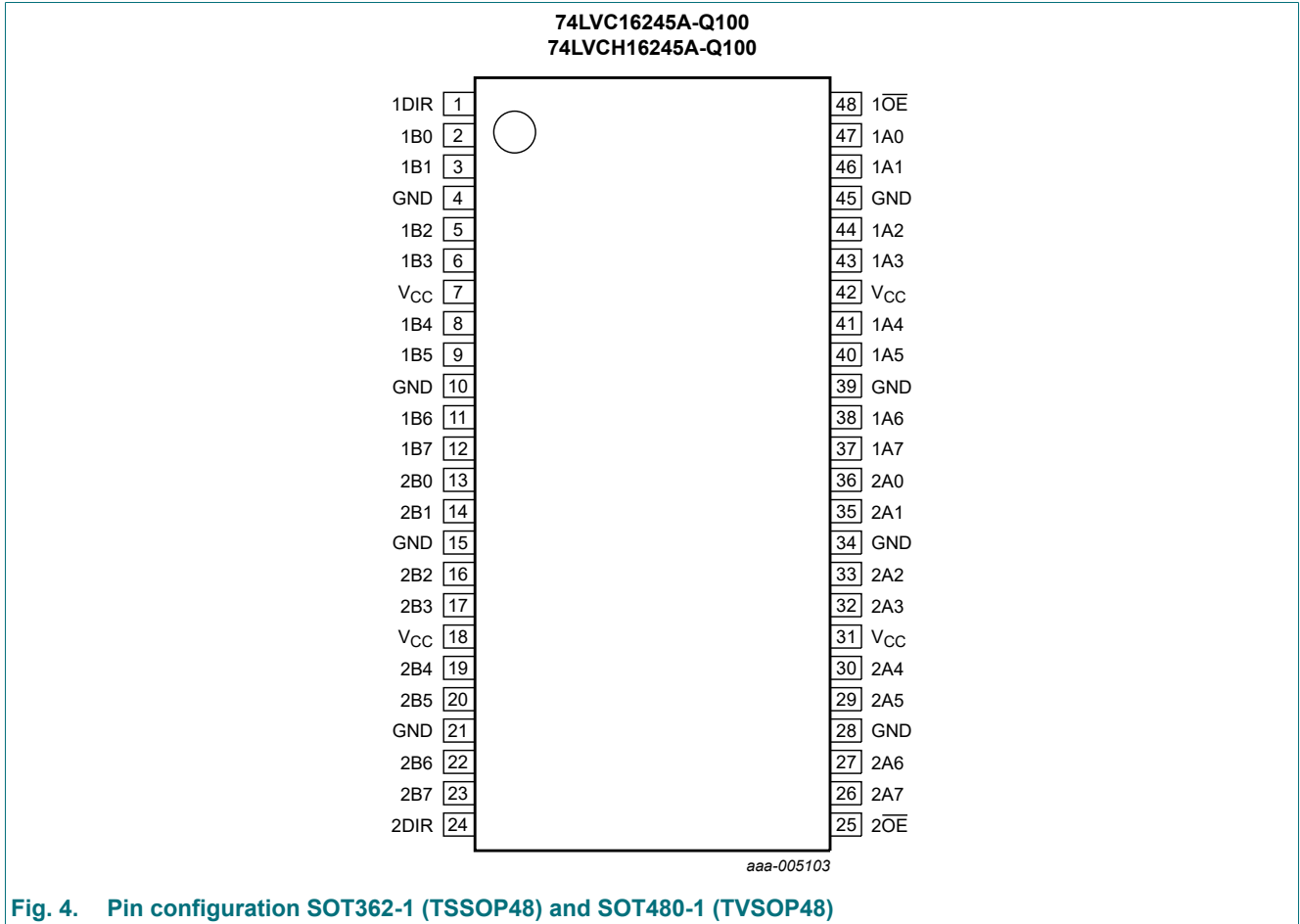


Fig. 4. Pin configuration SOT362-1 (TSSOP48) and SOT480-1 (TVSOP48)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1OE, 2OE	48, 25	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs		Outputs	
nOE	nDIR	nAn	nBn
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA	
V <sub>I</sub>	input voltage	[1]	-0.5	+6.5	V	
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA	
V <sub>O</sub>	output voltage	output HIGH or LOW	[2]	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state	[2]	-0.5	+6.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA	
I <sub>CC</sub>	supply current		-	100	mA	
I <sub>GND</sub>	ground current		-100	-	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT362-1 (TSSOP48) packages: P<sub>tot</sub> derates linearly with 12.2 mW/K above 109 °C.

For SOT480-1 (TVSOP48) packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.2 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V [2]	-	±0.1	±5	-	±20	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V [2][3]	-	±0.1	±5	-	±20	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0.0 V	-	±0.1	±10	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.6 V	-	0.1	20	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.7 V to 3.6 V	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	10	-	-	-	pF
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 1.65; V <sub>I</sub> = 0.58 V [4][5]	10	-	-	10	-	μA
		V <sub>CC</sub> = 2.3; V <sub>I</sub> = 0.7 V	30	-	-	25	-	μA
		V <sub>CC</sub> = 3.0; V <sub>I</sub> = 0.8 V	75	-	-	60	-	μA

16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 1.65; V <sub>I</sub> = 1.07 V [4][5]	-10	-	-	-10	-	µA
		V <sub>CC</sub> = 2.3; V <sub>I</sub> = 1.7 V	-30	-	-	-25	-	µA
		V <sub>CC</sub> = 3.0; V <sub>I</sub> = 2.0 V	-75	-	-	-60	-	µA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 1.95 V [4][6]	200	-	-	200	-	µA
		V <sub>CC</sub> = 2.7 V	300	-	-	300	-	µA
		V <sub>CC</sub> = 3.6 V	500	-	-	500	-	µA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 1.95 V [4][6]	-200	-	-	-200	-	µA
		V <sub>CC</sub> = 2.7 V	-300	-	-	-300	-	µA
		V <sub>CC</sub> = 3.6 V	-500	-	-	-500	-	µA

- [1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.
- [2] The bus hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.
- [3] For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.
- [4] Valid for data inputs of bus hold parts only (74LVCH16245A-Q100). Note that control inputs do not have a bus hold circuit.
- [5] The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
- [6] The specified overdrive current at the data input forces the data input to the opposite input state.

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

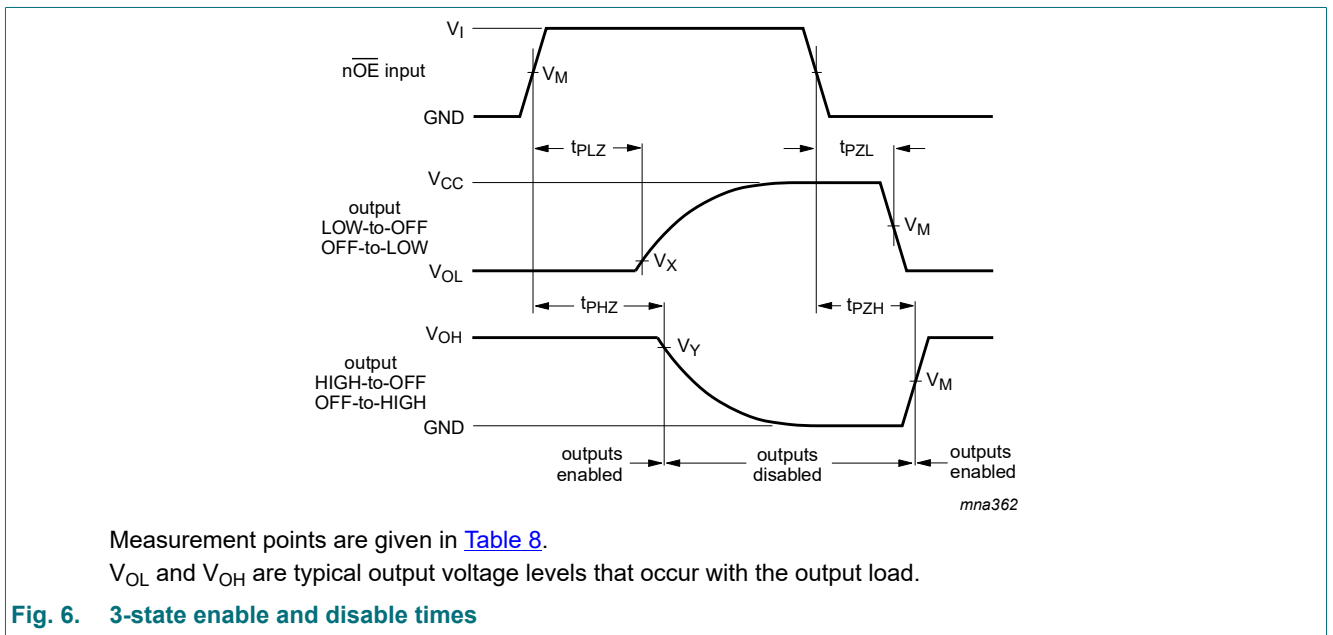
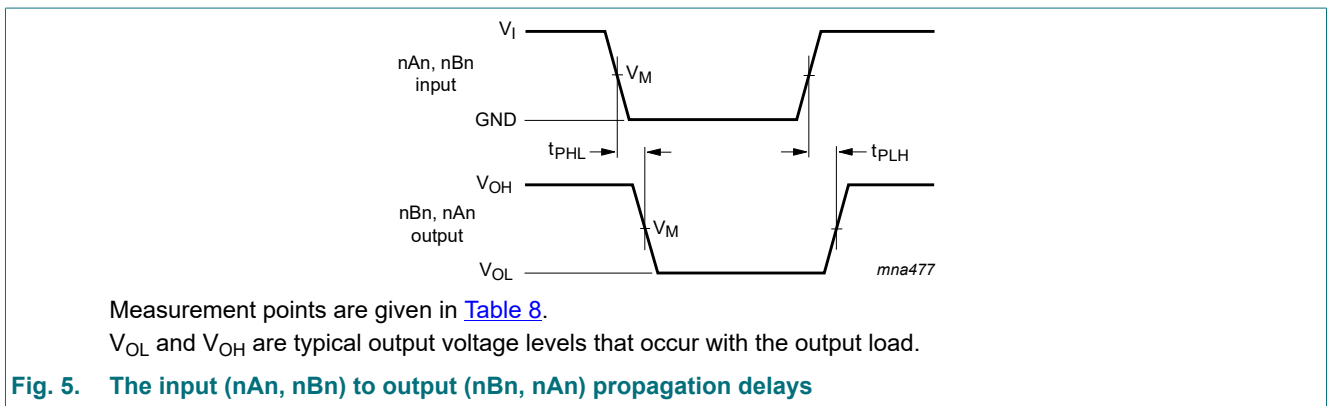
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn to nBn; nBn to nAn; see Fig. 5 [2]						
		V <sub>CC</sub> = 1.2 V	-	13.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	5.2	12.2	1.5	13.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.8	6.0	1.0	6.7	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.7	4.7	1.0	6.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.4	4.5	1.0	6.0	ns
t <sub>en</sub>	enable time	nOE to nAn, nBn; see Fig. 6 [2]						
		V <sub>CC</sub> = 1.2 V	-	15.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	5.9	15.0	1.5	16.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.3	7.9	1.0	8.8	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.5	6.7	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.7	5.5	1.0	7.0	ns
t <sub>dis</sub>	disable time	nOE to nAn, nBn; see Fig. 6 [2]						
		V <sub>CC</sub> = 1.2 V	-	11.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	4.9	13.1	1.0	14.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	2.7	7.1	0.5	7.9	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.4	6.6	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	3.3	5.6	1.5	7.0	ns

16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub> [3]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	11.5	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	15.2	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	18.5	-	-	-	pF

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in Volts  
 N = number of inputs switching  
 Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

10.1. Waveforms and test circuit

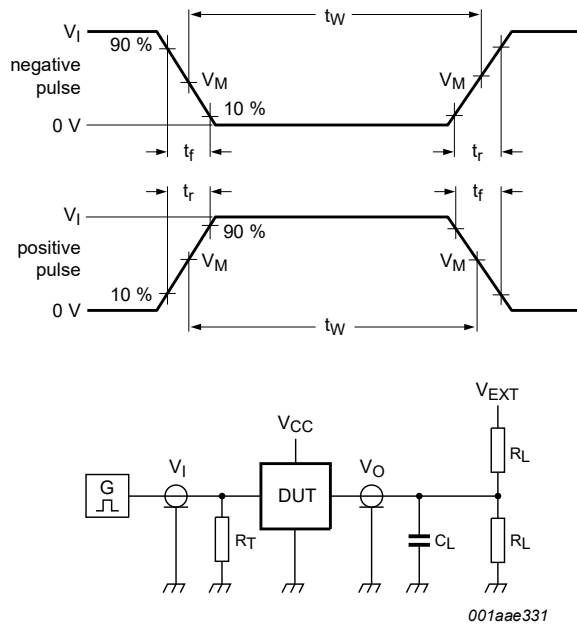




16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Table 8. Measurement points

Supply voltage	Input		Output		
$V_{CC}$	$V_M$	$V_I$	$V_M$	$V_X$	$V_Y$
1.2 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	2.7 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

### 11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

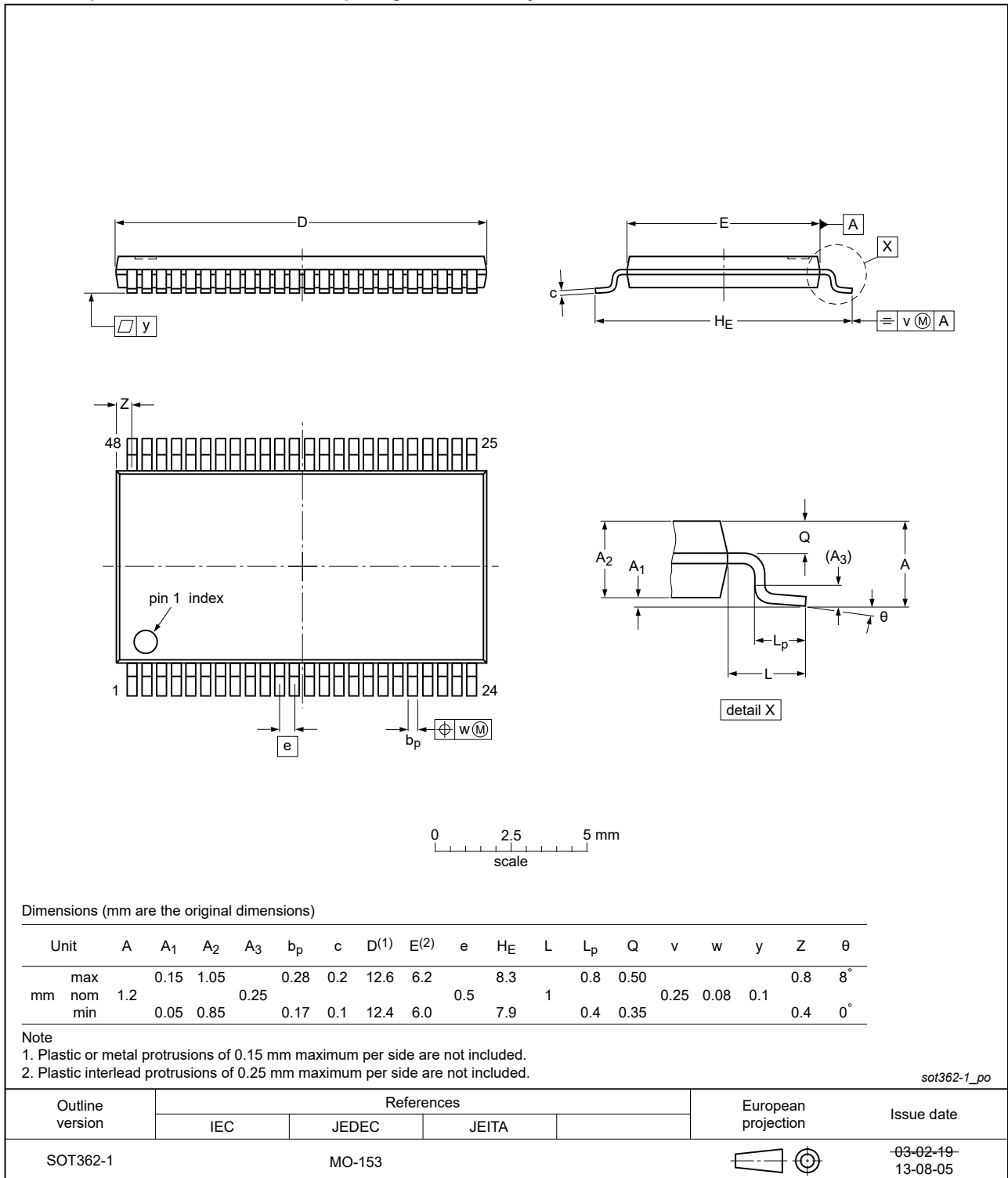


Fig. 8. Package outline SOT362-1 (TSSOP48)

16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

TVSOP48: plastic thin shrink small outline package; 48 leads;  
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1

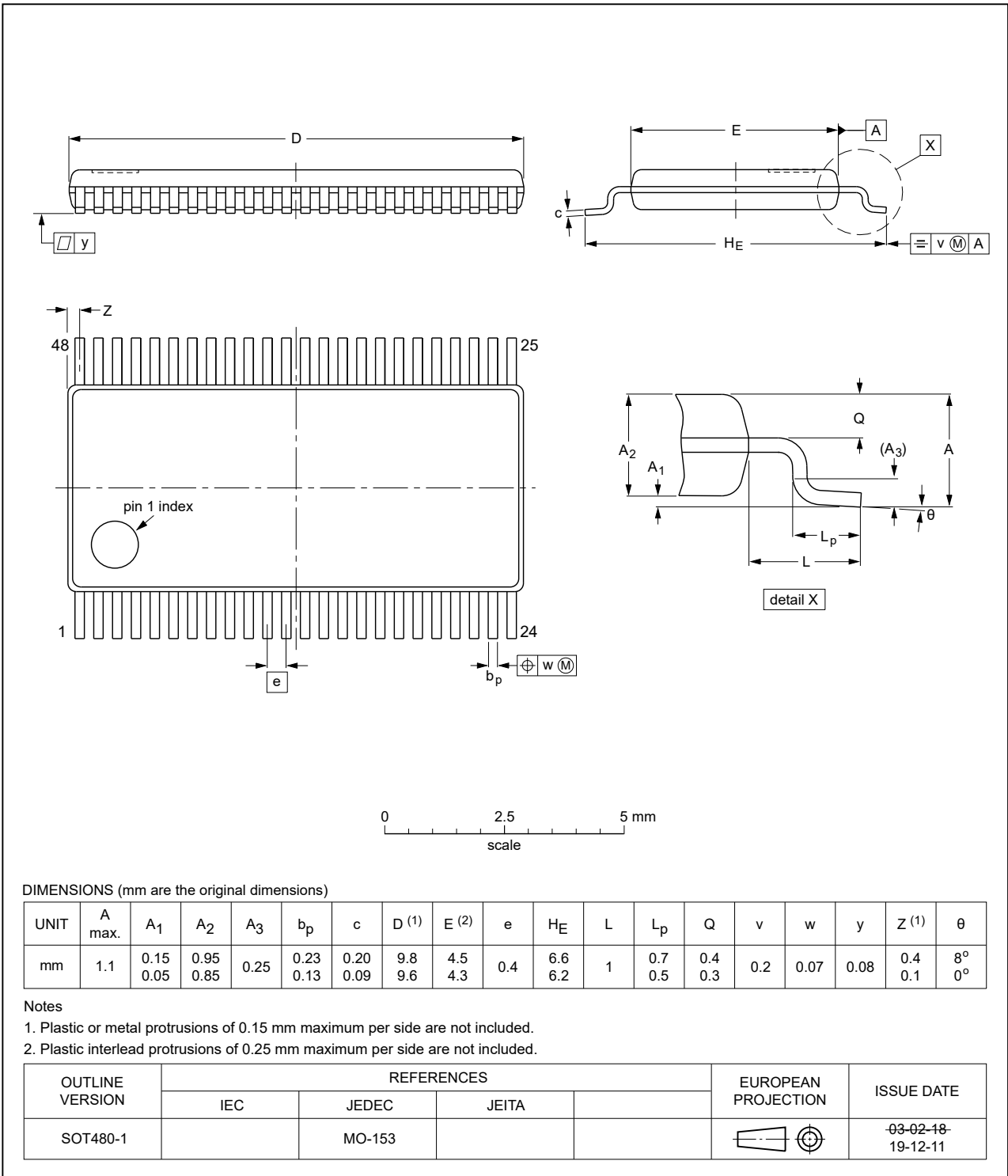


Fig. 9. Package outline SOT480-1 (TVSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16245A_Q100 v.3	20210924	Product data sheet	-	74LVC_LVCH16245A_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li>• <a href="#">Fig. 9</a>: Package outline drawing SOT480-1 (TVSOP48) updated.</li> </ul>			
74LVC_LVCH16245A_Q100 v.2	20190104	Product data sheet	-	74LVC_LVCH16245A_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Type numbers 74LVC16245AEV-Q100 and 74LVCH16245AEV-Q100 (SOT702-1) removed.</li> <li>• Type numbers 74LVC16245ADGV-Q100 and 74LVCH16245ADGV-Q100 (SOT480-1) added.</li> <li>• Package outline drawing <a href="#">Fig. 8</a> (TSSOP48) updated.</li> </ul>			
74LVC_LVCH16245A_Q100 v.1	20121120	Product data sheet	-	-

## 16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

## 14. Legal information

## Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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