# 74LVC8T245; 74LVCH8T245

## 8-bit dual supply translating transceiver; 3-state

Rev. 5 — 29 April 2021 Product data sheet

## 1. General description

The 74LVC8T245; 74LVCH8T245 are 8-bit dual supply translating transceivers with 3-state outputs that enable bidirectional level translation. They feature two data input-output ports (pins An and Bn), a direction control input (DIR), an output enable input ($\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2 V and 5.5 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An, $\overline{OE}$ and DIR are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input ($\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The devices are fully specified for partial power-down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the 74LVCH8T245 holds unused or floating data inputs at a valid logic level.

## 2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2 V to 5.5 V
  - $V_{CC(B)}$: 1.2 V to 5.5 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Maximum data rates:
  - 420 Mbps (3.3 V to 5.0 V translation)
  - 210 Mbps (translate to 3.3 V)
  - 140 Mbps (translate to 2.5 V)
  - 75 Mbps (translate to 1.8 V)
  - 60 Mbps (translate to 1.5 V)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- ±24 mA output drive ($V_{CC}$ = 3.0 V)
- Inputs accept voltages up to 5.5 V
- Low power consumption: 30 µA maximum $I_{CC}$
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC8T245PW | -40 °C to +125 °C | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |
| 74LVCH8T245PW | | | | |
| 74LVC8T245BQ | -40 °C to +125 °C | DHVQFN24 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm | SOT815-1 |
| 74LVCH8T245BQ | | | | |
| 74LVC8T245BZ | -40 °C to +125 °C | DHXQFN24 | plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 24 terminals; 0.4 mm pitch; body 2 mm × 4 mm × 0.48 mm | SOT8024-1 |

## 4. Functional diagram

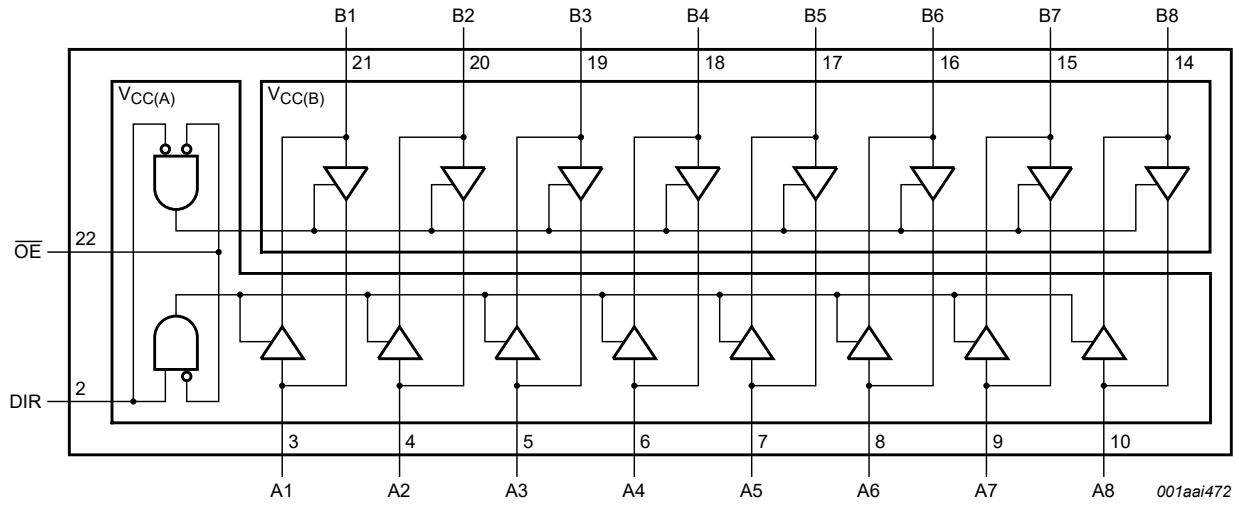



**Fig. 1. Logic symbol**

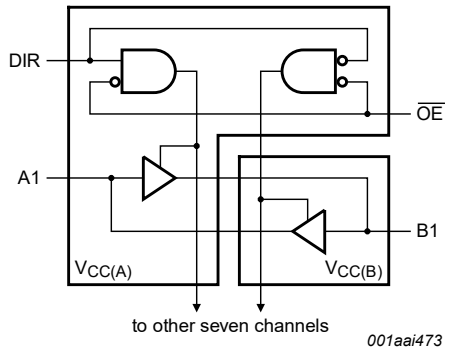



**Fig. 2. Logic diagram (one channel)**

# 5. Pinning information

## 5.1. Pinning

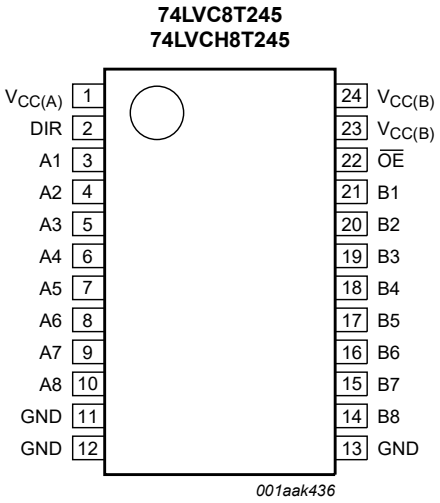
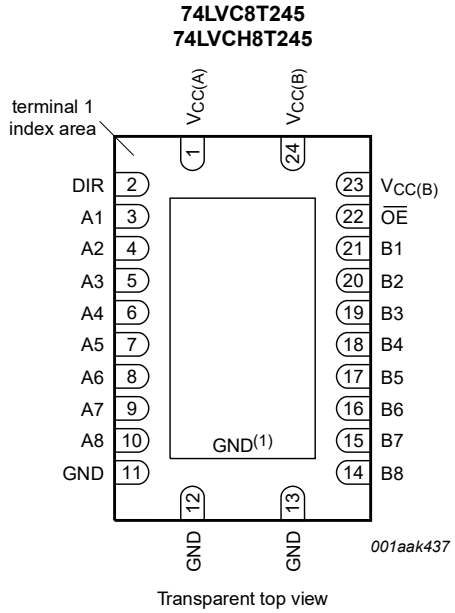


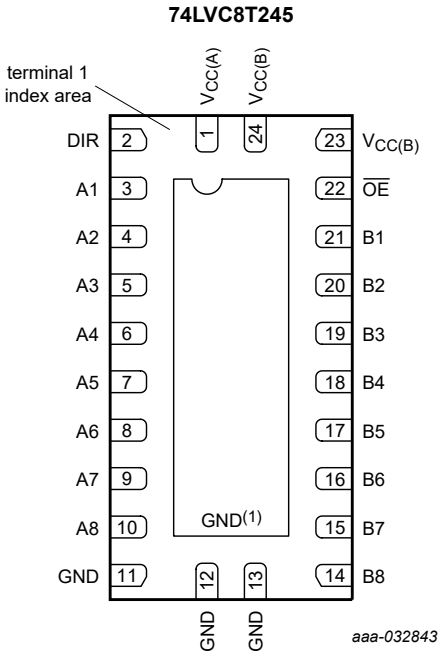

**Fig. 3. Pin configuration SOT355-1 (TSSOP24)**




Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

**Fig. 4. Pin configuration SOT815-1 (DHVQFN24)**




Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

**Fig. 5. Pin configuration SOT8024-1 (DHXQFN24)**

### 5.2. Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $V_{CC(A)}$ | 1 | supply voltage A<br>(An inputs/outputs, $\overline{OE}$ and DIR inputs are referenced to $V_{CC(A)}$) |
| DIR | 2 | direction control |
| A1, A2, A3, A4,<br>A5, A6, A7, A8 | 3, 4, 5, 6,<br>7, 8, 9, 10 | data input or output |
| GND [1] | 11, 12, 13 | ground (0 V) |
| B1, B2, B3, B4,<br>B5, B6, B7, B8 | 21, 20, 19, 18,<br>17, 16, 15, 14 | data input or output |
| $\overline{OE}$ | 22 | output enable input (active LOW) |
| $V_{CC(B)}$ | 23, 24 | supply voltage B (Bn inputs/outputs are referenced to $V_{CC(B)}$) |

[1] All GND pins must be connected to ground (0 V).

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

| Supply voltage | Input | | Input/output [1] | |
|---|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | $\overline{OE}$ [2] | DIR [2] | An [2] | Bn [2] |
| 1.2 V to 5.5 V | L | L | An = Bn | input |
| 1.2 V to 5.5 V | L | H | input | Bn = An |
| 1.2 V to 5.5 V | H | X | Z | Z |
| GND [1] | X | X | Z | Z |

[1] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.
[2] The An inputs/outputs, DIR and $\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The Bn inputs/outputs circuit is referenced to $V_{CC(B)}$.

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC(A)}$ | supply voltage A | | | -0.5 | +6.5 | V |
| $V_{CC(B)}$ | supply voltage B | | | -0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I$ < 0 V | | -50 | - | mA |
| $V_I$ | input voltage | | [1] | -0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O$ < 0 V | | -50 | - | mA |
| $V_O$ | output voltage | Active mode | [1] [2] [3] | -0.5 | $V_{CCO}$ + 0.5 | V |
| | | Suspend or 3-state mode | [1] | -0.5 | +6.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CCO}$ | [2] | - | ±50 | mA |
| $I_{CC}$ | supply current | $I_{CC(A)}$ or $I_{CC(B)}$; per $V_{CC}$ pin | | - | 100 | mA |
| $I_{GND}$ | ground current | per GND pin | | -100 | - | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C | | | | |
| | | SOT355-1; SOT815-1 | [4] | - | 500 | mW |
| | | SOT8024-1 | | - | 250 | mW |

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] $V_{CCO}$ is the supply voltage associated with the output port.
[3] $V_{CCO}$ + 0.5 V should not exceed 6.5 V.
[4] For SOT355-1 (TSSOP24) package: $P_{tot}$ derates linearly with 12.4 mW/K above 110 °C.
For SOT815-1 (DHVQFN24) package: $P_{tot}$ derates linearly with 15.0 mW/K above 117 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC(A)}$ | supply voltage A | | | 1.2 | 5.5 | V |
| $V_{CC(B)}$ | supply voltage B | | | 1.2 | 5.5 | V |
| $V_I$ | input voltage | | | 0 | 5.5 | V |
| $V_O$ | output voltage | Active mode | [1] | 0 | $V_{CCO}$ | V |
| | | Suspend or 3-state mode | | 0 | 5.5 | V |
| $T_{amb}$ | ambient temperature | | | -40 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CCI}$ = 1.2 V | [2] | - | 20 | ns/V |
| | | $V_{CCI}$ = 1.4 V to 1.95 V | | - | 20 | ns/V |
| | | $V_{CCI}$ = 2.3 V to 2.7 V | | - | 20 | ns/V |
| | | $V_{CCI}$ = 3 V to 3.6 V | | - | 10 | ns/V |
| | | $V_{CCI}$ = 4.5 V to 5.5 V | | - | 5 | ns/V |

[1] $V_{CCO}$ is the supply voltage associated with the output port.
[2] $V_{CCI}$ is the supply voltage associated with the input port.

# 9. Static characteristics

**Table 6. Typical static characteristics at $T_{amb}$ = 25 °C**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | [1] | | | | |
| | | $I_O$ = -3 mA; $V_{CCO}$ = 1.2 V | | - | 1.09 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 3 mA; $V_{CCO}$ = 1.2 V | [1] | - | 0.07 | - | V |
| $I_I$ | input leakage current | DIR, $\overline{OE}$ input; $V_I$ = 0 V to 5.5 V; $V_{CCI}$ = 1.2 V to 5.5 V | [2] | - | - | ±1 | µA |
| $I_{BHL}$ | bus hold LOW current | A or B port; $V_I$ = 0.42 V; $V_{CCI}$ = 1.2 V | [2] | - | 19 | - | µA |
| $I_{BHH}$ | bus hold HIGH current | A or B port; $V_I$ = 0.78 V; $V_{CCI}$ = 1.2 V | [2] | - | -19 | - | µA |
| $I_{BHLO}$ | bus hold LOW overdrive current | A or B port; $V_{CCI}$ = 1.2 V | [2] [3] | - | 19 | - | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | A or B port; $V_{CCI}$ = 1.2 V | [2] [3] | - | -19 | - | µA |
| $I_{OZ}$ | OFF-state output current | A or B port; $V_O$ = 0 V or $V_{CCO}$; $V_{CCO}$ = 1.2 V to 5.5 V | [1] | - | - | ±1 | µA |
| | | suspend mode A port; $V_O$ = 0 V or $V_{CCO}$; $V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V | [1] | - | - | ±1 | µA |
| | | suspend mode B port; $V_O$ = 0 V or $V_{CCO}$; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V | [1] | - | - | ±1 | µA |
| $I_{OFF}$ | power-off leakage current | A port; $V_I$ or $V_O$ = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 1.2 V to 5.5 V | | - | - | ±1 | µA |
| | | B port; $V_I$ or $V_O$ = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 1.2 V to 5.5 V | | - | - | ±1 | µA |
| $C_I$ | input capacitance | DIR, $\overline{OE}$ input; $V_I$ = 0 V or 3.3 V; $V_{CC(A)}$ = 3.3 V | | - | 3 | - | pF |
| $C_{I/O}$ | input/output capacitance | A and B port; $V_O$ = 3.3 V or 0 V; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V | | - | 6.5 | - | pF |

[1] $V_{CCO}$ is the supply voltage associated with the output port.
[2] $V_{CCI}$ is the supply voltage associated with the data input port.
[3] To guarantee the node switches, an external driver must source/sink at least $I_{BHLO}$ / $I_{BHHO}$ when the input is in the range $V_{IL}$ to $V_{IH}$.

**Table 7. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | data input [1] | | | | | |
| | | $V_{CCI}$ = 1.2 V | $0.8V_{CCI}$ | - | $0.8V_{CCI}$ | - | V |
| | | $V_{CCI}$ = 1.4 V to 1.95 V | $0.65V_{CCI}$ | - | $0.65V_{CCI}$ | - | V |
| | | $V_{CCI}$ = 2.3 V to 2.7 V | 1.7 | - | 1.7 | - | V |
| | | $V_{CCI}$ = 3.0 V to 3.6 V | 2.0 | - | 2.0 | - | V |
| | | $V_{CCI}$ = 4.5 V to 5.5 V | $0.7V_{CCI}$ | - | $0.7V_{CCI}$ | - | V |
| | | DIR, $\overline{OE}$ input | | | | | |
| | | $V_{CCI}$ = 1.2 V | $0.8V_{CC(A)}$ | - | $0.8V_{CC(A)}$ | - | V |
| | | $V_{CCI}$ = 1.4 V to 1.95 V | $0.65V_{CC(A)}$ | - | $0.65V_{CC(A)}$ | - | V |
| | | $V_{CCI}$ = 2.3 V to 2.7 V | 1.7 | - | 1.7 | - | V |
| | | $V_{CCI}$ = 3.0 V to 3.6 V | 2.0 | - | 2.0 | - | V |
| | | $V_{CCI}$ = 4.5 V to 5.5 V | $0.7V_{CC(A)}$ | - | $0.7V_{CC(A)}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | data input [1] | | | | | |
| | | $V_{CCI}$ = 1.2 V | - | $0.2V_{CCI}$ | - | $0.2V_{CCI}$ | V |
| | | $V_{CCI}$ = 1.4 V to 1.95 V | - | $0.35V_{CCI}$ | - | $0.35V_{CCI}$ | V |
| | | $V_{CCI}$ = 2.3 V to 2.7 V | - | 0.7 | - | 0.7 | V |
| | | $V_{CCI}$ = 3.0 V to 3.6 V | - | 0.8 | - | 0.8 | V |
| | | $V_{CCI}$ = 4.5 V to 5.5 V | - | $0.3V_{CCI}$ | - | $0.3V_{CCI}$ | V |
| | | DIR, $\overline{OE}$ input | | | | | |
| | | $V_{CCI}$ = 1.2 V | - | $0.2V_{CC(A)}$ | - | $0.2V_{CC(A)}$ | V |
| | | $V_{CCI}$ = 1.4 V to 1.95 V | - | $0.35V_{CC(A)}$ | - | $0.35V_{CC(A)}$ | V |
| | | $V_{CCI}$ = 2.3 V to 2.7 V | - | 0.7 | - | 0.7 | V |
| | | $V_{CCI}$ = 3.0 V to 3.6 V | - | 0.8 | - | 0.8 | V |
| | | $V_{CCI}$ = 4.5 V to 5.5 V | - | $0.3V_{CC(A)}$ | - | $0.3V_{CC(A)}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ | | | | | |
| | | $I_O$ = -100 µA; $V_{CCO}$ = 1.2 V to 4.5 V [2] | $V_{CCO}$ - 0.1 | - | $V_{CCO}$ - 0.1 | - | V |
| | | $I_O$ = -6 mA; $V_{CCO}$ = 1.4 V | 1.0 | - | 1.0 | - | V |
| | | $I_O$ = -8 mA; $V_{CCO}$ = 1.65 V | 1.2 | - | 1.2 | - | V |
| | | $I_O$ = -12 mA; $V_{CCO}$ = 2.3 V | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = -24 mA; $V_{CCO}$ = 3.0 V | 2.4 | - | 2.4 | - | V |
| | | $I_O$ = -32 mA; $V_{CCO}$ = 4.5 V | 3.8 | - | 3.8 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IL}$ [2] | | | | | |
| | | $I_O$ = 100 µA; $V_{CCO}$ = 1.2 V to 4.5 V | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 6 mA; $V_{CCO}$ = 1.4 V | - | 0.3 | - | 0.3 | V |
| | | $I_O$ = 8 mA; $V_{CCO}$ = 1.65 V | - | 0.45 | - | 0.45 | V |
| | | $I_O$ = 12 mA; $V_{CCO}$ = 2.3 V | - | 0.3 | - | 0.3 | V |
| | | $I_O$ = 24 mA; $V_{CCO}$ = 3.0 V | - | 0.55 | - | 0.55 | V |
| | | $I_O$ = 32 mA; $V_{CCO}$ = 4.5 V | - | 0.55 | - | 0.55 | V |
| $I_I$ | input leakage current | DIR, $\overline{OE}$ input; $V_I$ = 0 V to 5.5 V; $V_{CCI}$ = 1.2 V to 5.5 V | - | ±2 | - | ±10 | µA |

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $I_{BHL}$ | bus hold LOW current | A or B port [1] | | | | | |
| | | $V_I$ = 0.49 V; $V_{CCI}$ = 1.4 V | 15 | - | 10 | - | µA |
| | | $V_I$ = 0.58 V; $V_{CCI}$ = 1.65 V | 25 | - | 20 | - | µA |
| | | $V_I$ = 0.70 V; $V_{CCI}$ = 2.3 V | 45 | - | 45 | - | µA |
| | | $V_I$ = 0.80 V; $V_{CCI}$ = 3.0 V | 100 | - | 80 | - | µA |
| | | $V_I$ = 1.35 V; $V_{CCI}$ = 4.5 V | 100 | - | 100 | - | µA |
| $I_{BHH}$ | bus hold HIGH current | A or B port [1] | | | | | |
| | | $V_I$ = 0.91 V; $V_{CCI}$ = 1.4 V | -15 | - | -10 | - | µA |
| | | $V_I$ = 1.07 V; $V_{CCI}$ = 1.65 V | -25 | - | -20 | - | µA |
| | | $V_I$ = 1.70 V; $V_{CCI}$ = 2.3 V | -45 | - | -45 | - | µA |
| | | $V_I$ = 2.00 V; $V_{CCI}$ = 3.0 V | -100 | - | -80 | - | µA |
| | | $V_I$ = 3.15 V; $V_{CCI}$ = 4.5 V | -100 | - | -100 | - | µA |
| $I_{BHLO}$ | bus hold LOW overdrive current | A or B port [1] [3] | | | | | |
| | | $V_{CCI}$ = 1.6 V | 125 | - | 125 | - | µA |
| | | $V_{CCI}$ = 1.95 V | 200 | - | 200 | - | µA |
| | | $V_{CCI}$ = 2.7 V | 300 | - | 300 | - | µA |
| | | $V_{CCI}$ = 3.6 V | 500 | - | 500 | - | µA |
| | | $V_{CCI}$ = 5.5 V | 900 | - | 900 | - | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | A or B port [1] [3] | | | | | |
| | | $V_{CCI}$ = 1.6 V | -125 | - | -125 | - | µA |
| | | $V_{CCI}$ = 1.95 V | -200 | - | -200 | - | µA |
| | | $V_{CCI}$ = 2.7 V | -300 | - | -300 | - | µA |
| | | $V_{CCI}$ = 3.6 V | -500 | - | -500 | - | µA |
| | | $V_{CCI}$ = 5.5 V | -900 | - | -900 | - | µA |
| $I_{OZ}$ | OFF-state output current | A or B port; $V_O$ = 0 V or $V_{CCO}$; $V_{CCO}$ = 1.2 V to 5.5 V [2] | - | ±2 | - | ±10 | µA |
| | | suspend mode A port; $V_O$ = 0 V or $V_{CCO}$; $V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V [2] | - | ±2 | - | ±10 | µA |
| | | suspend mode B port; $V_O$ = 0 V or $V_{CCO}$; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V [2] | - | ±2 | - | ±10 | µA |
| $I_{OFF}$ | power-off leakage current | A port; $V_I$ or $V_O$ = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 1.2 V to 5.5 V | - | ±2 | - | ±10 | µA |
| | | B port; $V_I$ or $V_O$ = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 1.2 V to 5.5 V | - | ±2 | - | ±10 | µA |

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $I_{CC}$ | supply current | A port; $V_I$ = 0 V or $V_{CCI}$; $I_O$ = 0 A [1] | | | | | |
| | | $V_{CC(A)}$, $V_{CC(B)}$ = 1.2 V to 5.5 V | - | 15 | - | 20 | µA |
| | | $V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V | - | 15 | - | 20 | µA |
| | | $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V | -2 | - | -4 | - | µA |
| | | B port; $V_I$ = 0 V or $V_{CCI}$; $I_O$ = 0 A | | | | | |
| | | $V_{CC(A)}$, $V_{CC(B)}$ = 1.2 V to 5.5 V | - | 15 | - | 20 | µA |
| | | $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 5.5 V | -2 | - | -4 | - | µA |
| | | $V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 0 V | - | 15 | - | 20 | µA |
| | | A plus B port ($I_{CC(A)}$ + $I_{CC(B)}$); $I_O$ = 0 A; $V_I$ = 0 V or $V_{CCI}$ | | | | | |
| | | $V_{CC(A)}$, $V_{CC(B)}$ = 1.2 V to 5.5 V | - | 25 | - | 30 | µA |
| $\Delta I_{CC}$ | additional supply current | per input; $V_{CC(A)}$, $V_{CC(B)}$ = 3.0 V to 5.5 V | | | | | |
| | | DIR and $\overline{OE}$ input; DIR or $\overline{OE}$ input at $V_{CC(A)}$ - 0.6 V; A port at $V_{CC(A)}$ or GND; B port = open | - | 50 | - | 75 | µA |
| | | A port; A port at $V_{CC(A)}$ - 0.6 V; DIR at $V_{CC(A)}$; B port = open [4] | - | 50 | - | 75 | µA |
| | | B port; B port at $V_{CC(B)}$ - 0.6 V; DIR at GND; A port = open [4] | - | 50 | - | 75 | µA |

[1] $V_{CCI}$ is the supply voltage associated with the data input port.
[2] $V_{CCO}$ is the supply voltage associated with the output port.
[3] To guarantee the node switches, an external driver must source/sink at least $I_{BHLO}$ / $I_{BHHO}$ when the input is in the range $V_{IL}$ to $V_{IH}$.
[4] For non bus hold parts only (74LVC8T245).

## 10. Dynamic characteristics

**Table 8. Typical dynamic characteristics at $V_{CC(A)}$ = 1.2 V and $T_{amb}$ = 25 °C**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8; for wave forms see Fig. 6 and Fig. 7. [1]*

| Symbol | Parameter | Conditions | $V_{CC(B)}$ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V | |
| $t_{pd}$ | propagation delay | An to Bn | 11.0 | 8.5 | 7.4 | 6.2 | 5.7 | 5.4 | ns |
| | | Bn to An | 11.0 | 10.0 | 9.5 | 9.1 | 8.9 | 8.9 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 9.5 | 9.5 | 9.5 | 9.5 | 9.5 | 9.5 | ns |
| | | $\overline{OE}$ to Bn | 10.2 | 8.2 | 7.8 | 6.7 | 7.3 | 6.4 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 13.5 | 13.5 | 13.5 | 13.5 | 13.5 | 13.5 | ns |
| | | $\overline{OE}$ to Bn | 13.6 | 10.3 | 8.9 | 7.5 | 7.1 | 7.0 | ns |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.

**Table 9. Typical dynamic characteristics at $V_{CC(B)}$ = 1.2 V and $T_{amb}$ = 25 °C**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8; for wave forms see Fig. 6 and Fig. 7. [1]*

| Symbol | Parameter | Conditions | $V_{CC(A)}$ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V | |
| $t_{pd}$ | propagation delay | An to Bn | 11.0 | 10.0 | 9.5 | 9.1 | 8.9 | 8.8 | ns |
| | | Bn to An | 11.0 | 8.5 | 7.3 | 6.2 | 5.7 | 5.4 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 9.5 | 6.8 | 5.4 | 3.8 | 4.1 | 3.1 | ns |
| | | $\overline{OE}$ to Bn | 10.2 | 9.1 | 8.6 | 8.1 | 7.8 | 7.8 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 13.5 | 9.0 | 6.9 | 4.8 | 3.8 | 3.2 | ns |
| | | $\overline{OE}$ to Bn | 13.6 | 12.5 | 12.0 | 11.5 | 11.4 | 11.4 | ns |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.

**Table 10. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb}$ = 25 °C**

*Voltages are referenced to GND (ground = 0 V). [1] [2]*

| Symbol | Parameter | Conditions | $V_{CC(A)}$ and $V_{CC(B)}$ | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 1.8 V | 2.5 V | 3.3 V | 5.0 V | |
| $C_{PD}$ | power dissipation capacitance | A port: (direction A to B); B port: (direction B to A) | 1 | 1 | 1 | 2 | pF |
| | | A port: (direction B to A); B port: (direction A to B) | 13 | 13 | 13 | 13 | pF |

[1] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.

[2] $f_i$ = 10 MHz; $V_I$ = GND to $V_{CC}$; $t_r = t_f$ = 1 ns; $C_L$ = 0 pF; $R_L = \infty\ \Omega$.

**Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8; for waveforms see Fig. 6 and Fig. 7. [1]*

| Symbol | Parameter | Conditions | $V_{CC(B)}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.5 V ± 0.1 V | | 1.8 V ± 0.15 V | | 2.5 V ± 0.2 V | | 3.3 V ± 0.3 V | | 5.0 V ± 0.5 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| **$V_{CC(A)}$ = 1.5 V ± 0.1 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.7 | 27 | 1.7 | 23 | 1.3 | 18 | 1.0 | 15 | 0.8 | 13 | ns |
| | | Bn to An | 0.9 | 27 | 0.9 | 25 | 0.8 | 23 | 0.7 | 23 | 0.7 | 22 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 1.5 | 30 | 1.5 | 30 | 1.5 | 30 | 1.5 | 30 | 1.4 | 30 | ns |
| | | $\overline{OE}$ to Bn | 2.4 | 34 | 2.4 | 33 | 1.9 | 15 | 1.7 | 14 | 1.3 | 12 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 0.4 | 34 | 0.4 | 34 | 0.4 | 34 | 0.4 | 34 | 0.4 | 34 | ns |
| | | $\overline{OE}$ to Bn | 1.8 | 36 | 1.8 | 34 | 1.5 | 18 | 1.2 | 15 | 0.9 | 13 | ns |
| **$V_{CC(A)}$ = 1.8 V ± 0.15 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.7 | 25 | 1.7 | 21.9 | 1.3 | 9.2 | 1.0 | 7.4 | 0.8 | 7.1 | ns |
| | | Bn to An | 0.9 | 23 | 0.9 | 23.8 | 0.8 | 23.6 | 0.7 | 23.4 | 0.7 | 23.4 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 1.5 | 30 | 1.5 | 29.6 | 1.5 | 29.4 | 1.5 | 29.3 | 1.4 | 29.2 | ns |
| | | $\overline{OE}$ to Bn | 2.4 | 33 | 2.4 | 32.2 | 1.9 | 13.1 | 1.7 | 12.0 | 1.3 | 10.3 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 0.4 | 24 | 0.4 | 24.0 | 0.4 | 23.8 | 0.4 | 23.7 | 0.4 | 23.7 | ns |
| | | $\overline{OE}$ to Bn | 1.8 | 34 | 1.8 | 32.0 | 1.5 | 16.0 | 1.2 | 12.6 | 0.9 | 10.8 | ns |
| **$V_{CC(A)}$ = 2.5 V ± 0.2 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.5 | 23 | 1.5 | 21.4 | 1.2 | 9.0 | 0.8 | 6.2 | 0.6 | 4.8 | ns |
| | | Bn to An | 1.2 | 18 | 1.2 | 9.3 | 1.0 | 9.1 | 1.0 | 8.9 | 0.9 | 8.8 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 1.4 | 9.0 | 1.4 | 9.0 | 1.4 | 9.0 | 1.4 | 9.0 | 1.4 | 9.0 | ns |
| | | $\overline{OE}$ to Bn | 2.3 | 31 | 2.3 | 29.6 | 1.8 | 11.0 | 1.7 | 9.3 | 0.9 | 6.9 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 1.0 | 10.9 | 1.0 | 10.9 | 1.0 | 10.9 | 1.0 | 10.9 | 1.0 | 10.9 | ns |
| | | $\overline{OE}$ to Bn | 1.7 | 32 | 1.7 | 28.2 | 1.5 | 12.9 | 1.2 | 9.4 | 1.0 | 6.9 | ns |
| **$V_{CC(A)}$ = 3.3 V ± 0.3 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.5 | 23 | 1.5 | 21.2 | 1.1 | 8.8 | 0.8 | 6.3 | 0.5 | 4.4 | ns |
| | | Bn to An | 0.8 | 15 | 0.8 | 7.2 | 0.8 | 6.2 | 0.7 | 6.1 | 0.6 | 6.0 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 1.6 | 8.2 | 1.6 | 8.2 | 1.6 | 8.2 | 1.6 | 8.2 | 1.6 | 8.2 | ns |
| | | $\overline{OE}$ to Bn | 2.1 | 30 | 2.1 | 29.0 | 1.7 | 10.3 | 1.5 | 8.6 | 0.8 | 6.3 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 0.8 | 8.1 | 0.8 | 8.1 | 0.8 | 8.1 | 0.8 | 8.1 | 0.8 | 8.1 | ns |
| | | $\overline{OE}$ to Bn | 1.8 | 31 | 1.8 | 27.7 | 1.4 | 12.4 | 1.1 | 8.5 | 0.9 | 6.4 | ns |
| **$V_{CC(A)}$ = 5.0 V ± 0.5 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.5 | 22 | 1.5 | 21.4 | 1.0 | 8.8 | 0.7 | 6.0 | 0.4 | 4.2 | ns |
| | | Bn to An | 0.7 | 13 | 0.7 | 7.0 | 0.4 | 4.8 | 0.3 | 4.5 | 0.3 | 4.3 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 0.3 | 5.4 | 0.3 | 5.4 | 0.3 | 5.4 | 0.3 | 5.4 | 0.3 | 5.4 | ns |
| | | $\overline{OE}$ to Bn | 2.0 | 30 | 2.0 | 28.7 | 1.6 | 9.7 | 1.4 | 8.0 | 0.7 | 5.7 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 0.7 | 6.4 | 0.7 | 6.4 | 0.7 | 6.4 | 0.7 | 6.4 | 0.7 | 6.4 | ns |
| | | $\overline{OE}$ to Bn | 1.5 | 31 | 1.5 | 27.6 | 1.3 | 11.4 | 1.0 | 8.1 | 0.9 | 6.0 | ns |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.

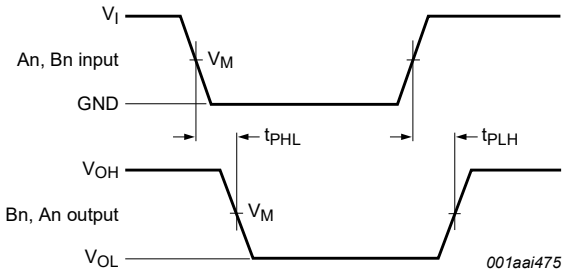
**Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8; for waveforms see Fig. 6 and Fig. 7. [1]*

| Symbol | Parameter | Conditions | $V_{CC(B)}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.5 V ± 0.1 V | | 1.8 V ± 0.15 V | | 2.5 V ± 0.2 V | | 3.3 V ± 0.3 V | | 5.0 V ± 0.5 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| **$V_{CC(A)}$ = 1.5 V ± 0.1 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.7 | 32 | 1.7 | 27 | 1.3 | 21 | 1.0 | 18 | 0.8 | 16 | ns |
| | | Bn to An | 0.9 | 32 | 0.9 | 30 | 0.8 | 28 | 0.7 | 28 | 0.7 | 26 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 1.5 | 34 | 1.5 | 34 | 1.5 | 34 | 1.5 | 34 | 1.4 | 34 | ns |
| | | $\overline{OE}$ to Bn | 2.4 | 41 | 2.4 | 40 | 1.9 | 18 | 1.7 | 17 | 1.3 | 15 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 0.4 | 40 | 0.4 | 40 | 0.4 | 40 | 0.4 | 40 | 0.4 | 40 | ns |
| | | $\overline{OE}$ to Bn | 1.8 | 43 | 1.8 | 41 | 1.5 | 22 | 1.2 | 18 | 0.9 | 16 | ns |
| **$V_{CC(A)}$ = 1.8 V ± 0.15 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.7 | 30 | 1.7 | 25.9 | 1.3 | 13.2 | 1.0 | 11.4 | 0.8 | 11.1 | ns |
| | | Bn to An | 0.9 | 27 | 0.9 | 28.8 | 0.8 | 27.6 | 0.7 | 27.4 | 0.7 | 27.4 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 1.5 | 34 | 1.5 | 33.6 | 1.5 | 33.4 | 1.5 | 33.3 | 1.4 | 33.2 | ns |
| | | $\overline{OE}$ to Bn | 2.4 | 40 | 2.4 | 36.2 | 1.9 | 17.1 | 1.7 | 16.0 | 1.3 | 14.3 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 0.4 | 28 | 0.4 | 28 | 0.4 | 27.8 | 0.4 | 27.7 | 0.4 | 27.7 | ns |
| | | $\overline{OE}$ to Bn | 1.8 | 41 | 1.8 | 40 | 1.5 | 20 | 1.2 | 16.6 | 0.9 | 14.8 | ns |
| **$V_{CC(A)}$ = 2.5 V ± 0.2 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.5 | 28 | 1.5 | 25.4 | 1.2 | 13 | 0.8 | 10.2 | 0.6 | 8.8 | ns |
| | | Bn to An | 1.2 | 23 | 1.2 | 13.3 | 1.0 | 13.1 | 1.0 | 12.9 | 0.9 | 12.8 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 1.4 | 13 | 1.4 | 13 | 1.4 | 13 | 1.4 | 13 | 1.4 | 13 | ns |
| | | $\overline{OE}$ to Bn | 2.3 | 37 | 2.3 | 33.6 | 1.8 | 15 | 1.7 | 14.3 | 0.9 | 10.9 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 1.0 | 17.2 | 1.0 | 17.2 | 1.0 | 17.3 | 1.0 | 17.2 | 1.0 | 17.3 | ns |
| | | $\overline{OE}$ to Bn | 1.7 | 38 | 1.7 | 32.2 | 1.5 | 18.1 | 1.2 | 14.1 | 1.0 | 11.2 | ns |
| **$V_{CC(A)}$ = 3.3 V ± 0.3 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.5 | 28 | 1.5 | 25.2 | 1.1 | 12.8 | 0.8 | 10.3 | 0.5 | 10.4 | ns |
| | | Bn to An | 0.8 | 18 | 0.8 | 11.2 | 0.8 | 10.2 | 0.7 | 10.1 | 0.6 | 10 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 1.6 | 12.2 | 1.6 | 12.2 | 1.6 | 12.2 | 1.6 | 12.2 | 1.6 | 12.2 | ns |
| | | $\overline{OE}$ to Bn | 2.1 | 36 | 2.1 | 33 | 1.7 | 14.3 | 1.5 | 12.6 | 0.8 | 10.3 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 0.8 | 14.1 | 0.8 | 14.1 | 0.8 | 13.6 | 0.8 | 13.2 | 0.8 | 13.6 | ns |
| | | $\overline{OE}$ to Bn | 1.8 | 37 | 1.8 | 31.7 | 1.4 | 18.4 | 1.1 | 12.9 | 0.9 | 10.9 | ns |
| **$V_{CC(A)}$ = 5.0 V ± 0.5 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to Bn | 1.5 | 26 | 1.5 | 25.4 | 1.0 | 12.8 | 0.7 | 10 | 0.4 | 8.2 | ns |
| | | Bn to An | 0.7 | 16 | 0.7 | 11 | 0.4 | 8.8 | 0.3 | 8.5 | 0.3 | 8.3 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An | 0.3 | 9.4 | 0.3 | 9.4 | 0.3 | 9.4 | 0.3 | 9.4 | 0.3 | 9.4 | ns |
| | | $\overline{OE}$ to Bn | 2.0 | 36 | 2.0 | 32.7 | 1.6 | 13.7 | 1.4 | 12 | 0.7 | 9.7 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An | 0.7 | 10.9 | 0.7 | 10.9 | 0.7 | 10.9 | 0.7 | 10.9 | 0.7 | 10.9 | ns |
| | | $\overline{OE}$ to Bn | 1.5 | 37 | 1.5 | 31.6 | 1.3 | 18.4 | 1.0 | 13.7 | 0.9 | 10.7 | ns |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.

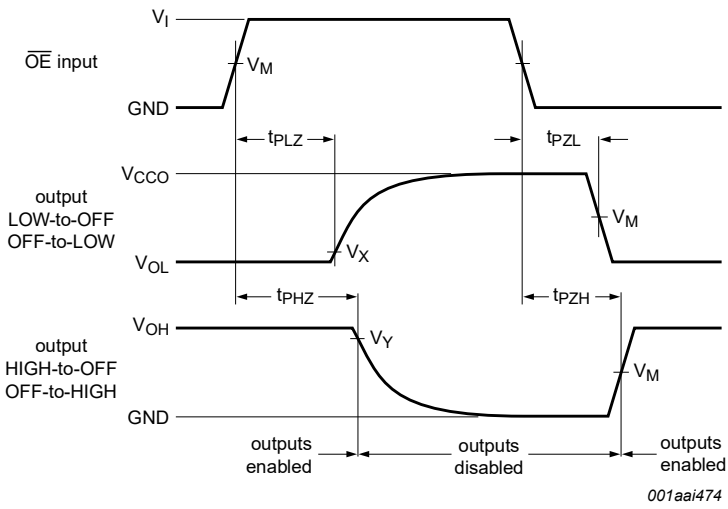
## 10.1. Waveforms and test circuit




Measurement points are given in Table 13.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 6. The data input (An, Bn) to output (Bn, An) propagation delay times**




Measurement points are given in Table 13.

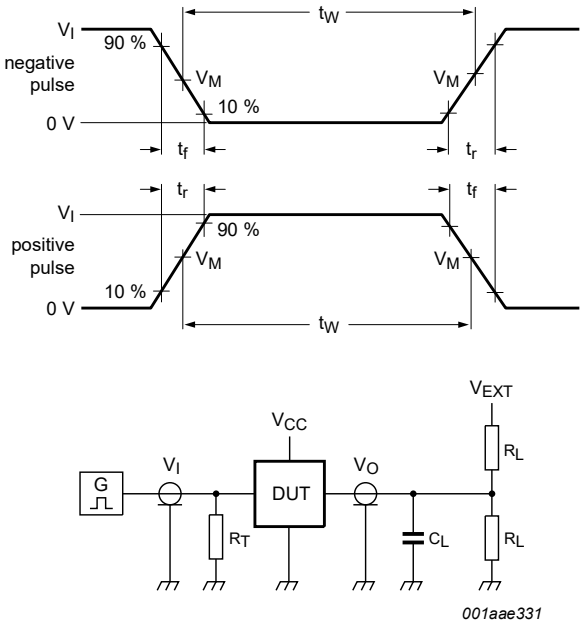
$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 7. Enable and disable times**

**Table 13. Measurement points**

| Supply voltage | Input [1] | Output [2] | | |
|---|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.2 V to 1.6 V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$ + 0.1 V | $V_{OH}$ - 0.1 V |
| 1.65 V to 2.7 V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 3.0 V to 5.5 V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |

[1] $V_{CCI}$ is the supply voltage associated with the data input port.
[2] $V_{CCO}$ is the supply voltage associated with the output port.




Test data is given in Table 14.

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance.

$V_{EXT}$ = External voltage for measuring switching times.

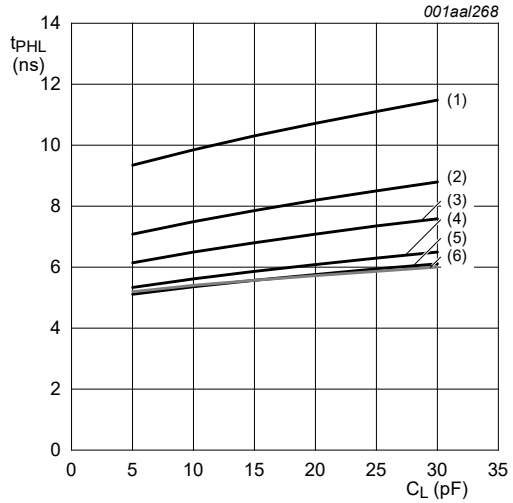
**Fig. 8. Test circuit for measuring switching times**

**Table 14. Test data**

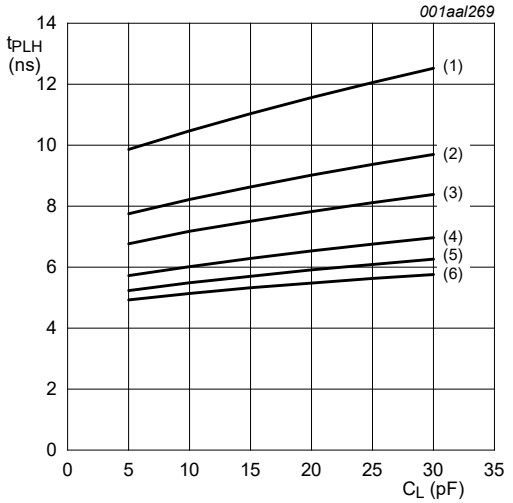
| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | $V_I$ [1] | Δt/ΔV [2] | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ [3] |
| 1.2 V to 5.5 V | $V_{CCI}$ | ≤ 1.0 ns/V | 15 pF | 2 kΩ | open | GND | $2V_{CCO}$ |

[1] $V_{CCI}$ is the supply voltage associated with the data input port.
[2] dV/dt ≥ 1.0 V/ns.
[3] $V_{CCO}$ is the supply voltage associated with the output port.

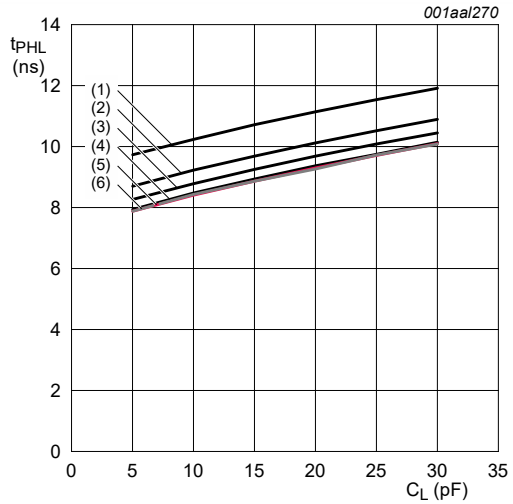
## 11. Typical propagation delay characteristics



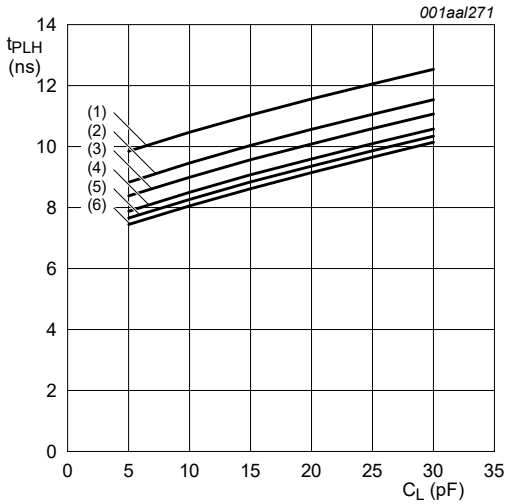

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)



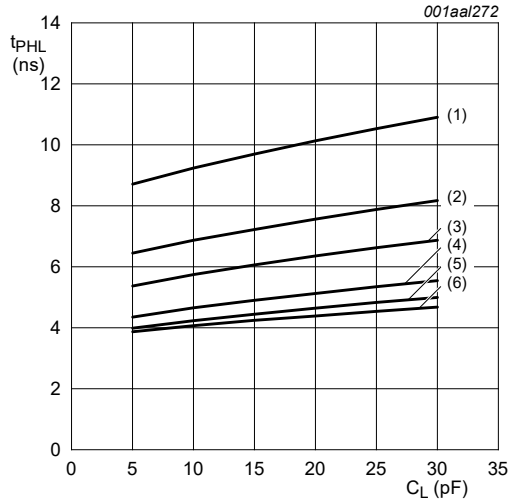

c. HIGH to LOW propagation delay (B to A)



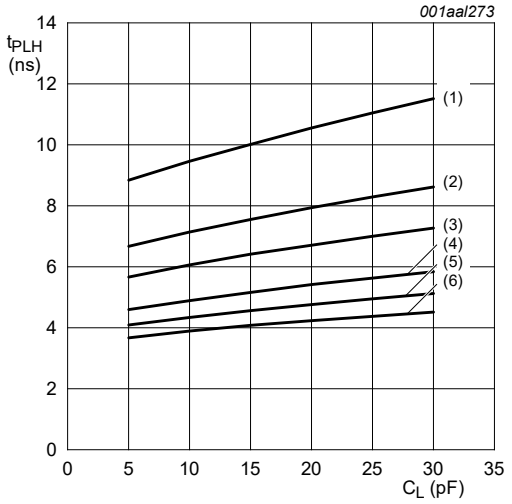

d. LOW to HIGH propagation delay (B to A)

(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

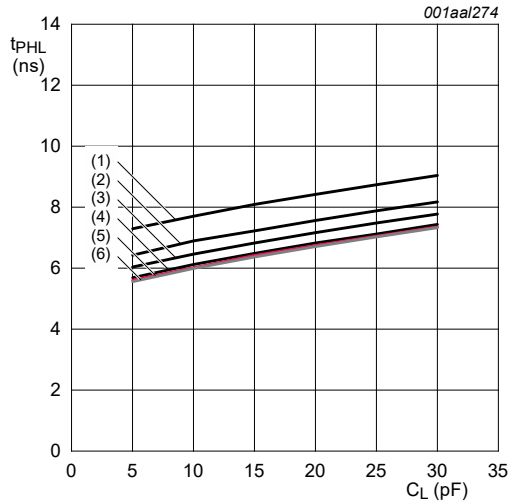
**Fig. 9. Typical propagation delay versus load capacitance; $T_{amb}$ = 25 °C; $V_{CC(A)}$ = 1.2 V**



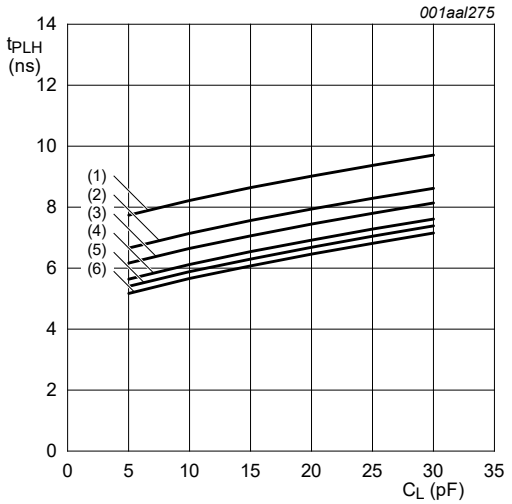

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)



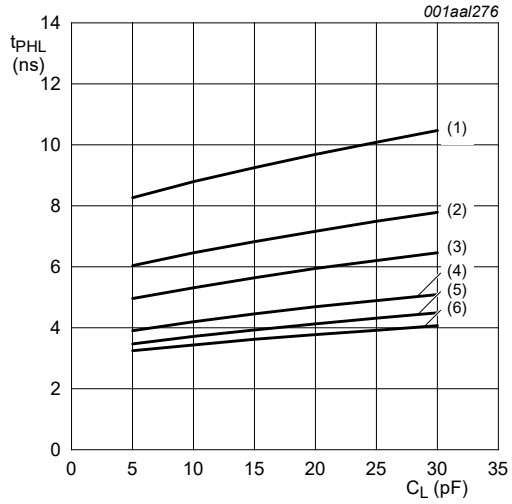

c. HIGH to LOW propagation delay (B to A)



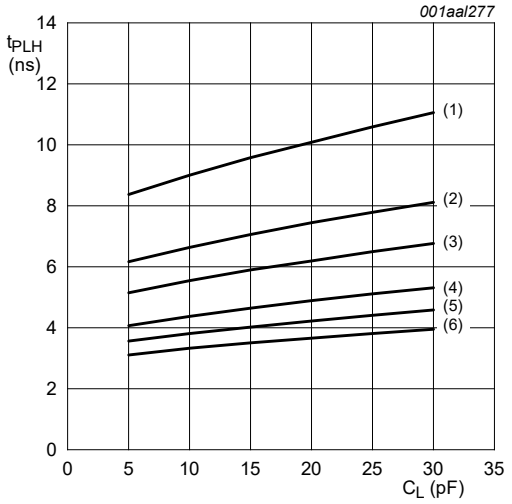

d. LOW to HIGH propagation delay (B to A)

(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

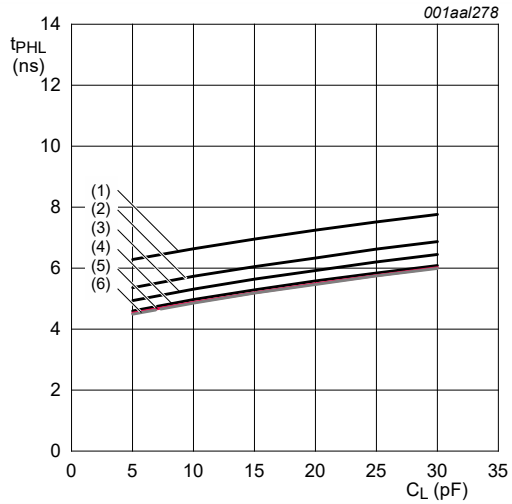
**Fig. 10. Typical propagation delay versus load capacitance; $T_{amb}$ = 25 °C; $V_{CC(A)}$ = 1.5 V**



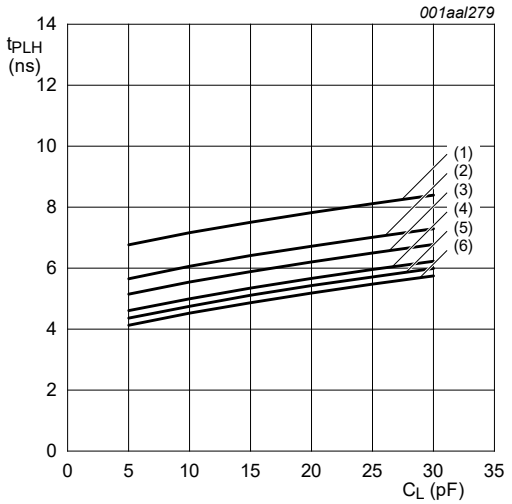

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)



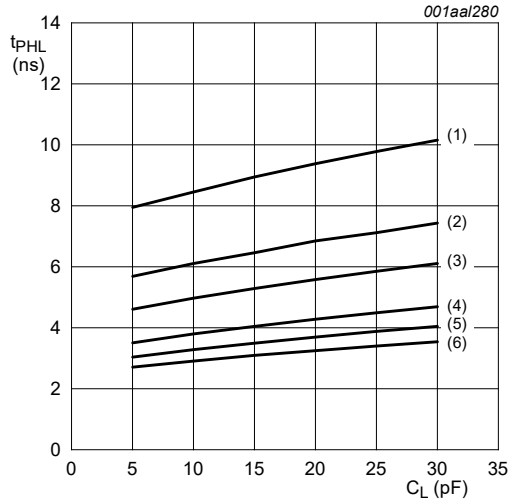

c. HIGH to LOW propagation delay (B to A)



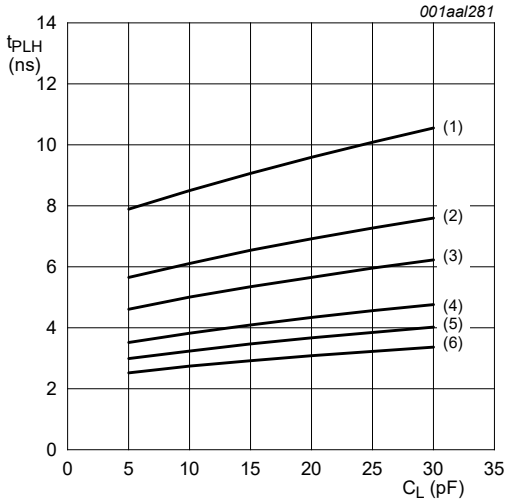

d. LOW to HIGH propagation delay (B to A)

(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

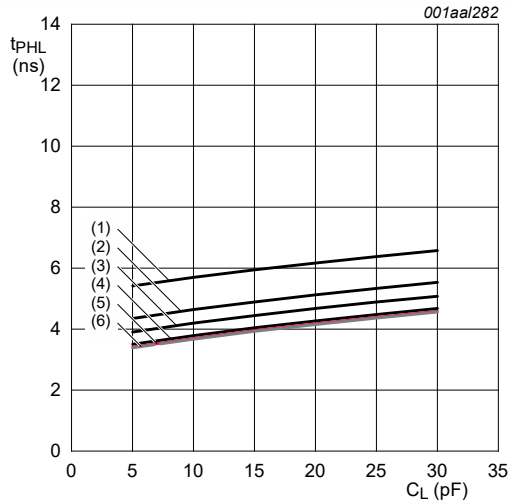
**Fig. 11. Typical propagation delay versus load capacitance; $T_{amb}$ = 25 °C; $V_{CC(A)}$ = 1.8 V**



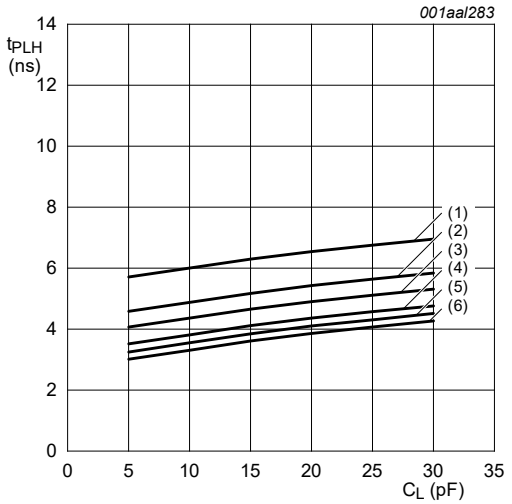

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)



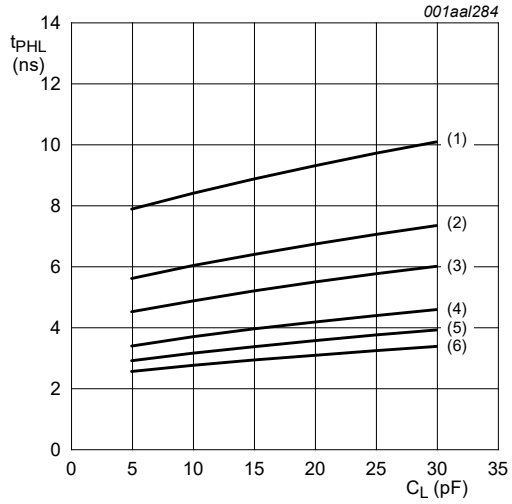

c. HIGH to LOW propagation delay (B to A)



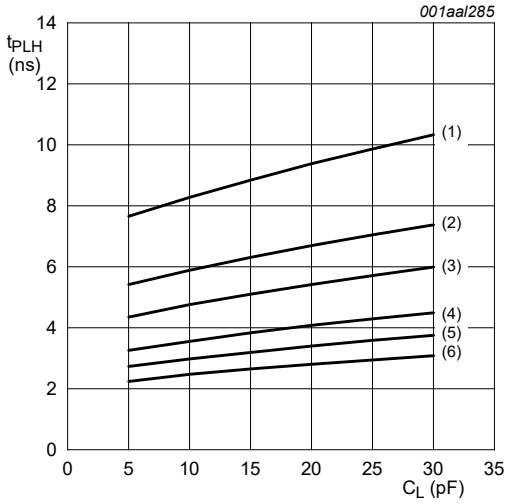

d. LOW to HIGH propagation delay (B to A)

(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

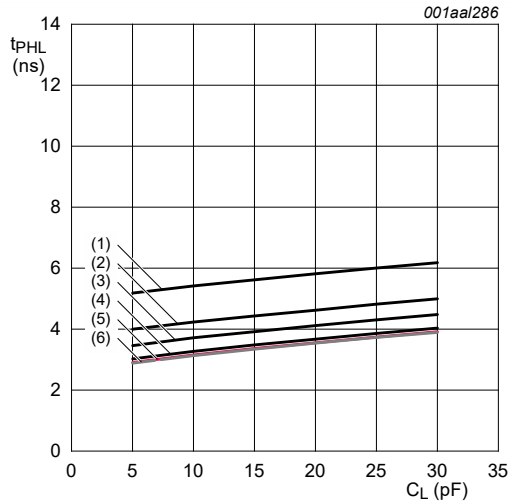
**Fig. 12. Typical propagation delay versus load capacitance; $T_{amb}$ = 25 °C; $V_{CC(A)}$ = 2.5 V**



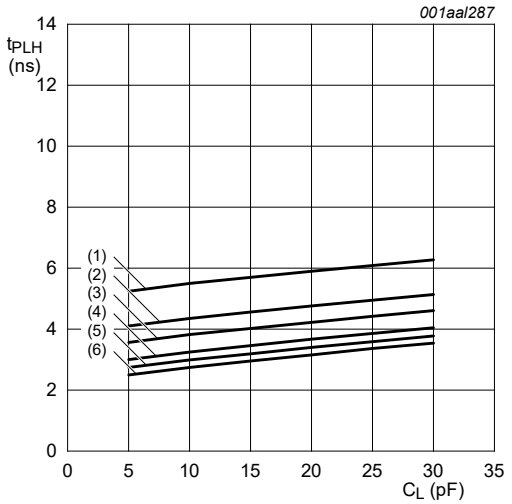

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)



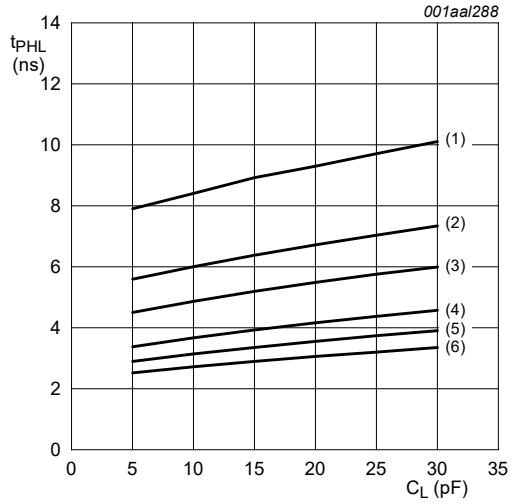

c. HIGH to LOW propagation delay (B to A)



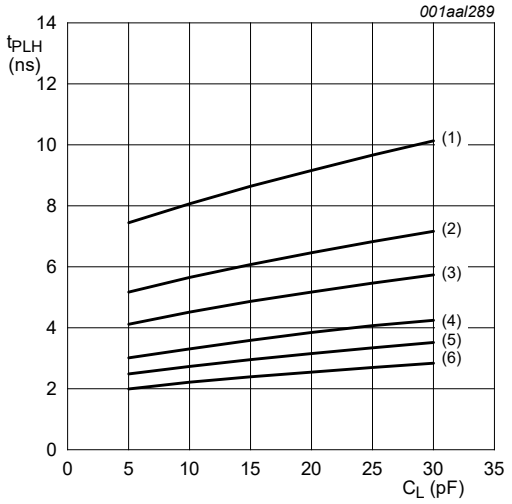

d. LOW to HIGH propagation delay (B to A)

(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

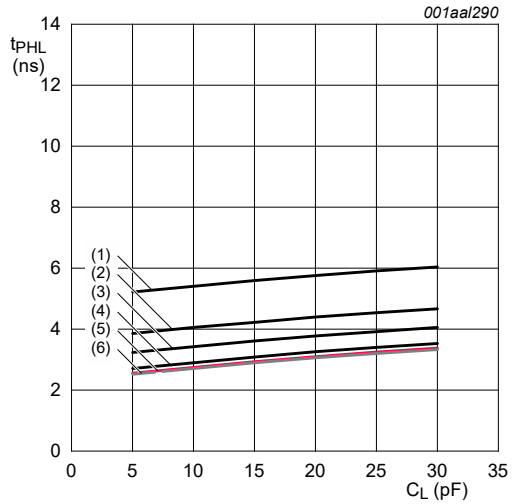
**Fig. 13. Typical propagation delay versus load capacitance; $T_{amb}$ = 25 °C; $V_{CC(A)}$ = 3.3 V**



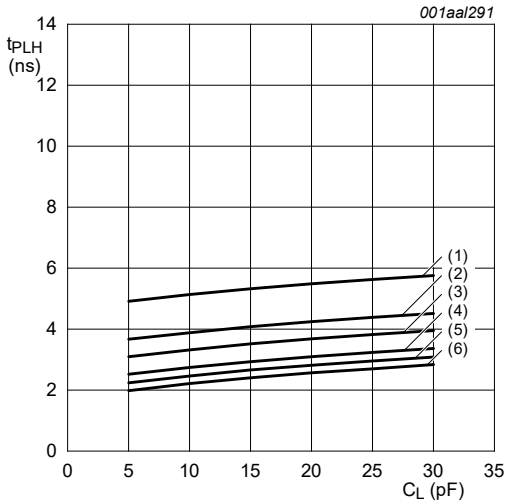

a. HIGH to LOW propagation delay (A to B)




b. LOW to HIGH propagation delay (A to B)




c. HIGH to LOW propagation delay (B to A)




d. LOW to HIGH propagation delay (B to A)

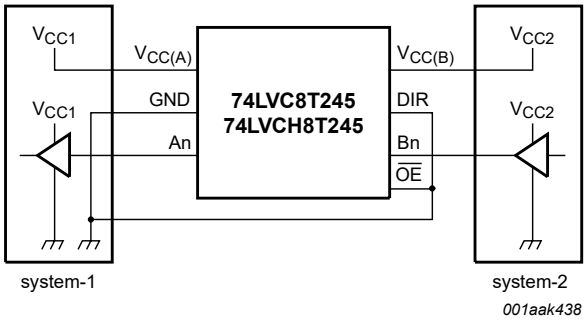
(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.
(6) $V_{CC(B)}$ = 5.0 V.

**Fig. 14. Typical propagation delay versus load capacitance; $T_{amb}$ = 25 °C; $V_{CC(A)}$ = 5 V**

# 12. Application information

## 12.1. Unidirectional logic level-shifting application

The circuit given in Fig. 15 is an example of the 74LVC8T245; 74LVCH8T245 being used in an unidirectional logic level-shifting application.




Schematic given for one channel.

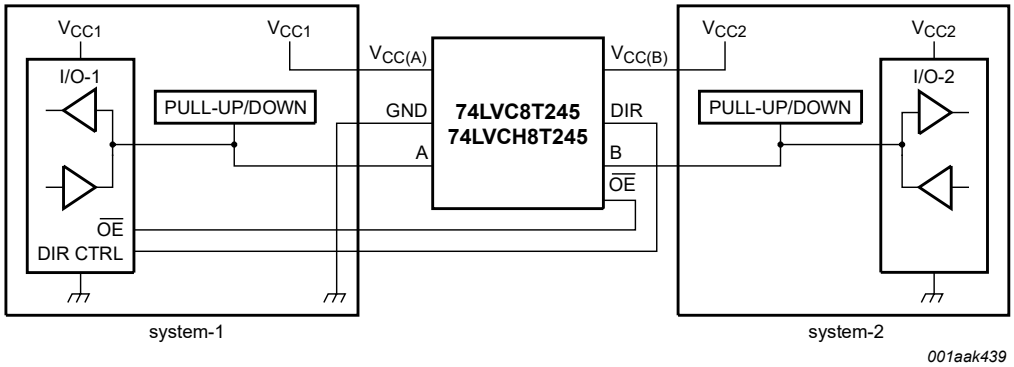
**Fig. 15. Unidirectional logic level-shifting application**

**Table 15. Description unidirectional logic level-shifting application**

| Name | Function | Description |
|---|---|---|
| $V_{CC(A)}$ | $V_{CC1}$ | supply voltage of system-1 (1.2 V to 5.5 V) |
| GND | GND | device GND |
| A | OUT | output level depends on $V_{CC1}$ voltage |
| B | IN | input threshold value depends on $V_{CC2}$ voltage |
| DIR | DIR | the GND (LOW level) determines B port to A port direction |
| $V_{CC(B)}$ | $V_{CC2}$ | supply voltage of system-2 (1.2 V to 5.5 V) |
| $\overline{OE}$ | $\overline{OE}$ | The GND (LOW level) enables the output ports |

## 12.2. Bidirectional logic level-shifting application

Fig. 16 shows the 74LVC8T245; 74LVCH8T245 being used in a bidirectional logic level-shifting application.




Schematic given for one channel.

Pull-up or pull-down only needed for 74LVC8T245.

**Fig. 16. Bidirectional logic level-shifting application**

Table 16 gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

**Table 16. Description bidirectional logic level-shifting application**

*H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.*

| State | DIR CTRL | $\overline{OE}$ | I/O-1 | I/O-2 | Description |
|---|---|---|---|---|---|
| 1 | H | L | output | input | system-1 data to system-2 |
| 2 | H | H | Z | Z | system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold. |
| 3 | L | H | Z | Z | DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold. |
| 4 | L | L | input | output | system-2 data to system-1 |

## 12.3. Power-up considerations

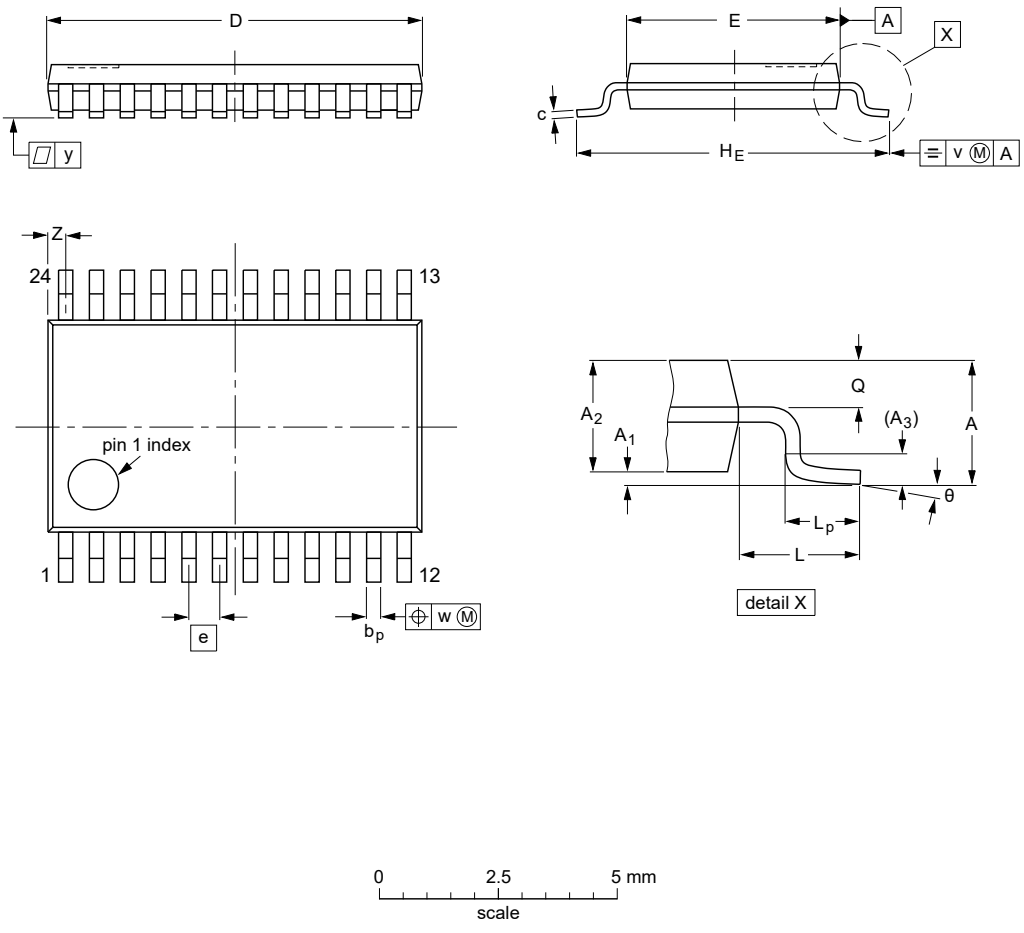
The device is designed such that no special power-up sequence is required other than GND being applied first.

**Table 17. Typical total supply current ($I_{CC(A)}$ + $I_{CC(B)}$)**

| $V_{CC(A)}$ | $V_{CC(B)}$ | | | | | Unit |
|---|---|---|---|---|---|---|
| | 0 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V | |
| 0 V | 0 | < 1 | < 1 | < 1 | < 1 | µA |
| 1.8 V | < 1 | < 2 | < 2 | < 2 | 2 | µA |
| 2.5 V | < 1 | < 2 | < 2 | < 2 | < 2 | µA |
| 3.3 V | < 1 | < 2 | < 2 | < 2 | < 2 | µA |
| 5.0 V | < 1 | 2 | < 2 | < 2 | < 2 | µA |

## 13. Package outline

**TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm** **SOT355-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 7.9<br>7.7 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

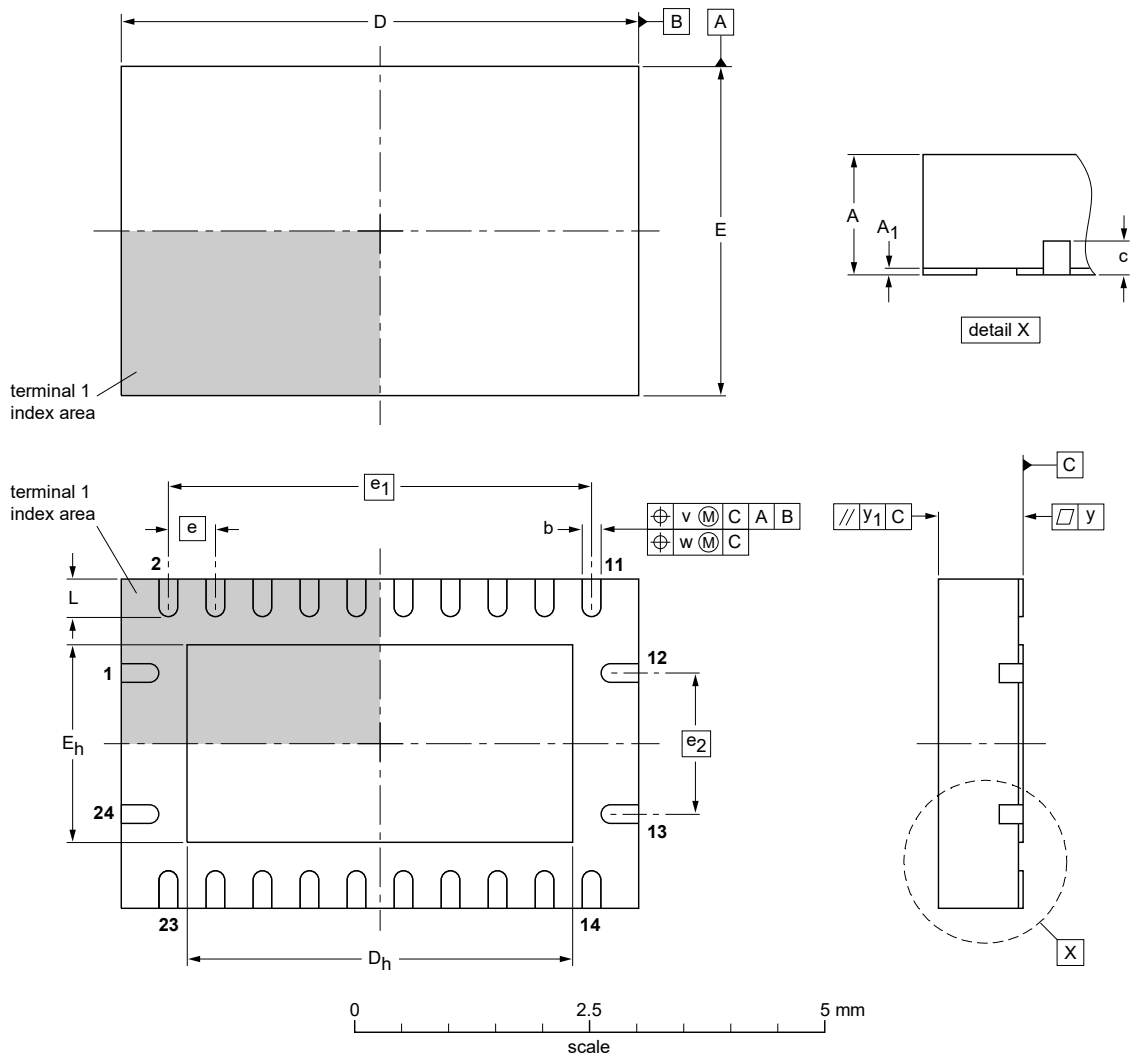
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT355-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 17. Package outline SOT355-1 (TSSOP24)**

**DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm** **SOT815-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 5.6<br>5.4 | 4.25<br>3.95 | 3.6<br>3.4 | 2.25<br>1.95 | 0.5 | 4.5 | 1.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

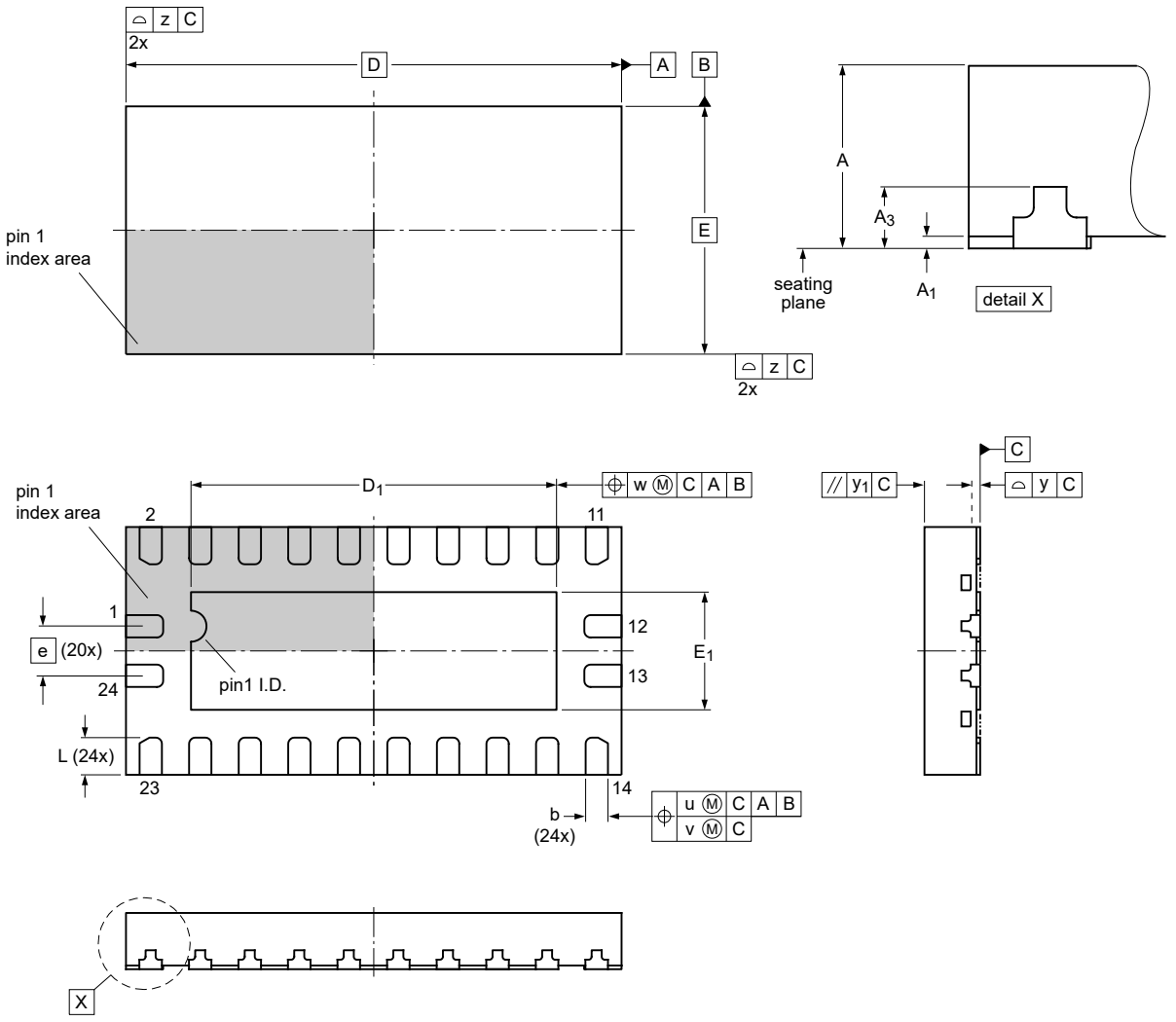
**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT815-1 | - - - | - - - | - - - | | | 03-04-29 |

**Fig. 18. Package outline SOT815-1 (DHVQFN24)**

**DHXQFN24: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 24 terminals; 0.4 mm pitch; body 2 mm x 4 mm x 0.48 mm** **SOT8024-1**




Dimensions (mm are the original dimensions)

| Unit | A | $A_1$ | $A_3$ | b | D | $D_1$ | E | $E_1$ | e | k | L | u | v | w | y | $y_1$ | z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| max | 0.48 | 0.05 | 0.15 (typ) | 0.23 | 4.0 | 3.00 | 2.0 | 1.00 | 0.4 | | 0.35 | 0.1 | 0.05 | 0.1 | 0.05 | 0.05 | 0.05 |
| mm nom | 0.45 | 0.02 | | 0.18 | | 2.95 | | 0.95 | | | 0.30 | | | | | | |
| min | 0.42 | 0.00 | | 0.13 | | 2.90 | | 0.90 | | 0.2 | 0.25 | | | | | | |

*sot8024-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT8024-1 | | | | | | ~~20-09-18~~ 20-09-22 |

**Fig. 19. Package outline SOT8024-1 (DHXQFN24)**

## 14. Abbreviations

**Table 18. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

## 15. Revision history

**Table 19. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC_LVCH8T245 v.5 | 20210429 | Product data sheet | - | 74LVC_LVCH8T245 v.4 |
| Modifications: | • Type number 74LVC8T245BZ (SOT8024-1 / DHXQFN24) added. | | | |
| 74LVC_LVCH8T245 v.4 | 20200922 | Product data sheet | - | 74LVC_LVCH8T245 v.3 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Table 4: Derating values for $P_{tot}$ total power dissipation updated. | | | |
| 74LVC_LVCH8T245 v.3 | 20111212 | Product data sheet | - | 74LVC_LVCH8T245 v.2 |
| Modifications: | • Legal pages updated. | | | |
| 74LVC_LVCH8T245 v.2 | 20110211 | Product data sheet | - | 74LVC_LVCH8T245 v.1 |
| 74LVC_LVCH8T245 v.1 | 20100111 | Product data sheet | - | - |

# 16. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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