

74LVC244A-Q100; 74LVCH244A-Q100

Octal buffer/line driver; 3-state

Rev. 3 — 13 August 2018

Product data sheet

1. General description

The 74LVC244A-Q100; 74LVCH244A-Q100 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5.0 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 V and 5 V environment.

The 74LVCH244A-Q100 bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when $V_{CC} = 0$ V
- Bus hold on all data inputs (74LVCH244A-Q100 only)
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC244AD-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC244APW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVCH244APW-Q100				
74LVC244ABQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

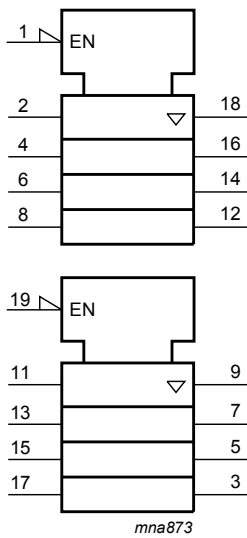


Fig. 1. IEC logic diagram

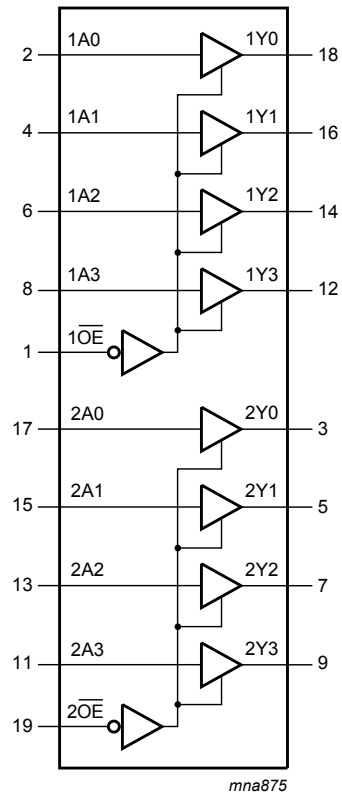


Fig. 2. Functional diagram

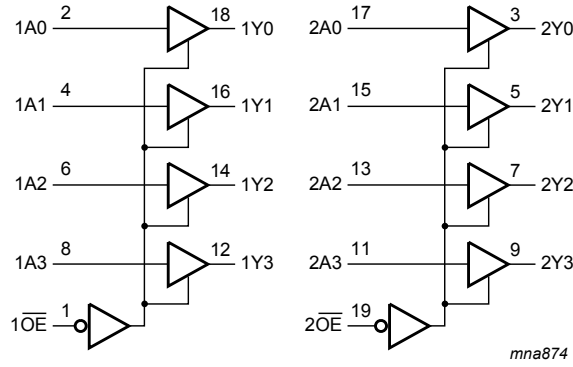


Fig. 3. Logic symbol

5. Pinning information

5.1. Pinning

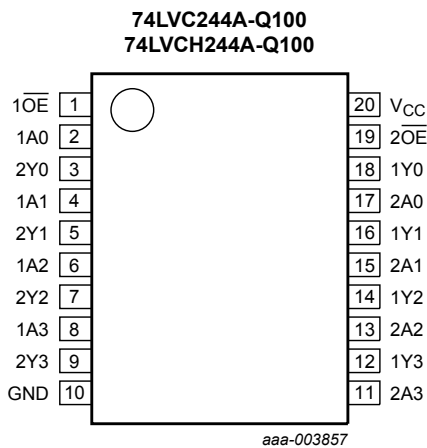
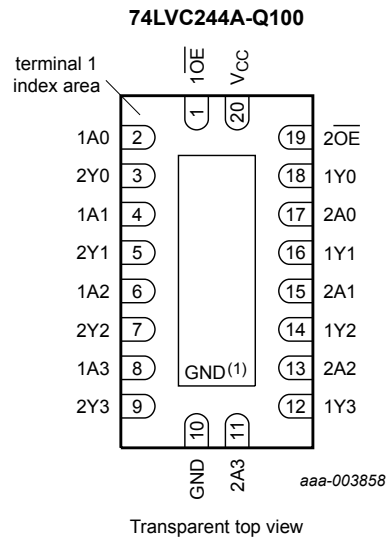


Fig. 4. Pin configuration SOT163-1 (SO20) and SOT360-1 (TSSOP20)



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig. 5. Pin configuration SOT764-1 (DHVQFN20)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3,	18, 16, 14, 12	data output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	output HIGH or LOW	[2] -0.5	V _{CC} + 0.5	V
		output 3-state	[2] -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3] -	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
 [2] The output voltage ratings may be exceeded if the output current ratings are observed.
 [3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
 For TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 3.6 \text{ V}$ [2]	-	± 0.1	± 5	-	± 20	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = 5.5 \text{ V}$ or GND; $V_{CC} = 3.6 \text{ V}$ [2]	-	± 0.1	± 5	-	± 20	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5 \text{ V}$; $V_{CC} = 0.0 \text{ V}$	-	± 0.1	± 10	-	± 20	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 3.6 \text{ V}$	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_{CC} = 2.7 \text{ V}$ to 3.6 V	-	5	500	-	5000	μA
C_I	input capacitance		-	4.0	-	-	-	pF
I_{BHL}	bus hold LOW current	$V_{CC} = 1.65 \text{ V}$; $V_I = 0.58 \text{ V}$ [3][4]	10	-	-	10	-	μA
		$V_{CC} = 2.3 \text{ V}$; $V_I = 0.7 \text{ V}$	30	-	-	25	-	μA
		$V_{CC} = 3.0 \text{ V}$; $V_I = 0.8 \text{ V}$	75	-	-	60	-	μA
I_{BHH}	bus hold HIGH current	$V_{CC} = 1.65 \text{ V}$; $V_I = 1.07 \text{ V}$ [3][4]	-10	-	-	-10	-	μA
		$V_{CC} = 2.3 \text{ V}$; $V_I = 1.7 \text{ V}$	-30	-	-	-25	-	μA
		$V_{CC} = 3.0 \text{ V}$; $V_I = 2.0 \text{ V}$	-75	-	-	-60	-	μA
I_{BHLO}	bus hold LOW overdrive current	$V_{CC} = 1.95 \text{ V}$ [3][5]	200	-	-	200	-	μA
		$V_{CC} = 2.7 \text{ V}$	300	-	-	300	-	μA
		$V_{CC} = 3.6 \text{ V}$	500	-	-	500	-	μA
I_{BHHO}	bus hold HIGH overdrive current	$V_{CC} = 1.95 \text{ V}$ [3][5]	-200	-	-	-200	-	μA
		$V_{CC} = 2.7 \text{ V}$	-300	-	-	-300	-	μA
		$V_{CC} = 3.6 \text{ V}$	-500	-	-	-500	-	μA

[1] All typical values are measured at $V_{CC} = 3.3 \text{ V}$ (unless stated otherwise) and $T_{amb} = 25 \text{ }^\circ\text{C}$.

[2] The bus hold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input terminal.

[3] Valid for data inputs of bus hold parts only (74LVCH244A-Q100). Note that control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data input holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nYn; see Fig. 6 [2]						
		V _{CC} = 1.2 V	-	17.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.4	13.7	1.5	15.8	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.4	7.1	1.0	8.2	ns
		V _{CC} = 2.7 V	1.5	3.4	6.9	1.5	9.0	ns
t _{en}	enable time	nOE to nYn; see Fig. 7 [2]						
		V _{CC} = 1.2 V	-	24.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	7.0	17.3	1.5	20.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	3.9	9.5	1.5	11.0	ns
		V _{CC} = 2.7 V	1.5	4.1	8.6	1.5	11.0	ns
t _{dis}	disable time	nOE to nYn; see Fig. 7 [2]						
		V _{CC} = 1.2 V	-	9.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.2	4.5	9.8	2.2	11.3	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	3.6	5.5	0.5	6.4	ns
		V _{CC} = 2.7 V	1.5	3.3	6.8	1.5	8.5	ns
t _{sk(o)}	output skew time	[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC} [4]						
		V _{CC} = 1.65 V to 1.95 V	-	6.4	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	9.6	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	12.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

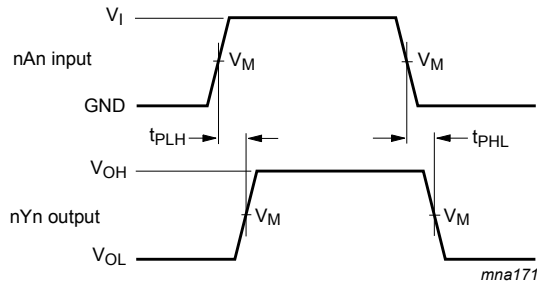
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

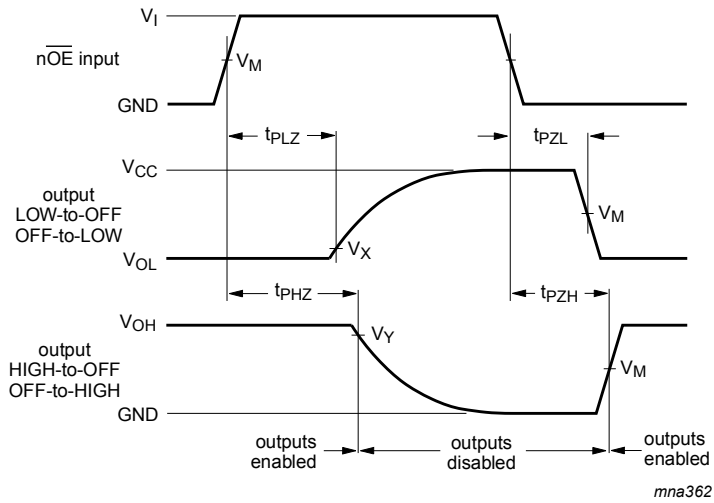
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The input (nAn) to output (nYn) propagation delays



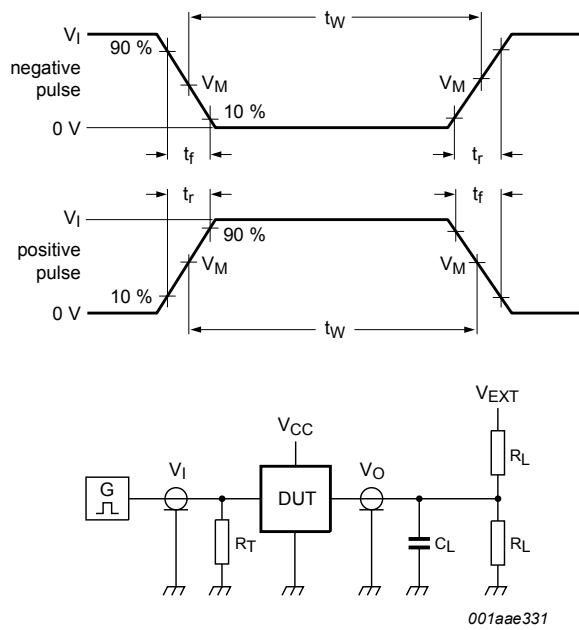
Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).
 Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

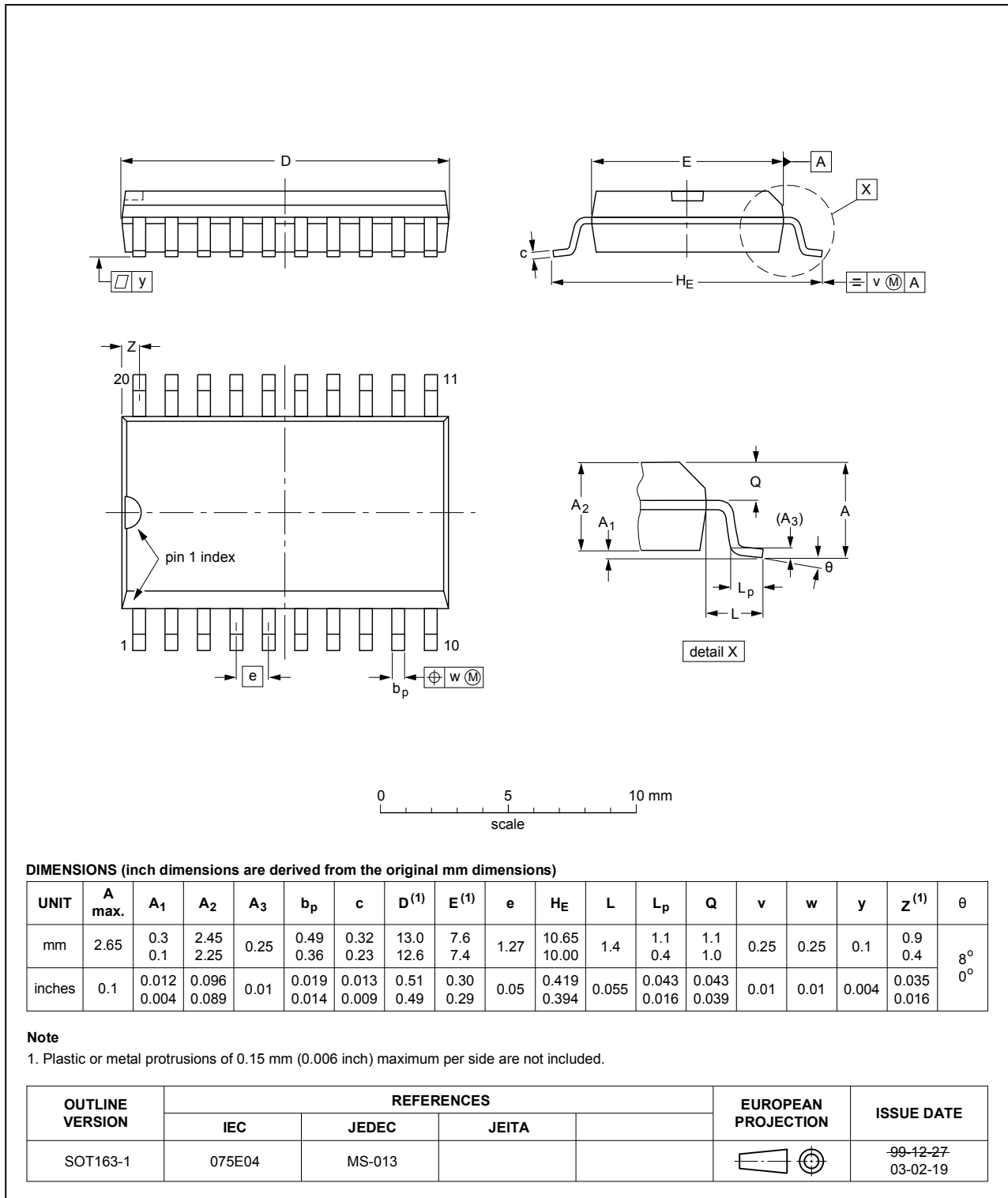


Fig. 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

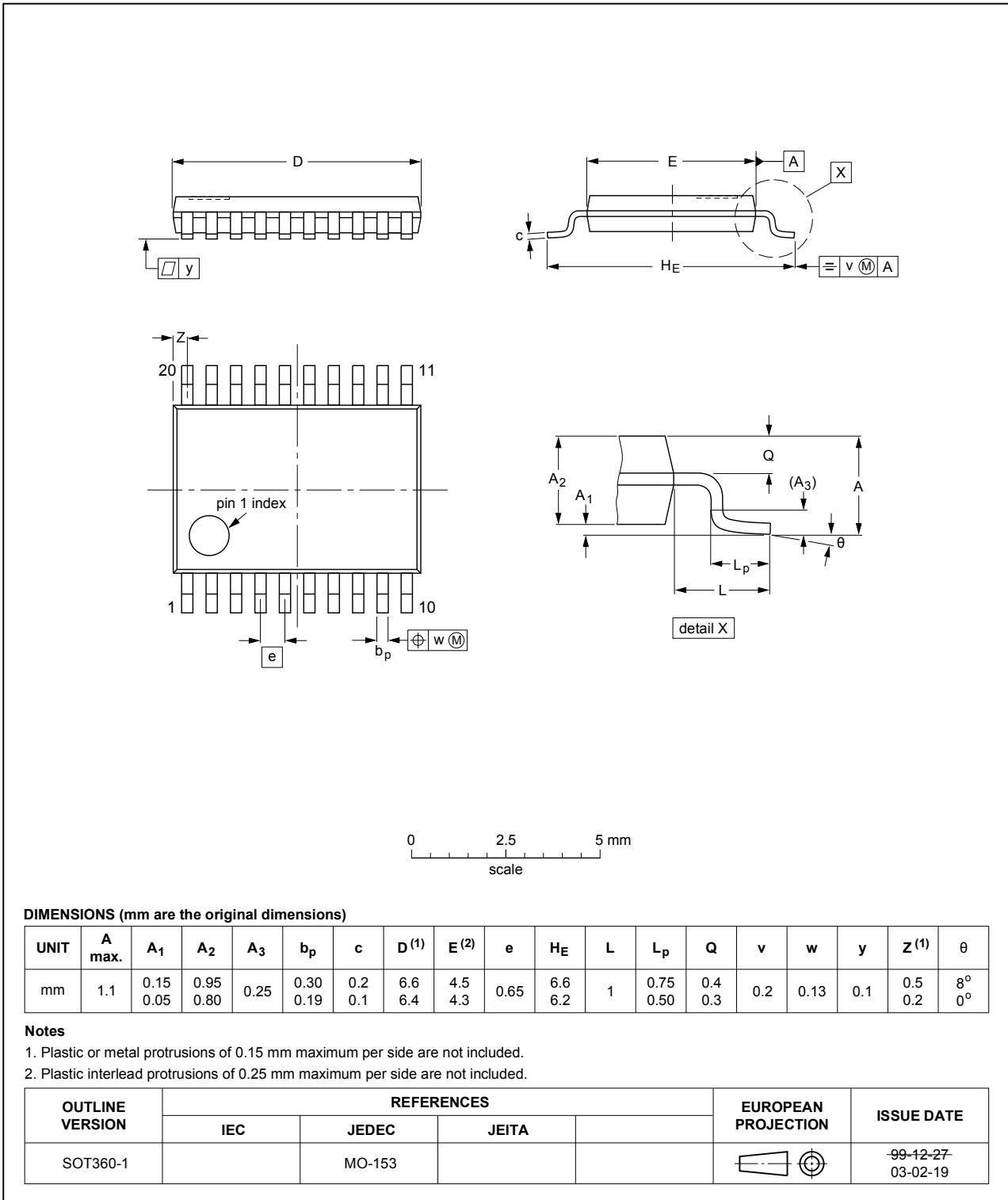


Fig. 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

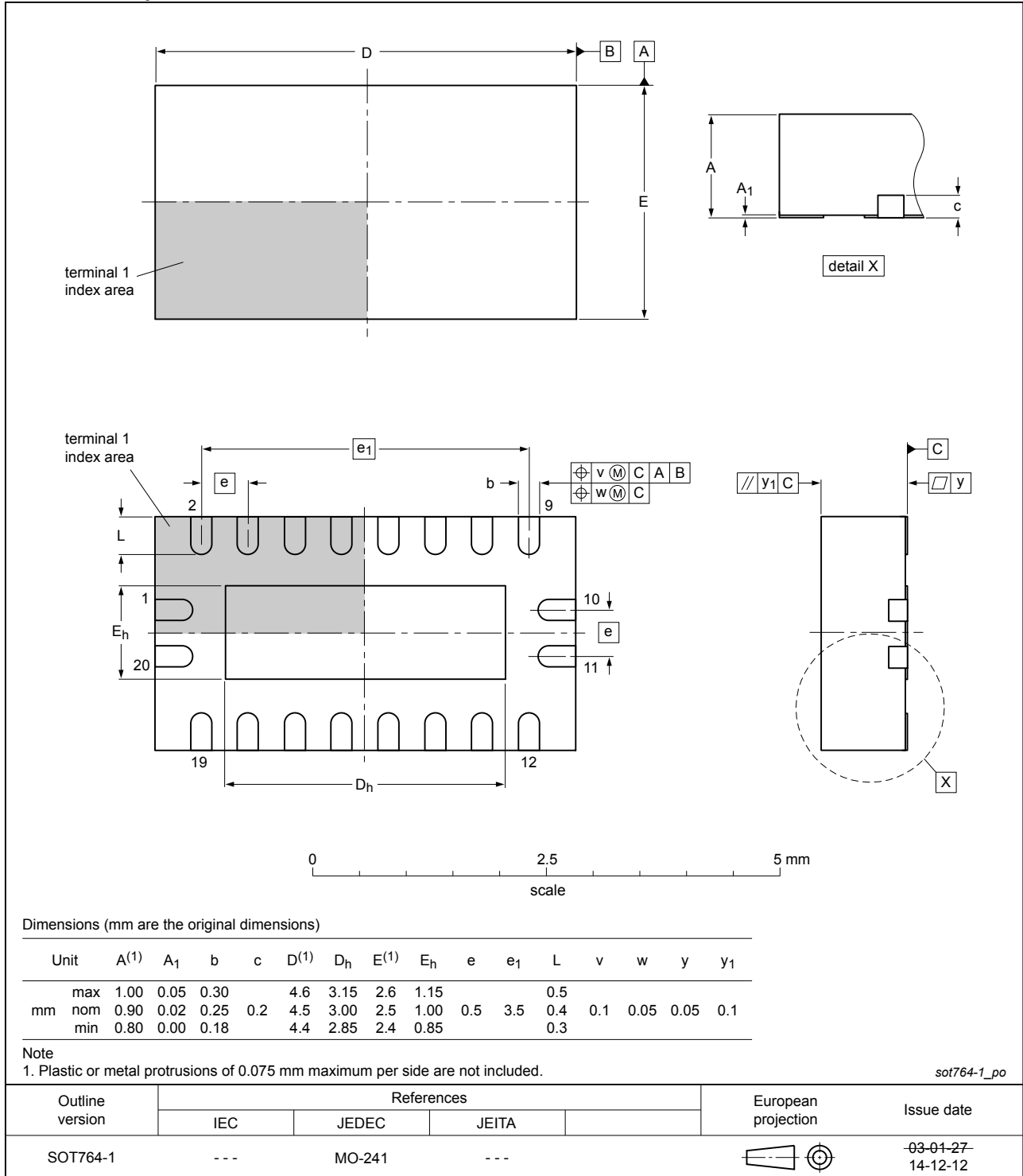


Fig. 11. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH244A_Q100 v.3	20180813	Product data sheet	-	74LVC_LVCH244A_Q100 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74LVCH244AD-Q100 (SOT163-1) removed. Type numbers 74LVC244ADB-Q100 and 74LVCH244ADB-Q100 (SOT339-1) removed. Type number 74LVCH244ABQ-Q100 (SOT764-1) removed. 			
74LVC_LVCH244A_Q100 v.2	20130813	Product data sheet	-	74LVC_LVCH244A_Q100 v.1
Modifications:	<ul style="list-style-type: none"> 74LVC244ADB-Q100 and 74LVCH244DB-Q100 added. 			
74LVC_LVCH244A_Q100 v.1	20120823	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[54FCT240CTDB](#) [028192B](#) [042140C](#) [051117G](#) [070519XB](#) [NL17SZ07P5T5G](#) [NLU1GT126AMUTCG](#) [74AUP1G17FW5-7](#)
[74LVC2G17FW4-7](#) [CD4502BE](#) [74LVCE1G126FZ4-7](#) [NL17SH17P5T5G](#) [74HCT126T14-13](#) [74LVC2G34FW4-7](#) [74VHC9126FT\(BJ\)](#)
[RHRXH162244K1](#) [74AUP1G34FW5-7](#) [74AUP1G07FW5-7](#) [74LVC1G126FW4-7](#) [74LVC2G126RA3-7](#) [NLX2G17CMUTCG](#)
[74LVCE1G125FZ4-7](#) [54FCT240TDB](#) [54FCT240TLB](#) [TC74HC4050AP\(F\)](#) [74LVCE1G07FZ4-7](#) [NLX3G16DMUTCG](#) [NLX2G06AMUTCG](#)
[NLVVHC1G50DFT2G](#) [LE87100NQC](#) [LE87100NQCT](#) [LE87285NQC](#) [LE87290YQC](#) [LE87290YQCT](#) [74AUP1G125FW5-7](#)
[NLU2G16CMUTCG](#) [MC74LCX244MN2TWG](#) [NLV74HC125ADR2G](#) [NLVHCT245ADTR2G](#) [NLV37WZ16USG](#) [NLVVHC1G126DFT2G](#)
[NLV27WZ126USG](#) [PCA9615DPZ](#)