74LVT244B; 74LVTH244B

3.3 V octal buffer/line driver; 3-state

Rev. 6 — 12 August 2021 Product data sheet

1. General description

The 74LVT244B; 74LVTH244B is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables ($1\overline{OE}$ and $2\overline{OE}$), each controlling four of the 3-state outputs. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

2. Features and benefits

- Octal bus interface
- 3-state buffers
- Speed upgrade of 74LVT244A
- Wide supply voltage range from 2.7 to 3.6 V
- BiCMOS high speed and output drive
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Live insertion and extraction permitted
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A 200 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT244BD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVTH244BD				
74LVT244BPW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVTH244BPW				

4. Functional diagram

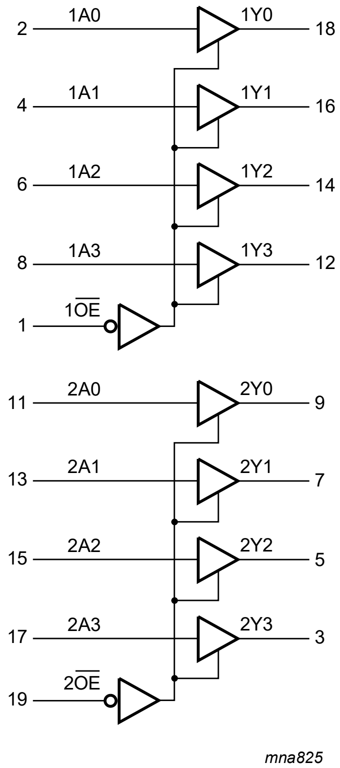


Fig. 1. Logic symbol

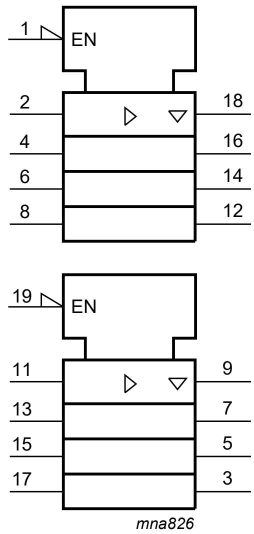


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning

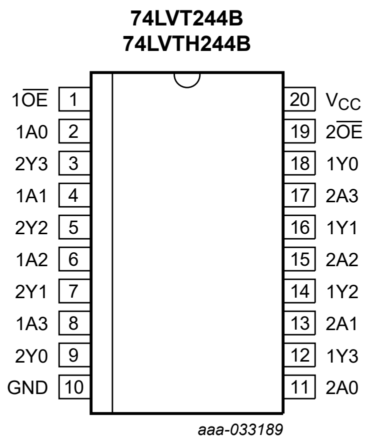


Fig. 3. Pin configuration SOT163-1 (SO20)

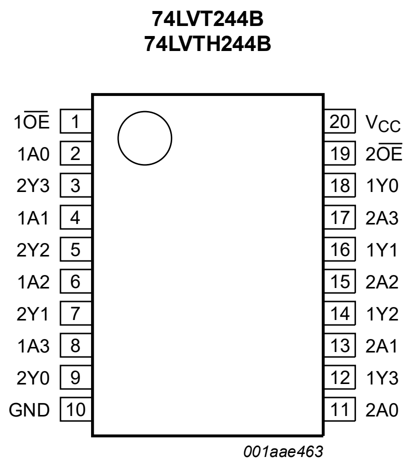


Fig. 4. Pin configuration SOT360-1 (TSSOP20)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
$n\overline{OE}$	**nAn**	**nYn**
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage		[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-64	-	mA
T_{stg}	storage temperature			-65	+150	°C
T_j	junction temperature		[2]	-	150	°C
P_{tot}	total power dissipation	T_{amb} = -40 to +85 °C		-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f_i ≥ 1 kHz	-	-	64	mA
T_{amb}	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = -18 mA	-1.2	-0.9	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V; I_{OH} = -100 μA	V_{CC} - 2.0	V_{CC} - 2.1	-	V
		V_{CC} = 2.7 V; I_{OH} = -8 mA	2.4	2.5	-	V
		V_{CC} = 3.0 V; I_{OH} = -32 mA	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 μA	-	0.1	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 16 mA	-	0.25	0.4	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 64 mA	-	0.4	0.55	V
I_I	input leakage current	all input pins				
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	0.1	10	μA
		control pins				
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-1	±0.1	1	μA
		data pins [2]				
		V_{CC} = 3.6 V; V_I = V_{CC}	-	0.1	1	μA
		V_{CC} = 3.6 V; V_I = 0 V	-5	-1	-	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-100	1	+100	μA
I_{BHL}	bus hold LOW current	V_{CC} = 3 V; V_I = 0.8 V	75	130	-	μA
I_{BHH}	bus hold HIGH current	V_{CC} = 3 V; V_I = 2.0 V	-	-140	-75	μA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [3]	500	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V; V_I = 0 V to 3.6 V	-	-	-500	μA
I_{EX}	external current	nYn output in HIGH-state when V_O > V_{CC}; V_O = 5.5 V; V_{CC} = 3.3 V	-	60	125	μA

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2$ V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care	[4]	-100	±1	+100	μA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}					
		V_O = 3.0 V		-	1	5	μA
		V_O = 0.5 V		-5	-1	-	μA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A					
		output HIGH		-	0.13	0.19	mA
		output LOW		-	2	5	mA
		outputs disabled	[5]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input at V_{CC} - 0.6 V and other inputs at V_{CC} or GND	[6]	-	0.1	0.2	mA
C_I	input capacitance	V_I = 0 V or 3.0 V		-	4	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V		-	8	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
[2] Unused pins at V_{CC} or GND.
[3] This is the bus hold overdrive current required to force the input to the opposite logic state.
[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.
[6] This is the increase in supply current for each input at V_{CC} - 0.6 V.

10. Dynamic characteristics

Table 7. Dynamic characteristics

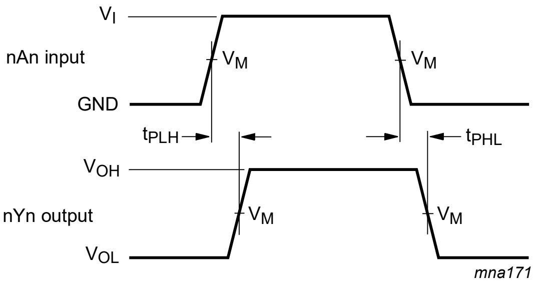
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	3.8	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	1.9	3.5	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	3.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	2.0	3.3	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nYn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	2.8	4.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nYn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	4.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.4	2.3	4.4	ns

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{PHZ}	HIGH to OFF-state propagation delay	n$\overline{OE}$ to nYn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	4.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.9	2.9	4.4	ns
t_{PLZ}	LOW to OFF-state propagation delay	n$\overline{OE}$ to nYn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	4.4	ns
		V_{CC} = 3.0 V to 3.6 V	1.8	2.5	4.4	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

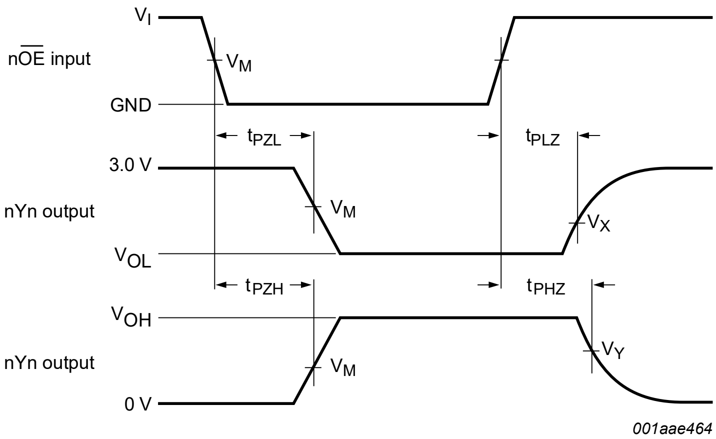
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Propagation delay input (nAn) to output (nYn)



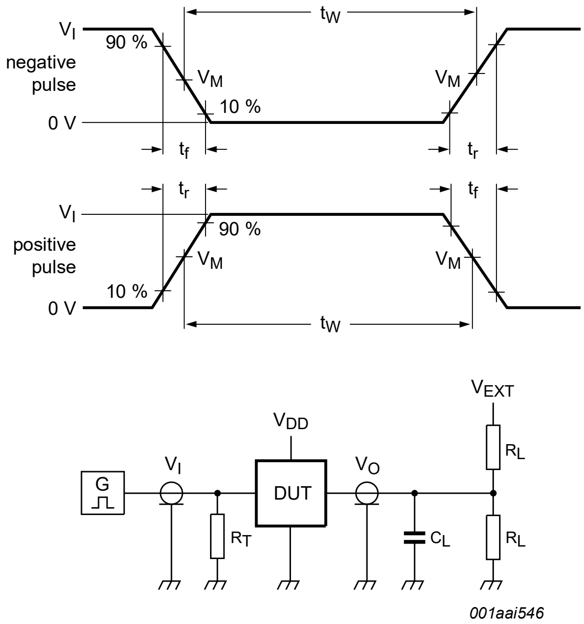
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. 3-state output enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

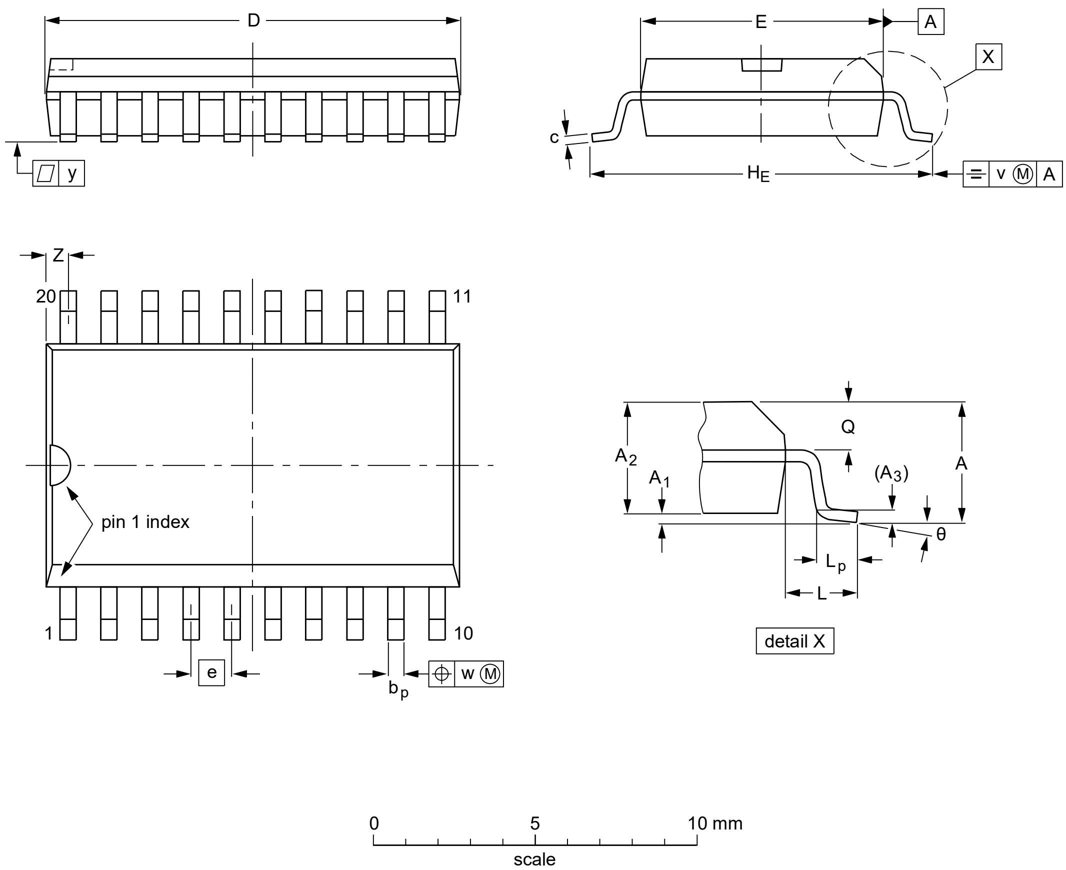
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(1)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

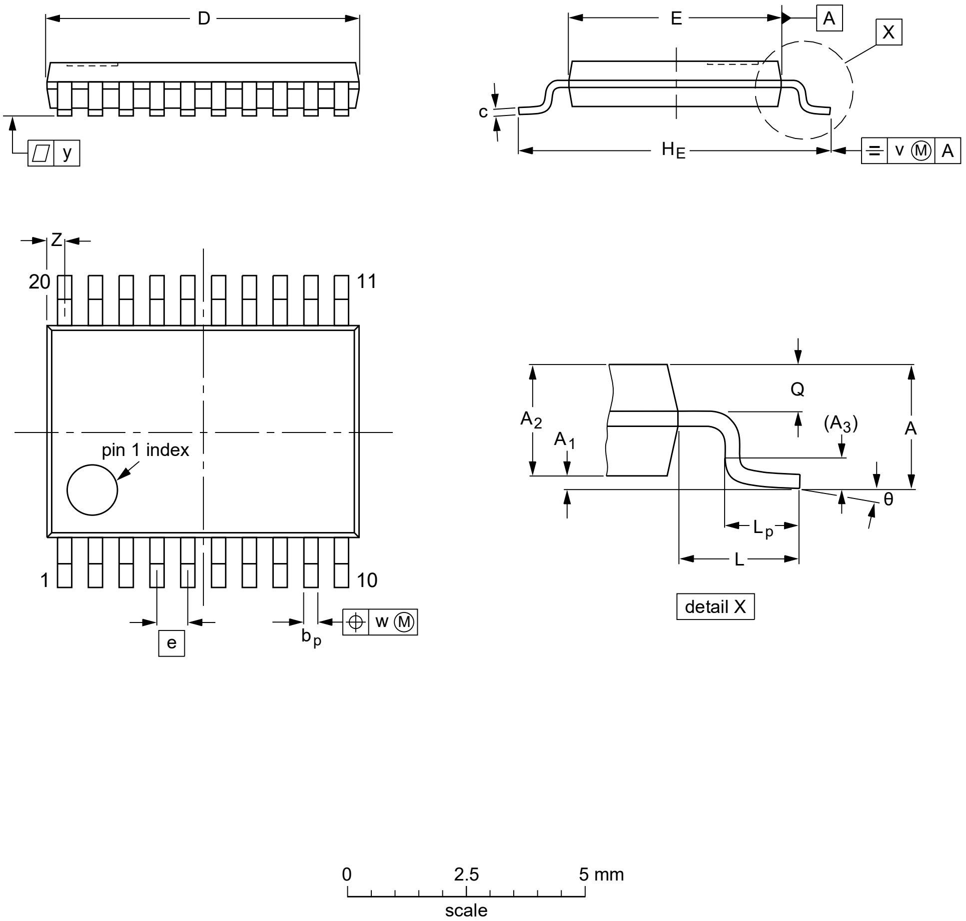
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 9. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244B v.6	20210812	Product data sheet	-	74LVT_LVTH244B v.5
Modifications:	• Type number 74LVT244BDB (SOT339-1/SSOP20) removed.			
74LVT_LVTH244B v.5	20210212	Product data sheet	-	74LVT_LVTH244B v.4
Modifications:	• Type number 74LVTH244BDB (SOT339-1 / SSOP20) removed. • Section 1 and Section 2 updated.			
74LVT_LVTH244B v.4	20170614	Product data sheet	-	74LVT_LVTH244B v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LVT_LVTH244B v.3	20060303	Product data sheet	-	74LVT244B v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 3: Added type numbers 74LVTH244BD, 74LVTH244BDB and 74LVTH244BPW.			
74LVT244B v.2	20030919	Product specification	-	74LVT244B v.1
74LVT244B v.1	19981101	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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