



# BC817RAPN

45 V, 500 mA NPN/PNP general-purpose double transistors

14 September 2018

Product data sheet

## 1. General description

NPN/PNP general-purpose double transistors in a leadless ultra small DFN1412-6 (SOT1268) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: BC817RA

PNP/PNP complement: BC807RA

## 2. Features and benefits

- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

## 3. Applications

- General-purpose switching and amplification
- Mobile applications

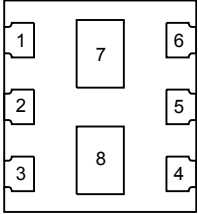
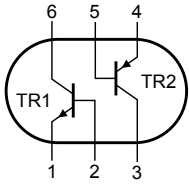
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$V_{CE0}$	collector-emitter voltage	open base	-	-	45	V
$I_C$	collector current		-	-	500	mA
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	1	A
$h_{FE}$	DC current gain	$V_{CE} = 1$ V; $I_C = 100$ mA; $T_{amb} = 25$ °C	160	-	400	
		$V_{CE} = 1$ V; $I_C = 500$ mA; pulsed; $t_p \leq 300$ $\mu$ s; $\delta \leq 0.02$ ; $T_{amb} = 25$ °C	40	-	-	

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>Transparent top view DFN1412-6 (SOT1268)</p>	 <p><i>sym019</i></p>
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BC817RAPN	DFN1412-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 mm x 1.2 mm x 0.47 mm	SOT1268

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BC817RAPN	A8

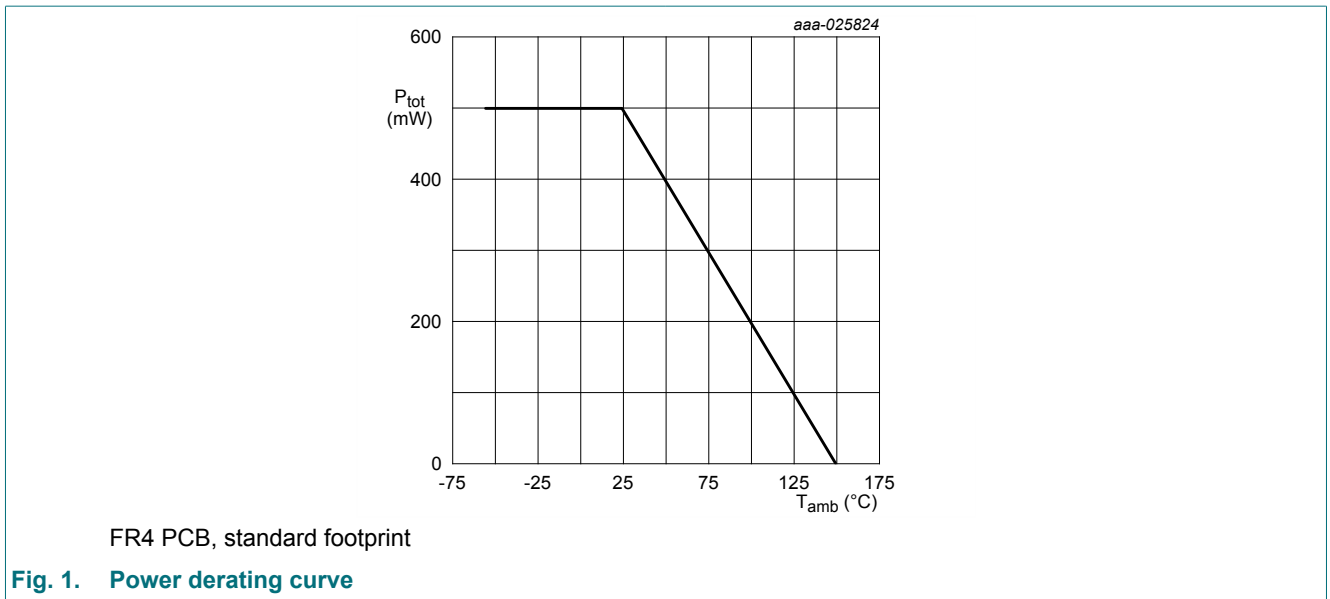
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>					
$V_{CBO}$	collector-base voltage	open emitter	-	50	V
$V_{CEO}$	collector-emitter voltage	open base	-	45	V
$V_{EBO}$	emitter-base voltage	open collector	-	5	V
$I_C$	collector current		-	500	mA
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	1	A
$I_{BM}$	peak base current		-	200	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25$ °C	[1]	350	mW
<b>Per device</b>					
$P_{tot}$	total power dissipation	$T_{amb} \leq 25$ °C	[1]	500	mW
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-55	150	°C
$T_{stg}$	storage temperature		-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

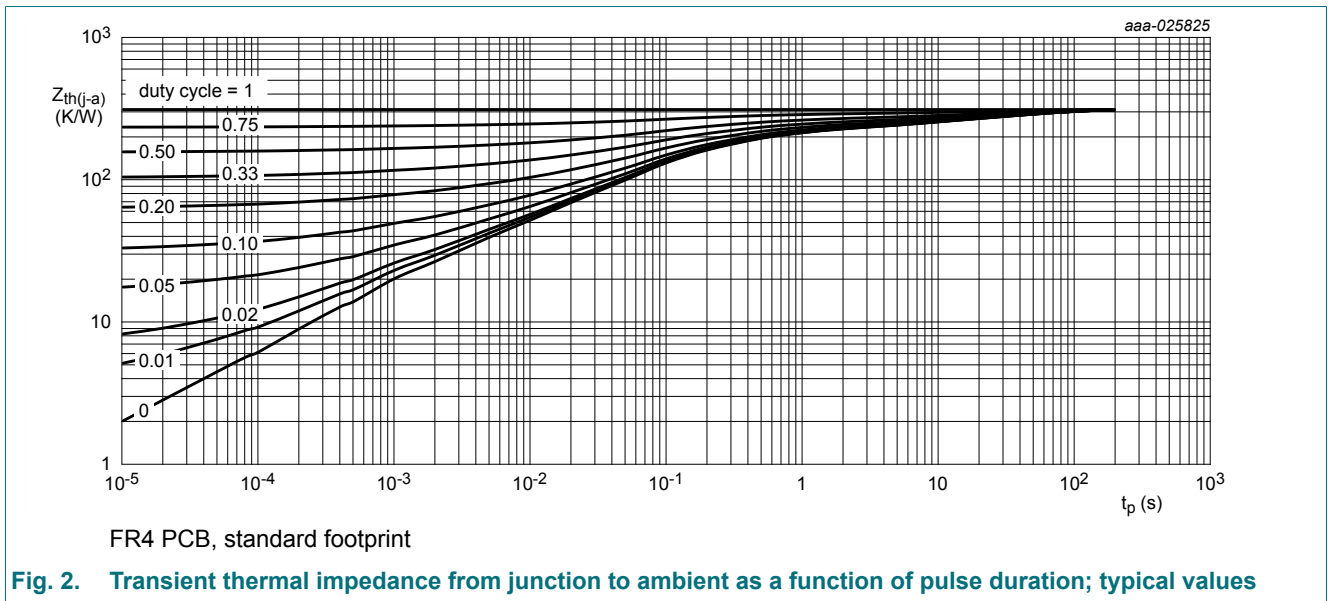


## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	358	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W

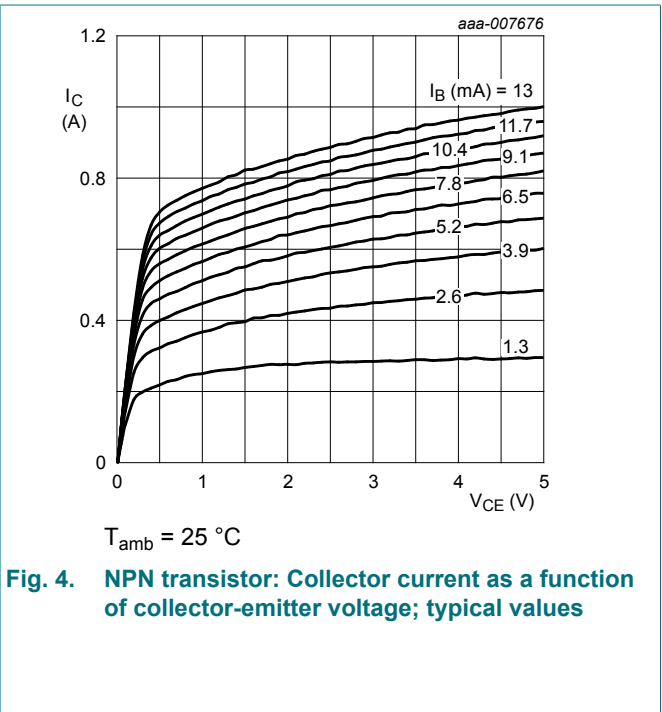
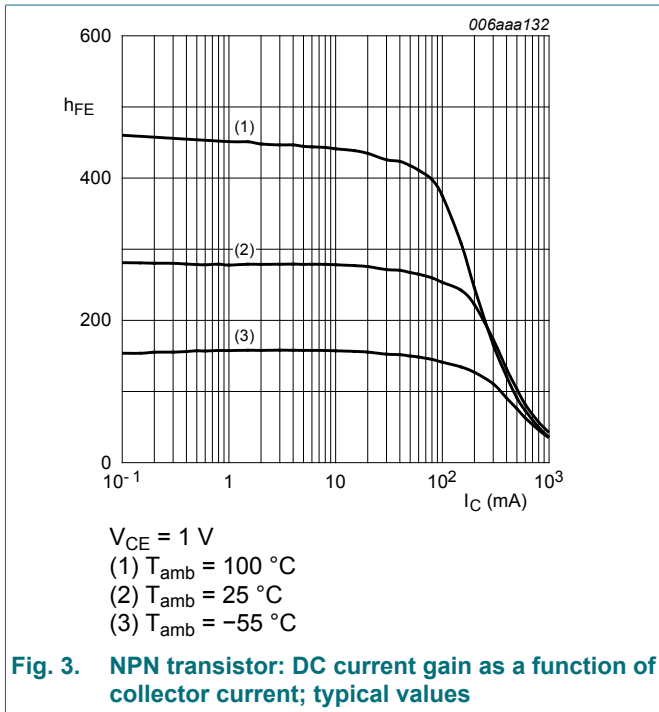
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

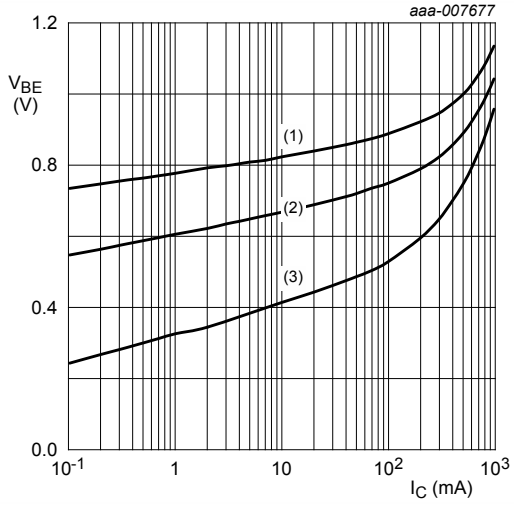


## 10. Characteristics

Table 7. Characteristics

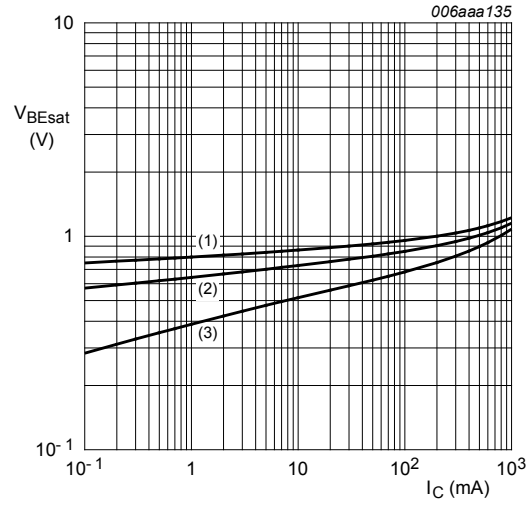
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 20\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	100	nA
		$V_{CB} = 20\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ °C}$	-	-	5	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 1\text{ V}; I_C = 100\text{ mA}; T_{amb} = 25\text{ °C}$	160	-	400	
		$V_{CE} = 1\text{ V}; I_C = 500\text{ mA}; \text{pulsed}; t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	40	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 500\text{ mA}; I_B = 50\text{ mA}; \text{pulsed}; t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	-	-	700	mV
$V_{BE}$	base-emitter voltage	$V_{CE} = 1\text{ V}; I_C = 500\text{ mA}; T_{amb} = 25\text{ °C}$	-	-	1.2	V
<b>Per transistor</b>						
$C_C$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$	-	3	-	pF
		$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$	-	6	-	pF
$f_T$	transition frequency	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ °C}$	100	-	-	MHz
		$V_{CE} = -5\text{ V}; I_C = -10\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ °C}$	80	-	-	MHz





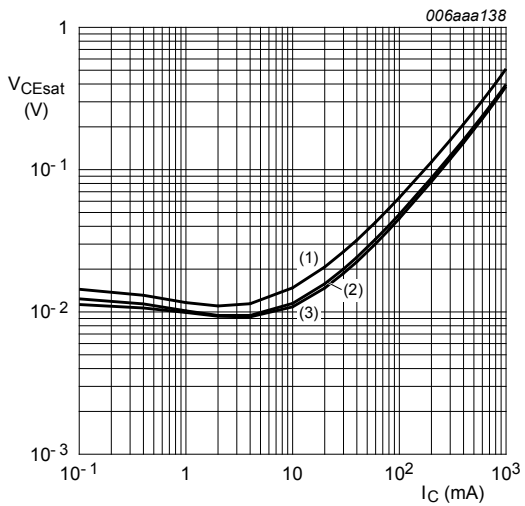
$V_{CE} = 1\text{ V}$   
 (1)  $T_{amb} = -55\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig. 5. NPN transistor: Base-emitter voltage as a function of collector current; typical values**



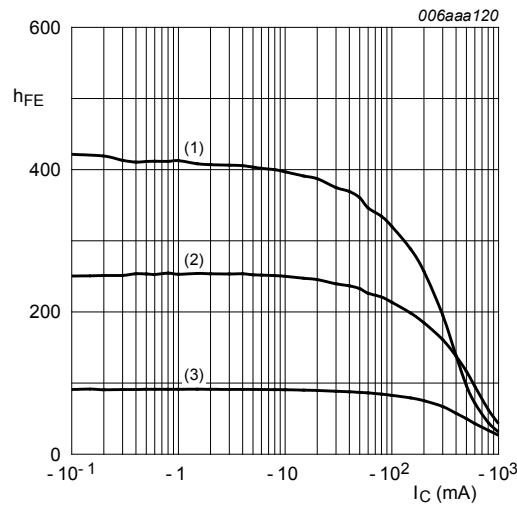
$I_C/I_B = 10$   
 (1)  $T_{amb} = -55\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig. 6. NPN transistor: Base-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 10$   
 (1)  $T_{amb} = -55\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig. 7. NPN transistor: Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = -1\text{ V}$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig. 8. PNP transistor: DC current gain as a function of collector current; typical values**

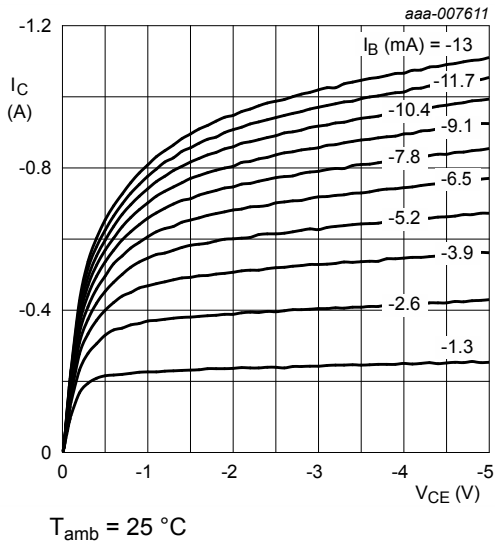


Fig. 9. PNP transistor: Collector current as a function of collector-emitter voltage; typical values

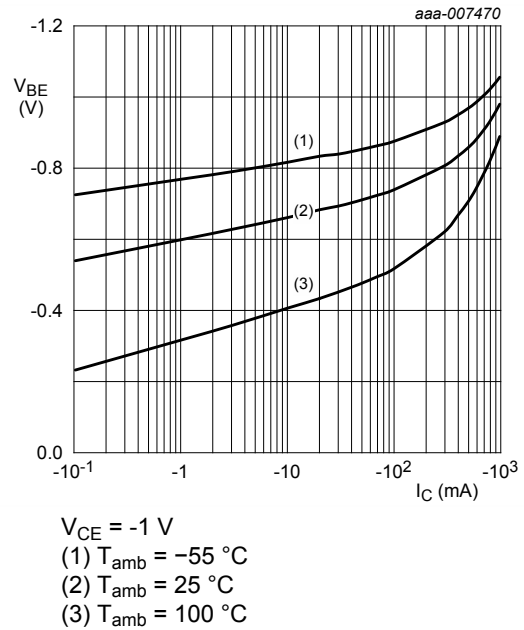


Fig. 10. PNP transistor: Base-emitter voltage as a function of collector current; typical values

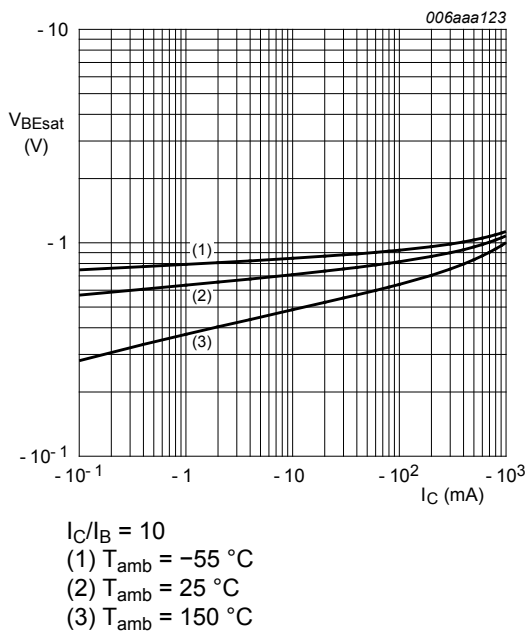


Fig. 11. PNP transistor: Base-emitter saturation voltage as a function of collector current; typical values

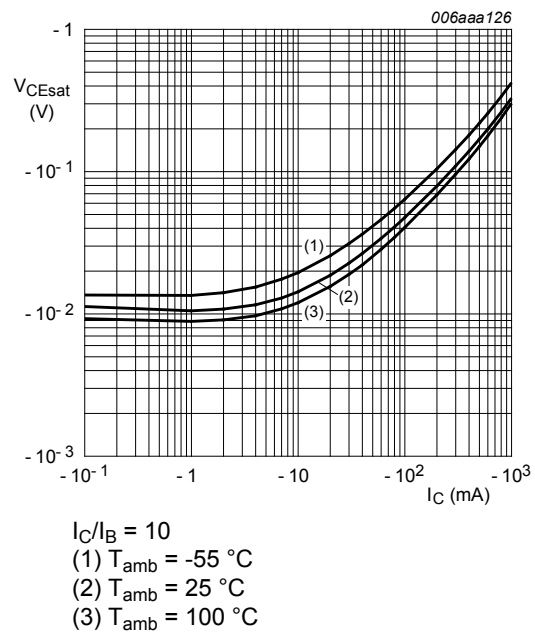


Fig. 12. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN1412-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 x 1.2 x 0.47 mm

SOT1268

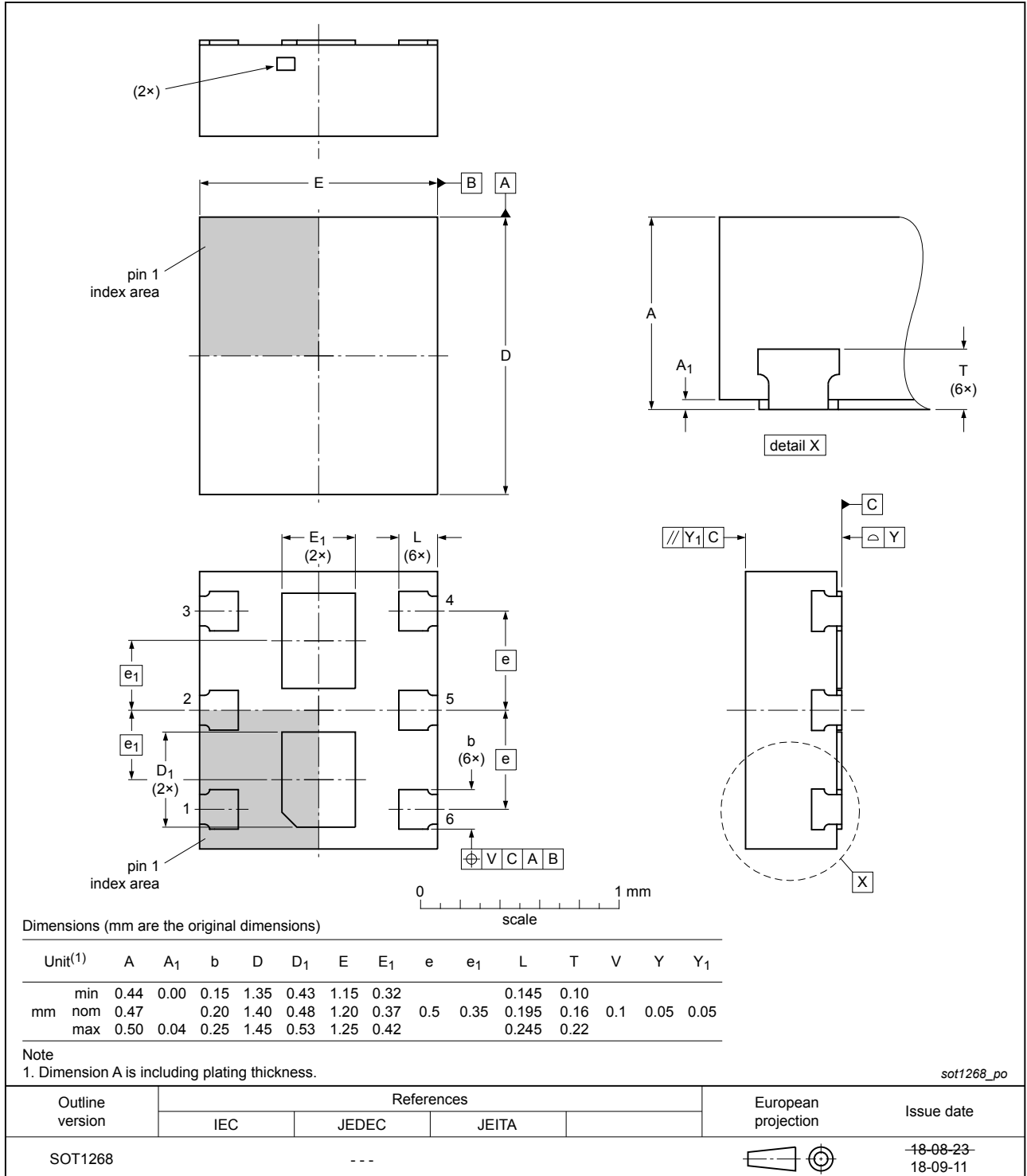


Fig. 13. Package outline DFN1412-6 (SOT1268)



### 13. Soldering

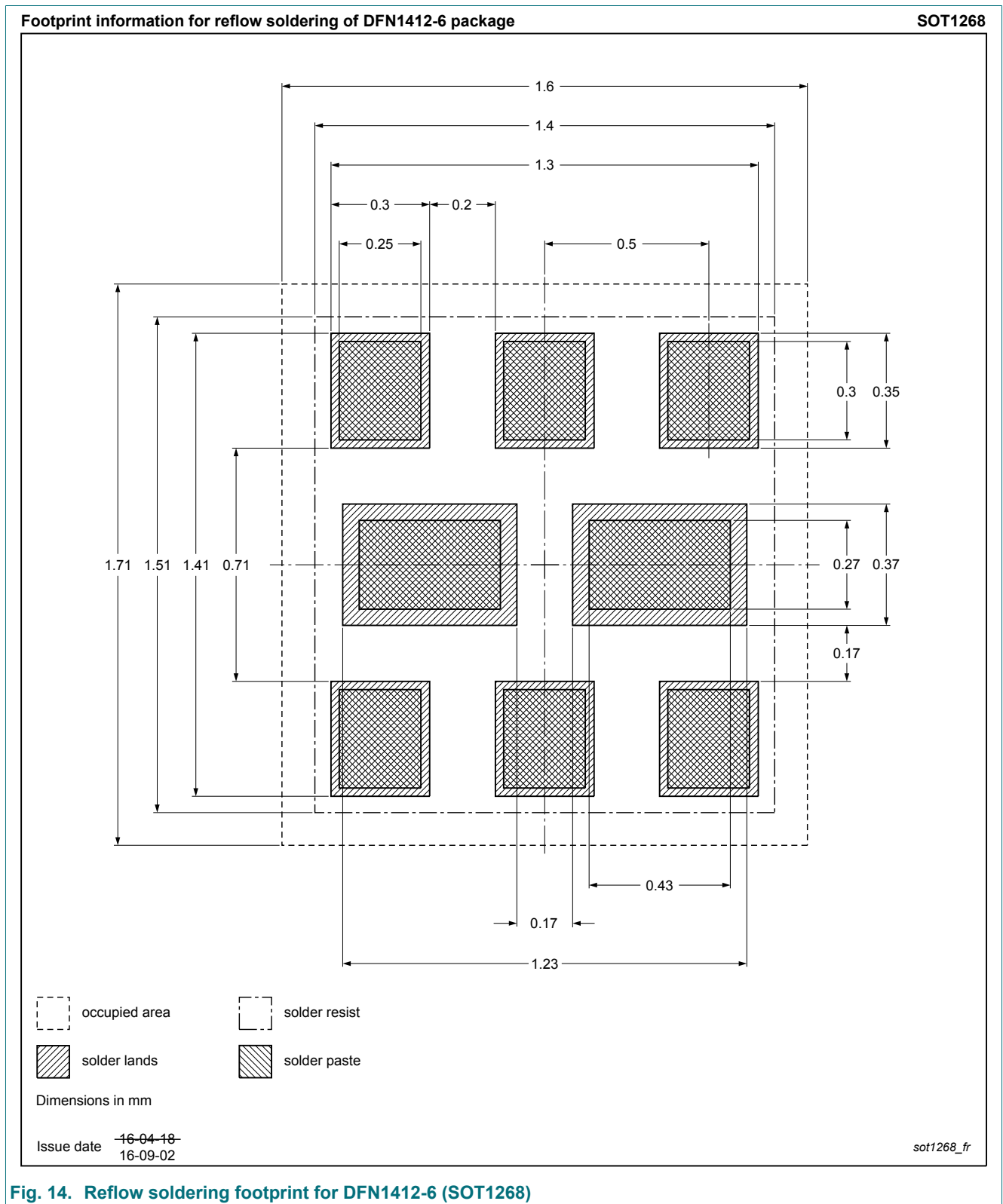


Fig. 14. Reflow soldering footprint for DFN1412-6 (SOT1268)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BC817RAPN v.2	20180914	Product data sheet	-	BC817RAPN v.1
Modifications:	• Package outline drawing updated: Unit T added			
BC817RAPN v.1	20170613	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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