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Team Nexperia

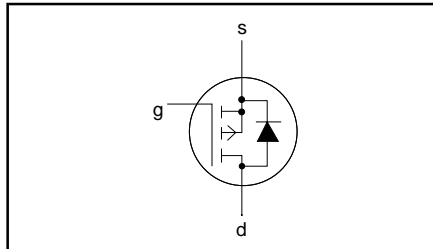
## P-channel enhancement mode MOS transistor

## BSH201

### FEATURES

- Low threshold voltage
- Fast switching
- Logic level compatible
- Subminiature surface mount package

### SYMBOL



### QUICK REFERENCE DATA

$V_{DS} = -60 \text{ V}$
$I_D = -0.3 \text{ A}$
$R_{DS(ON)} \leq 2.5 \Omega (V_{GS} = -10 \text{ V})$

### GENERAL DESCRIPTION

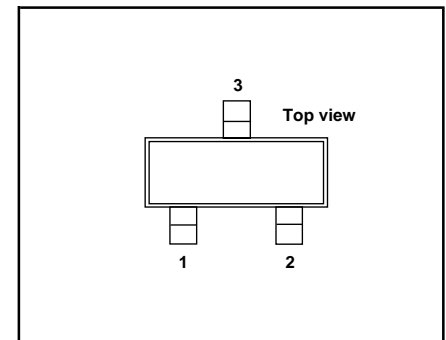
P-channel, enhancement mode, logic level, field-effect power transistor. This device has low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The BSH201 is supplied in the SOT23 subminiature surface mounting package.

### PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

### SOT23



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage		-	-60	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	-60	V
$V_{GS}$	Gate-source voltage		-	$\pm 20$	V
$I_D$	Drain current (DC)	$T_a = 25 \text{ }^\circ\text{C}$	-	-0.3	A
		$T_a = 100 \text{ }^\circ\text{C}$	-	-0.19	A
$I_{DM}$	Drain current (pulse peak value)	$T_a = 25 \text{ }^\circ\text{C}$	-	-1.2	A
$P_{tot}$	Total power dissipation	$T_a = 25 \text{ }^\circ\text{C}$	-	0.417	W
		$T_a = 100 \text{ }^\circ\text{C}$	-	0.17	W
$T_{stg}, T_j$	Storage & operating temperature		-55	150	$^\circ\text{C}$

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint	300	-	K/W

## P-channel enhancement mode MOS transistor

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### ELECTRICAL CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = -10\ \mu\text{A}$	-60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = -1\ \text{mA}$	-1	-1.9	-	V
		$T_j = 150^\circ\text{C}$	-0.4	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = -10\ \text{V}; I_D = -160\ \text{mA}$	-	2.1	2.5	$\Omega$
		$V_{GS} = -4.5\ \text{V}; I_D = -80\ \text{mA}$	-	2.7	3.75	$\Omega$
		$V_{GS} = -10\ \text{V}; I_D = -160\ \text{mA}; T_j = 150^\circ\text{C}$	-	3.6	4.25	$\Omega$
$g_{fs}$	Forward transconductance	$V_{DS} = -48\ \text{V}; I_D = -160\ \text{mA}$	0.1	0.35	-	S
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-	$\pm 10$	$\pm 100$	nA
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = -48\ \text{V}; V_{GS} = 0\ \text{V}; T_j = 150^\circ\text{C}$	-	-50	-100	nA
			-	-1.3	-10	$\mu\text{A}$
$Q_{g(tot)}$	Total gate charge	$I_D = -0.5\ \text{A}; V_{DD} = -10\ \text{V}; V_{GS} = -10\ \text{V}$	-	3	-	nC
$Q_{gs}$	Gate-source charge		-	0.5	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	0.4	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = -10\ \text{V}; I_D = -0.5\ \text{A};$	-	2	-	ns
$t_r$	Turn-on rise time	$V_{GS} = -10\ \text{V}; R_G = 6\ \Omega$	-	4.5	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	45	-	ns
$t_f$	Turn-off fall time		-	20	-	ns
$C_{iss}$	Input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = -48\ \text{V}; f = 1\ \text{MHz}$	-	70	-	pF
$C_{oss}$	Output capacitance		-	15	-	pF
$C_{rss}$	Feedback capacitance		-	5	-	pF

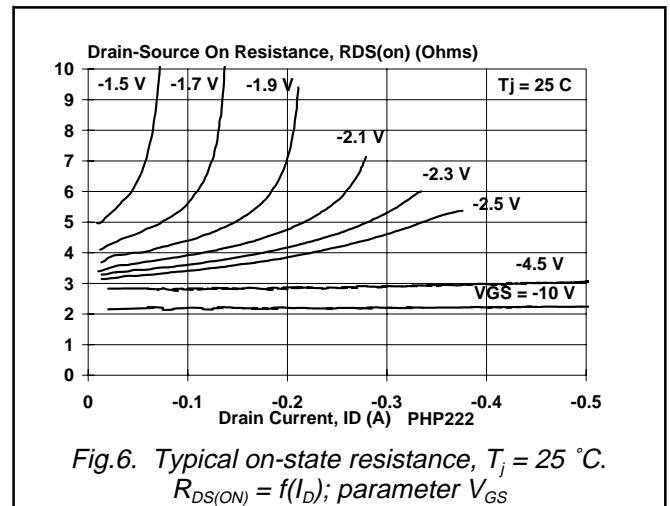
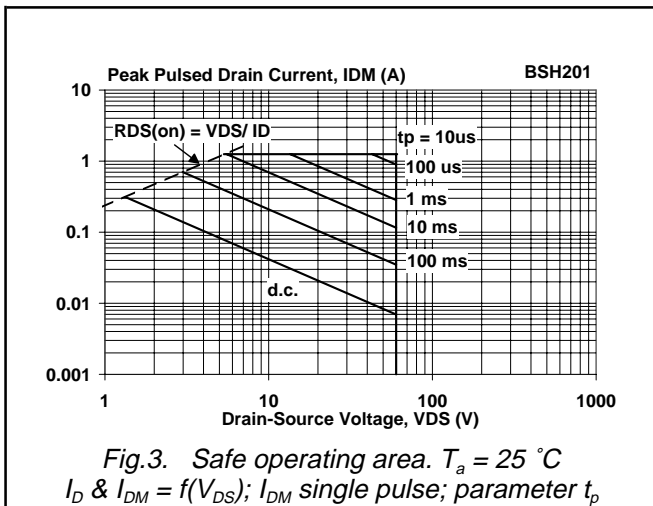
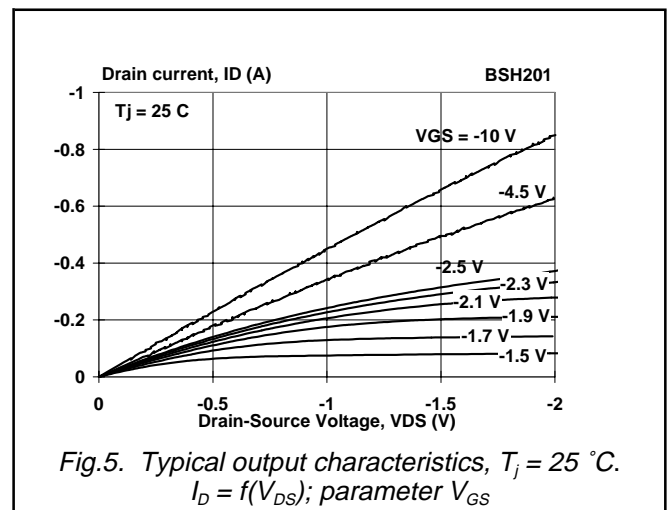
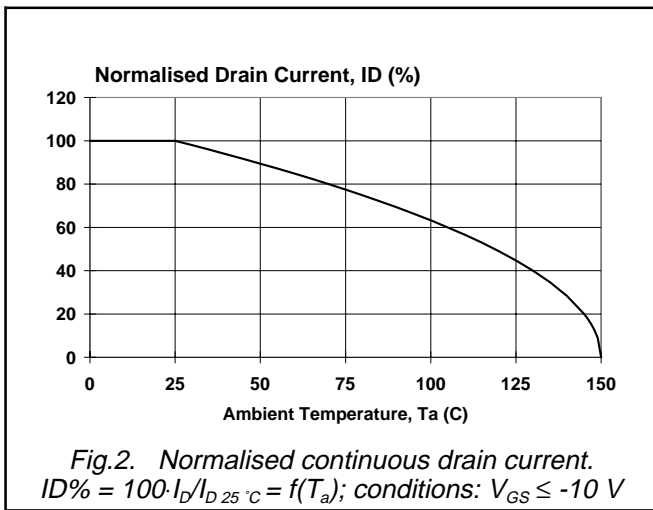
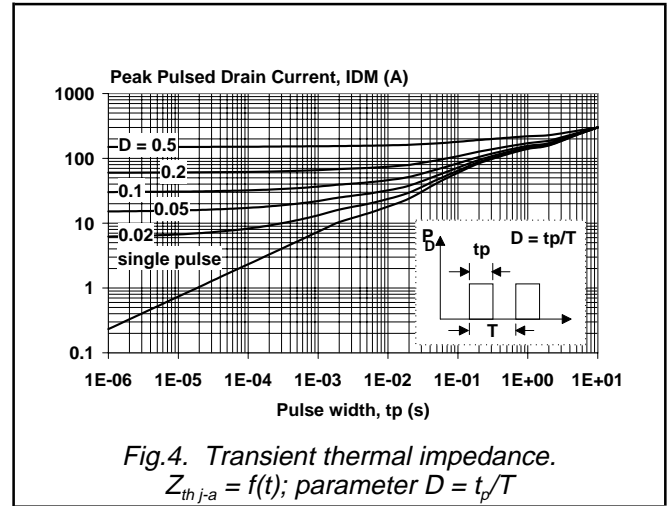
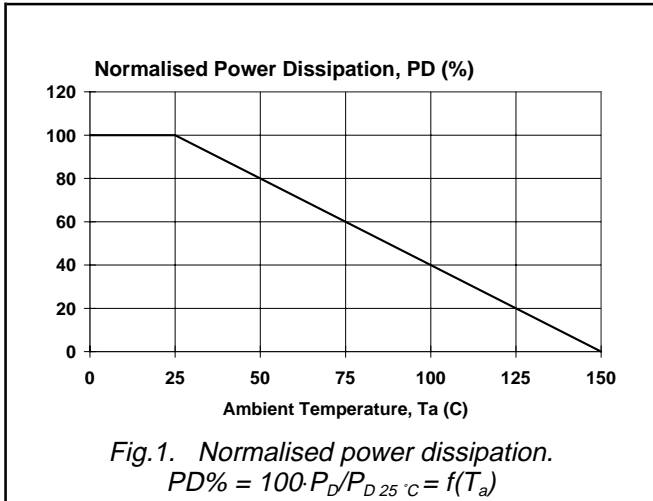
### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current	$T_a = 25^\circ\text{C}$	-	-	-0.3	A
$I_{DRM}$	Pulsed reverse drain current		-	-	-1.2	A
$V_{SD}$	Diode forward voltage	$I_F = -0.38\ \text{A}; V_{GS} = 0\ \text{V}$	-	-0.97	-1.3	V
$t_{rr}$	Reverse recovery time	$I_F = -0.25\ \text{A}; -di_F/dt = 100\ \text{A}/\mu\text{s};$	-	38	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = 0\ \text{V}; V_R = -48\ \text{V}$	-	58	-	nC

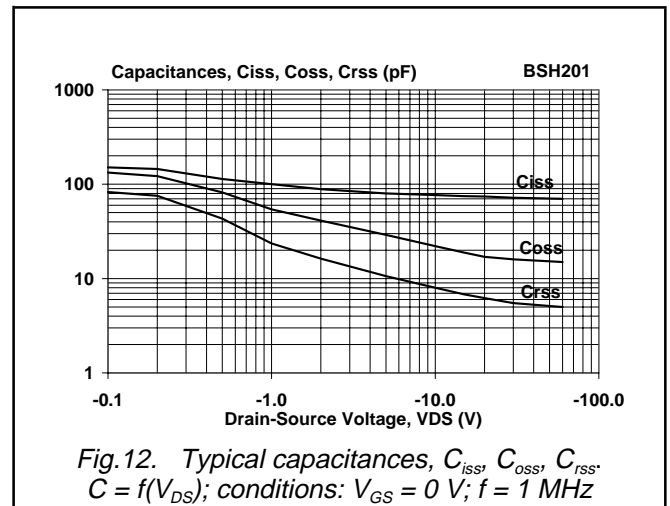
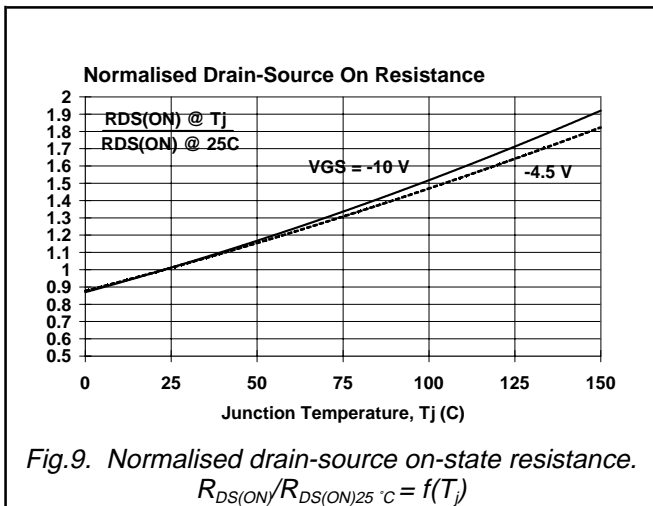
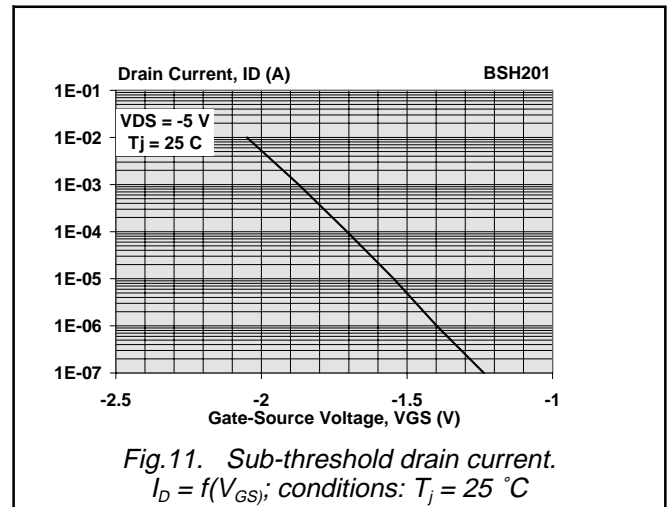
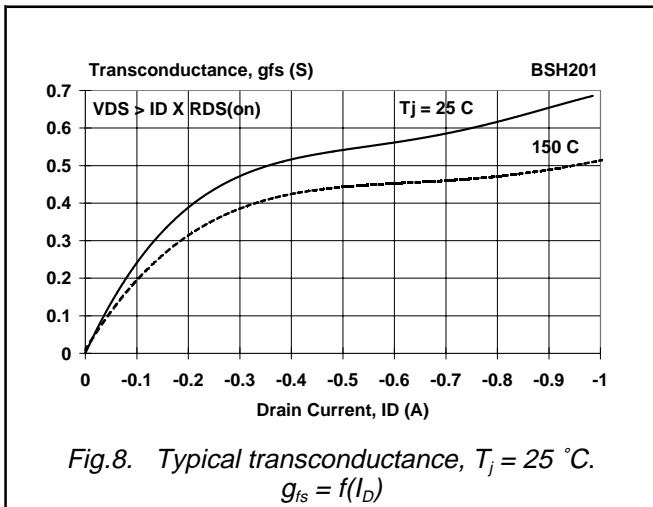
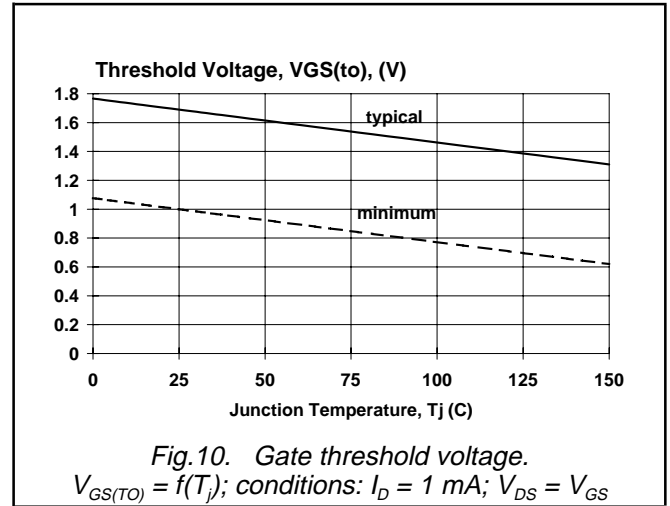
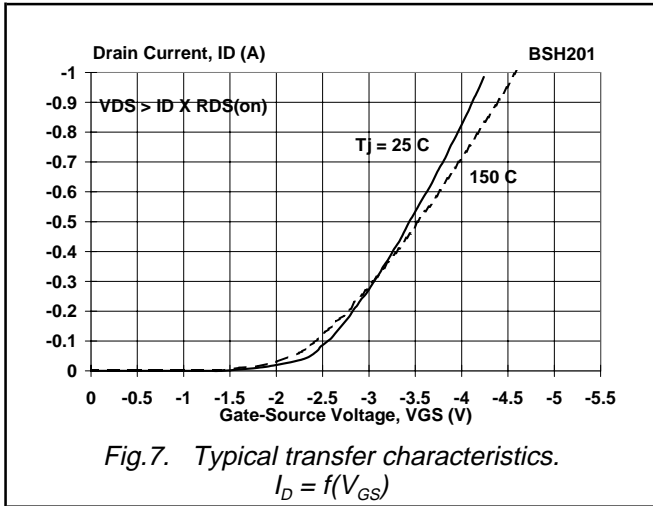
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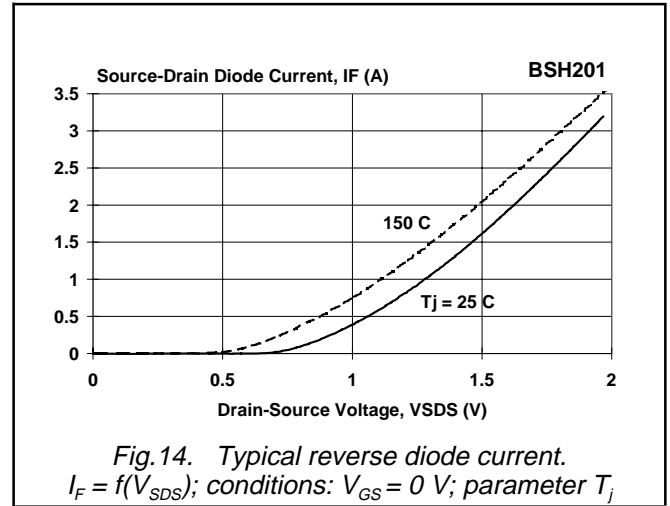
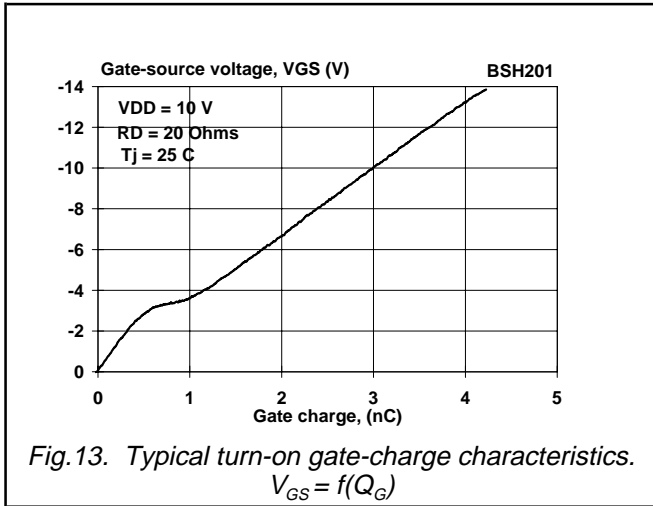
P-channel enhancement mode MOS transistor

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P-channel enhancement mode  
MOS transistor

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P-channel enhancement mode  
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**MECHANICAL DATA**

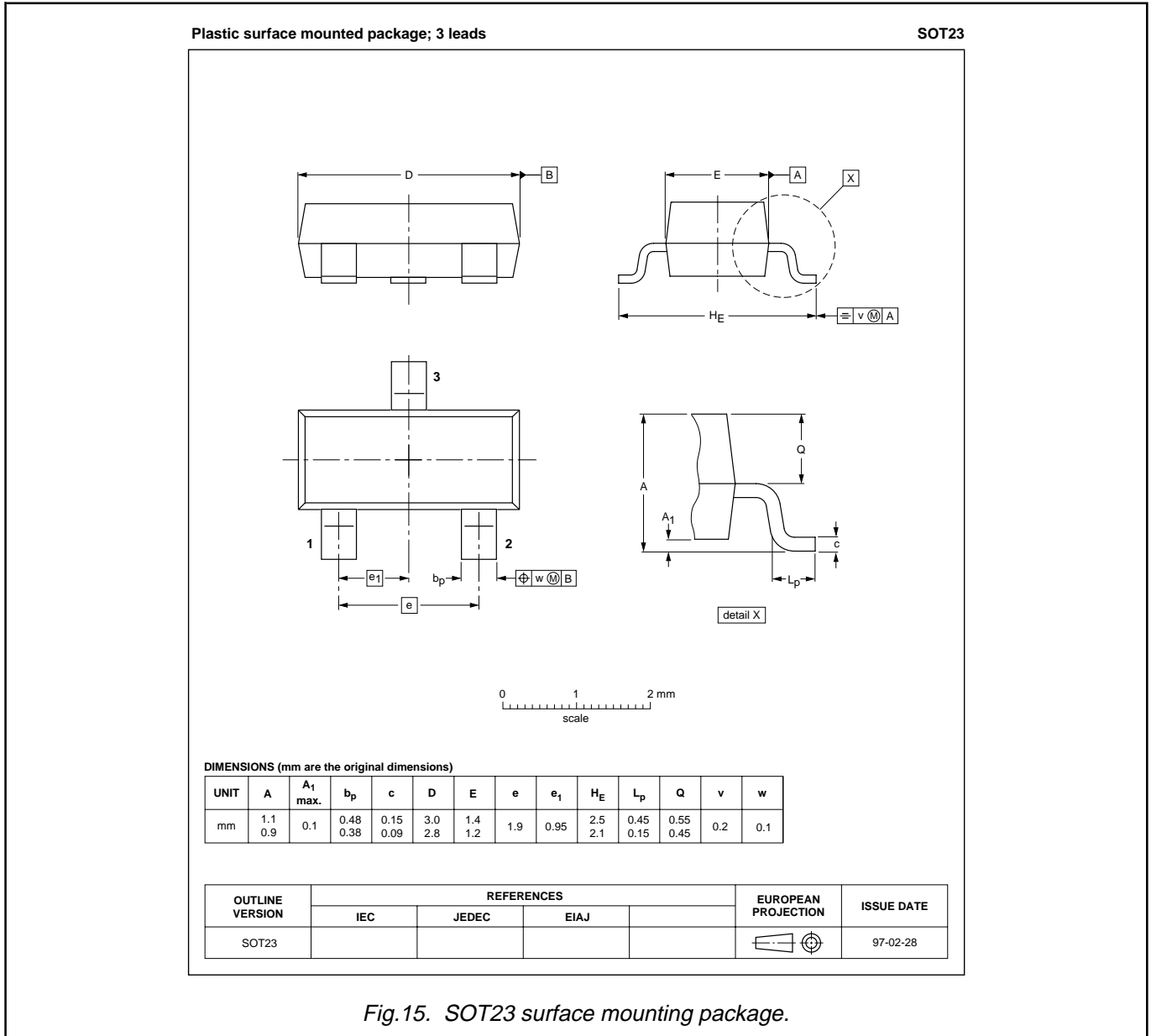


Fig.15. SOT23 surface mounting package.

**Notes**

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
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