Product data sheet

1. General description

P-channel enhancement mode MOSFET in an LFPAK56 (Power SO8) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

This product has been designed and qualified to AEC-Q101 standard for use in high-performance automotive applications such as reverse battery protection.

2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- · Reverse battery protection
- Power management
- · High-side loadswitch
- Motor drive

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-60	V	
V_{GS}	gate-source voltage		[1]	-20	-	20	V	
I _D	drain current	V _{GS} = -10 V; T _{mb} = 25 °C		-	-	-25	Α	
P _{tot}	total power dissipation	T _{mb} = 25 °C		-	-	66	W	
Static characte	Static characteristics							
R _{DSon}	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -4.7 \text{ A}; T_j = 25 \text{ °C}$		-	48	61	mΩ	

[1] $V_{GS} = -20 \text{ V/+}5 \text{ V}$ according AEC-Q101 at $T_i = 175 \text{ °C}$; $V_{GS} = -20 \text{ V/+}20 \text{ V}$ according AEC-Q101 at $T_i = 150 \text{ °C}$



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	a	G (F)
4	G	gate		s
mb	D	mounting base; connected to drain	LFPAK56; Power- SO8 (SOT669)	017aaa094

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
BUK6Y61-60P	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669			

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6Y61-60P	6Y6160P

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-60	V
V _{GS}	gate-source voltage		[1]	-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{mb} = 25 °C		-	-25	Α
		V _{GS} = -10 V; T _{mb} = 100 °C		-	-17.7	Α
I _{DM}	peak drain current	single pulse; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$		-	-100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C		-	66	W
Tj	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drai	n diode				'	_
Is	source current	T _{mb} = 25 °C		-	-25	Α
I _{SM}	peak source current	single pulse; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$		-	-100	Α
ESD maxim	um rating			-	'	
V _{ESD}	electrostatic discharge voltage	НВМ	[2]	-	800	V
Avalanche r	uggedness		'	'		
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = -4.6 A; DUT in avalanche (unclamped)		-	61	mJ

- [1] $V_{GS} = -20 \text{ V/+5 V}$ according AEC-Q101 at $T_j = 175 \text{ °C}$; $V_{GS} = -20 \text{ V/+20 V}$ according AEC-Q101 at $T_j = 150 \text{ °C}$
- [2] Measured between all pins.

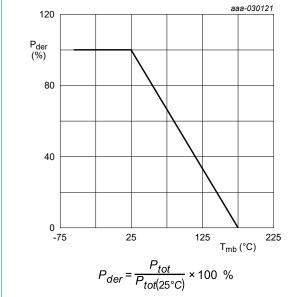
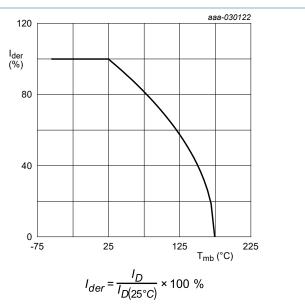


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



ig. 2. Normalized continuous drain current as a function of mounting base temperature

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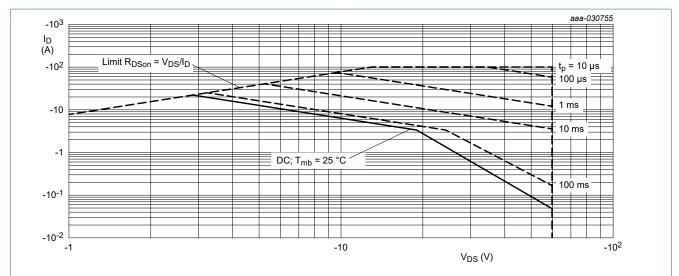
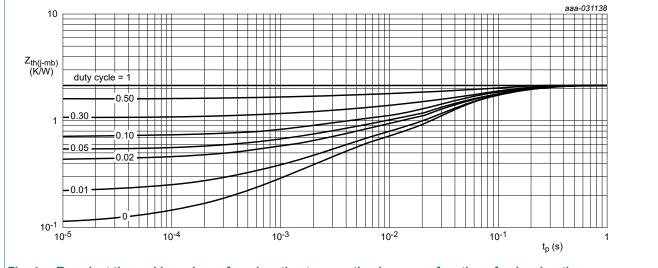


Fig. 3. Safe operating area; junction to mounting base; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base		-	1.8	2.3	K/W



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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	I_D = -250 μ A; V_{GS} = 0 V; T_j = 25 °C	-60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \ \mu A; \ V_{DS} = V_{GS}; \ T_j = 25 \ ^{\circ}C$	-1.5	-2	-3	V
I _{DSS}	drain leakage current	V _{DS} = -60 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μΑ
		V _{DS} = -60 V; V _{GS} = 0 V; T _j = 125 °C	-	-	-10	μΑ
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state	$V_{GS} = -10 \text{ V}; I_D = -4.7 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	48	61	mΩ
	resistance	$V_{GS} = -10 \text{ V}; I_D = -4.7 \text{ A}; T_j = 175 ^{\circ}\text{C}$	-	100	130	mΩ
		$V_{GS} = -4.5 \text{ V}; I_D = -3.8 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	62	93	mΩ
9 _{fs}	forward transconductance	V_{DS} = -10 V; I_D = -4 A; T_j = 25 °C	-	65	-	S
R_G	gate resistance	f = 1 MHz; T _j = 25 °C	-	12	-	Ω
Dynamic ch	naracteristics		'	-		
Q _{G(tot)}	total gate charge	V _{DS} = -30 V; I _D = -4.7 A; V _{GS} = -10 V;	-	20	30	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	3.3	-	nC
Q_{GD}	gate-drain charge		-	4.3	-	nC
C _{iss}	input capacitance	V _{DS} = -30 V; f = 1 MHz; V _{GS} = 0 V;	-	1060	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	85	-	pF
C _{rss}	reverse transfer capacitance		-	49	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = -30 \text{ V}; I_D = -4.7 \text{ A}; V_{GS} = -10 \text{ V};$	-	12	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	58	-	ns
t _{d(off)}	turn-off delay time	1	-	21	-	ns
t _f	fall time	1	-	204	-	ns
Source-drai	in diode		1			
V _{SD}	source-drain voltage	I _S = -22.4 A; V _{GS} = 0 V; T _j = 25 °C	-	-0.7	-1.2	V
t _{rr}	reverse recovery time	I _S = -22.4 A; dI _S /dt = 100 A/µs;	-	30	-	ns
Q _r	recovered charge	V_{GS} = -10 V; V_{DS} = -30 V; T_j = 25 °C	_	37	_	nC

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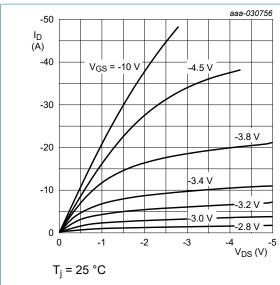


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

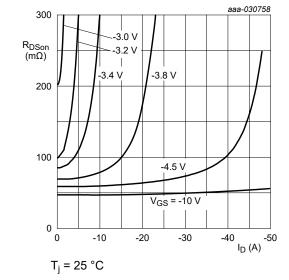


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

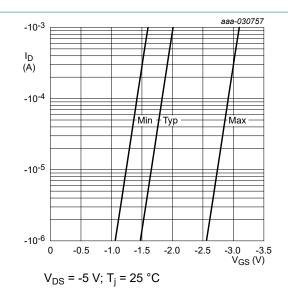


Fig. 6. Sub-threshold drain current as a function of gate-source voltage

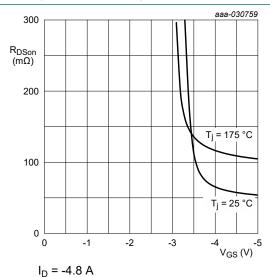


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

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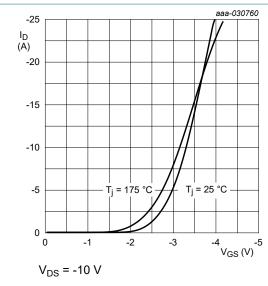


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

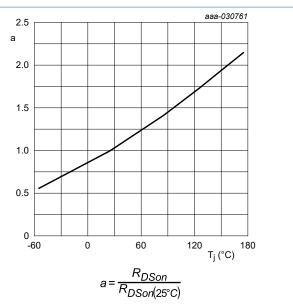


Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values

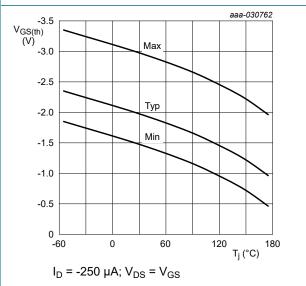


Fig. 11. Gate-source threshold voltage as a function of junction temperature

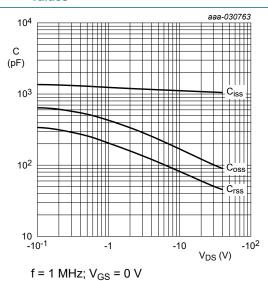


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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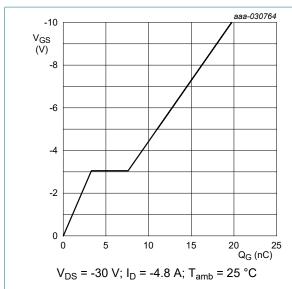


Fig. 13. Gate-source voltage as a function of gate charge; typical values

 $V_{GS} = 0 V$

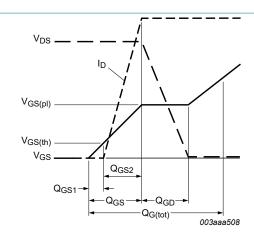


Fig. 14. Gate charge waveform definitions

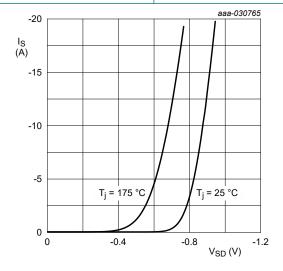
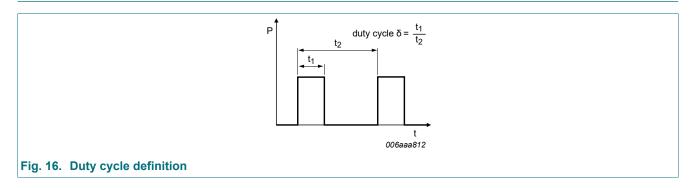


Fig. 15. Source current as a function of source-drain voltage; typical values

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11. Test information



Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

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12. Package outline

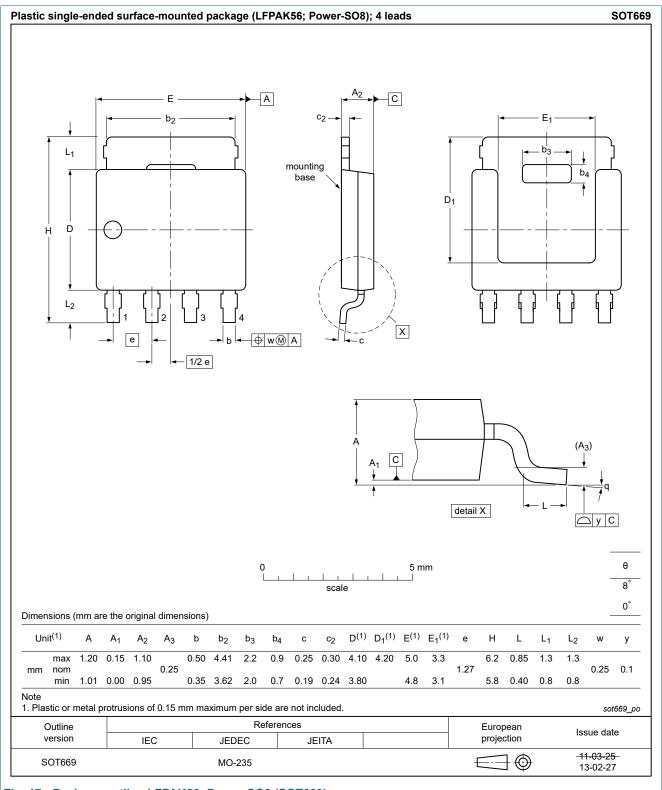


Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

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13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6Y61-60P v.1	20200316	Product data sheet	-	-

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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