



BUK7S2R5-40H

N-channel 40 V, 2.5 mOhm standard level MOSFET in LFPAK88

6 April 2021

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a copper-clip LFPAK88 package. This product has been fully designed and qualified to meet beyond AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

- Fully automotive qualified to beyond AEC-Q101:
 - -55 °C to +175 °C rating suitable for thermally demanding environments
- LFPAK88 package:
 - Designed for smaller footprint and improved power density over older wire bond packages such as D²PAK for today's space constrained high power automotive applications
 - Thin package and copper clip enables LFPAK88 to be highly efficient thermally
- LFPAK copper clip technology enabling improvements over wire bond packages by:
 - Increased maximum current capability and excellent current spreading
 - Improved R_{DSon}
 - Low source inductance
 - Low thermal resistance R_{th}
- LFPAK Gull Wing leads:
 - Flexible leads enabling high Board Level Reliability absorbing mechanical and thermal cycling stress, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joint
- Unique 40 V Trench 9 superjunction technology:
 - Reduced cell pitch and superjunction platform enables lower R_{DSon} in the same footprint
 - Improved SOA and avalanche capability compared to standard TrenchMOS
 - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs

3. Applications

- 12 V automotive systems
- 48 V DC/DC systems (on 12 V secondary side)
- Higher power motors, lamps and solenoid control
- Reverse polarity protection
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

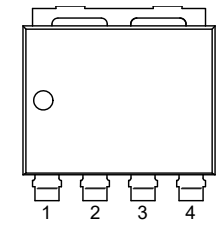
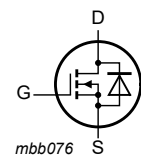
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	[1]	-	-	140	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$		-	-	135	W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	1.51	2.16	2.51	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14	-	7	14	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; [2]	-	19.1	-	nC
S	softness factor	$V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 17	-	0.89	-	

- [1] 140A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating temperature
 [2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFPAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	Source		
3	S	Source		
4	S	Source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7S2R5-40H	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7S2R5-40H	7S2R540H

8. Limiting values

Table 5. Limiting values

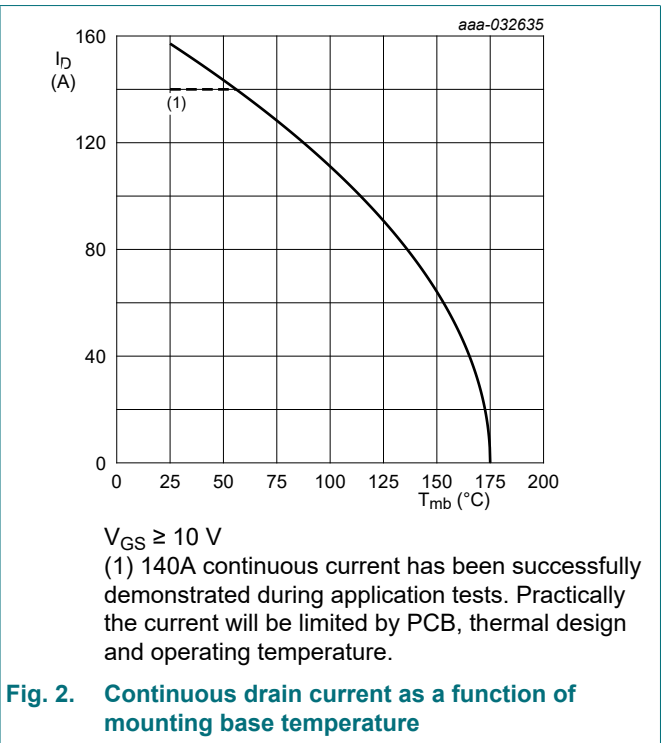
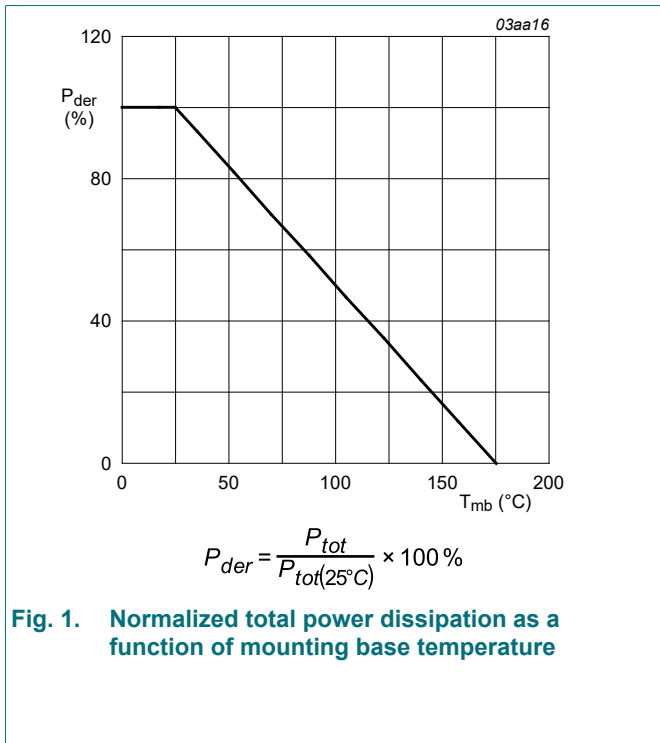
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	40	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V _{GS}	gate-source voltage	DC; T _j = 175 °C		-10	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	135	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	140	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	629	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[2]	-	135	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	629	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 96 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[3] [4]	-	80	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[5]	-	96	A

- [1] 140A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating temperature
- [2] 135A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating temperature
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.
- [5] Protected by 100% test.



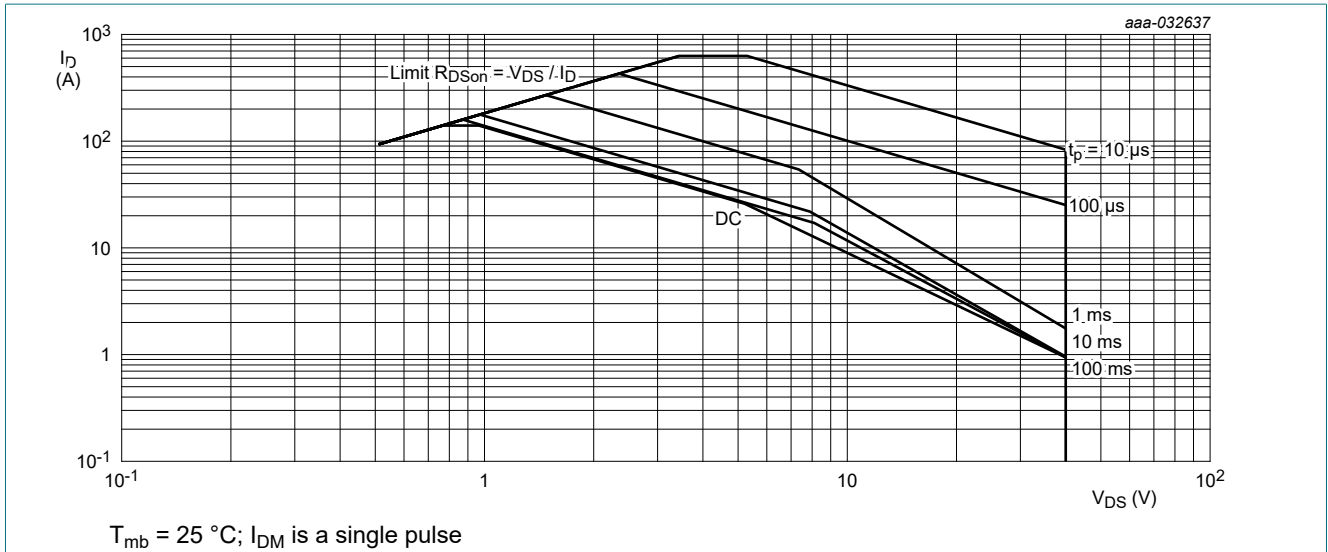


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

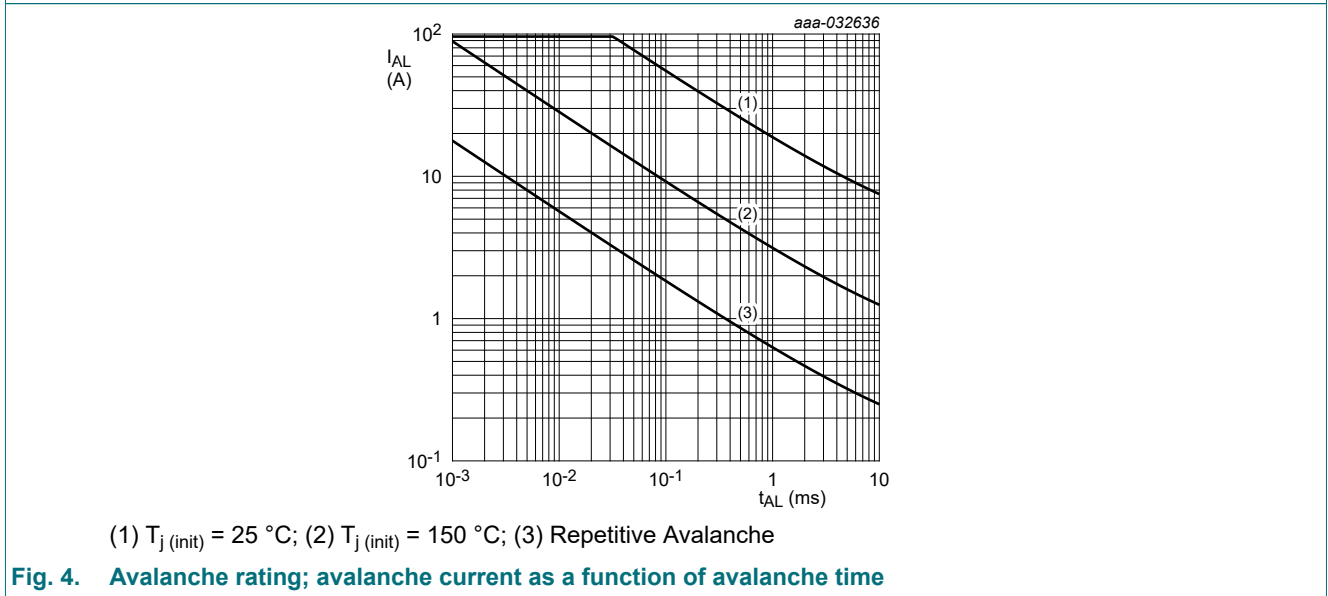


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.97	1.11	K/W

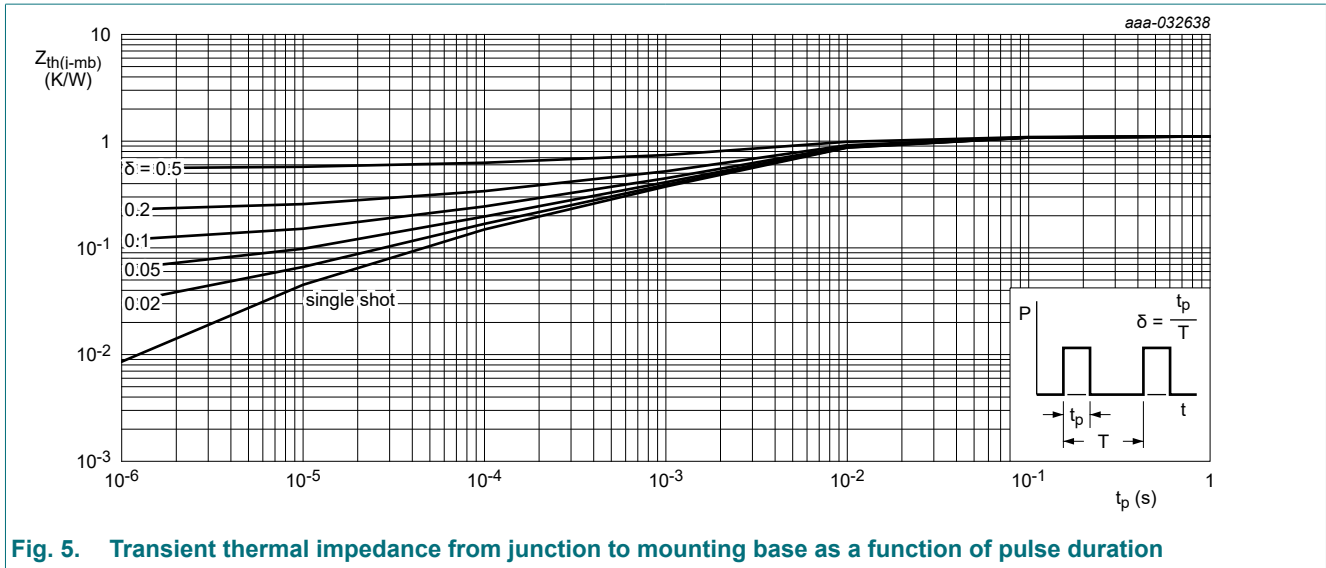


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

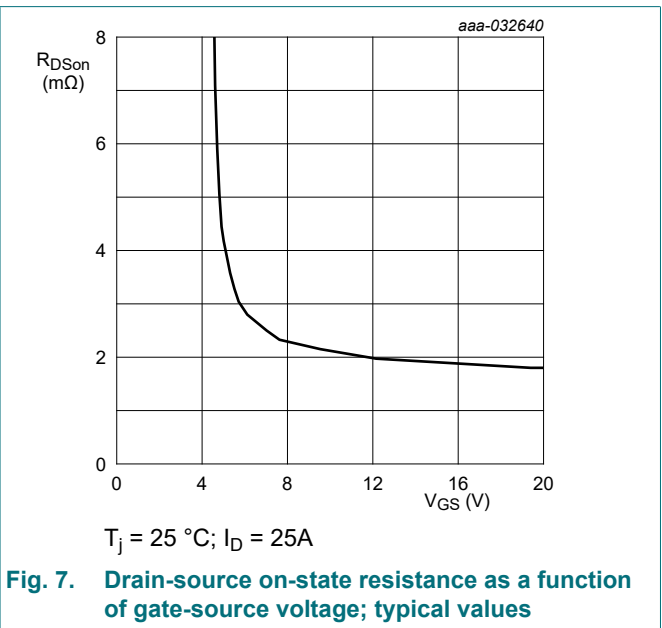
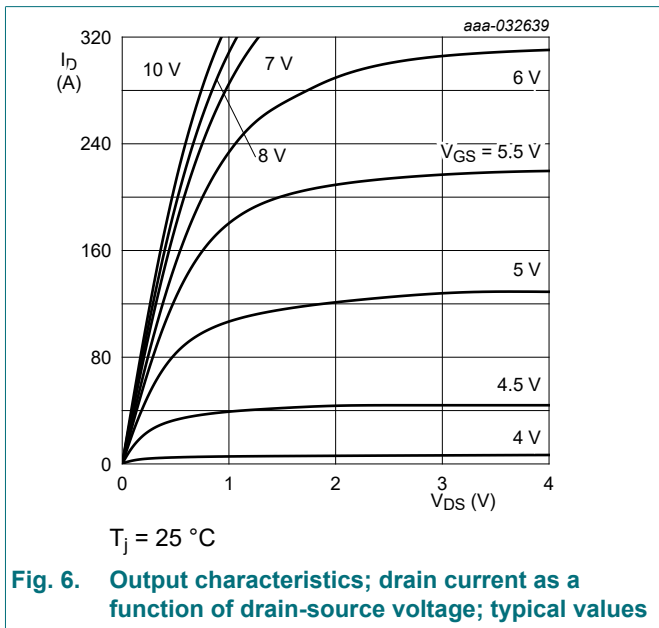
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	40.5	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}; \text{ Fig. 10}$	2.4	3	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 10}$	-	-	4.3	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 10}$	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.027	1	μA
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	0.7	10	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	82	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$	1.51	2.16	2.51	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105 \text{ }^\circ C; \text{ Fig. 12}$	2.14	3.32	3.99	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125 \text{ }^\circ C; \text{ Fig. 12}$	2.37	3.64	4.39	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C; \text{ Fig. 12}$	2.97	4.52	5.47	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.31	0.76	1.91	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 13}; \text{ Fig. 14}$	-	38	54	nC
Q_{GS}	gate-source charge		-	11	16	nC
Q_{GD}	gate-drain charge		-	7	14	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 15}$	-	2709	3793	pF	
C_{oss}	output capacitance		-	729	1021	pF	
C_{rss}	reverse transfer capacitance		-	127	279	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega; V_{GS} = 10\text{ V}; R_{G(ext)} = 5\text{ }\Omega$	-	10	-	ns	
t_r	rise time		-	8.5	-	ns	
$t_{d(off)}$	turn-off delay time		-	22	-	ns	
t_f	fall time		-	11	-	ns	
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 16}$	-	0.79	1	V	
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 17}$	-	30.1	-	ns	
Q_r	recovered charge		[1]	-	19.1	-	nC
S	softness factor		-	-	0.89	-	
		$I_S = 25\text{ A}; di_S/dt = -500\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 17}$	-	0.67	-		

[1] includes capacitive recovery



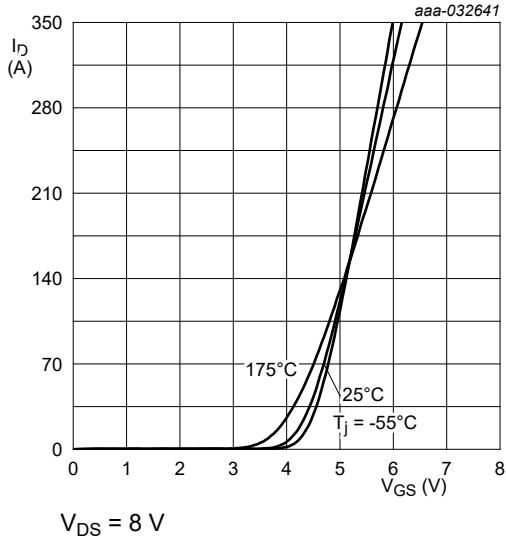


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

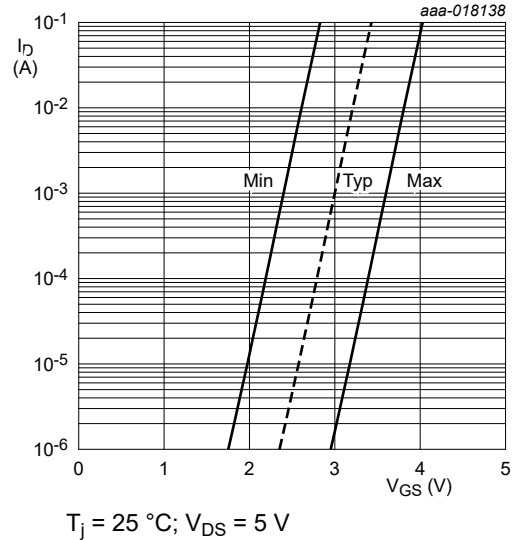


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

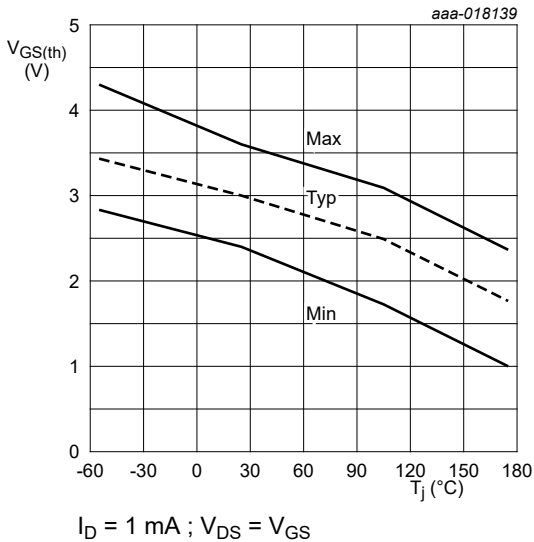


Fig. 10. Gate-source threshold voltage as a function of junction temperature

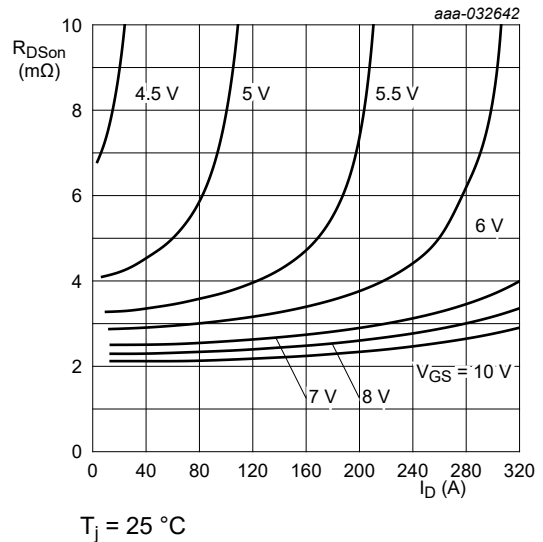
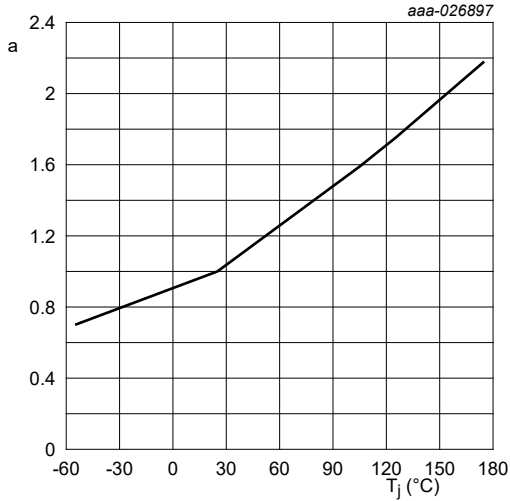
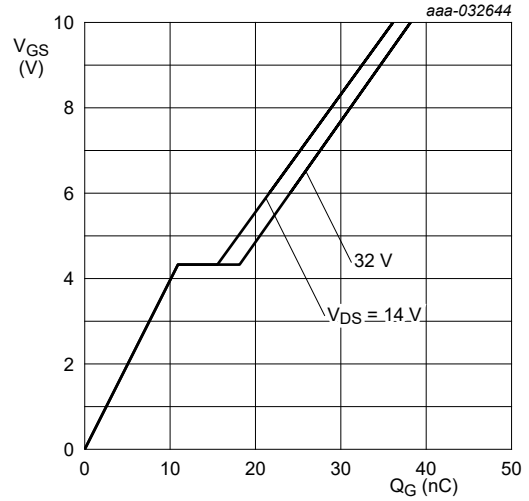


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

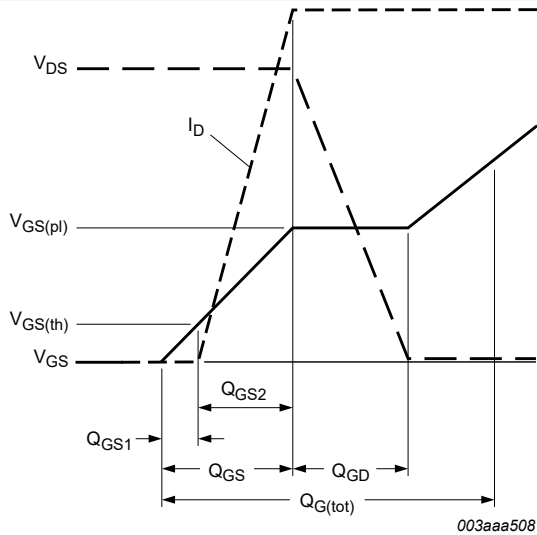
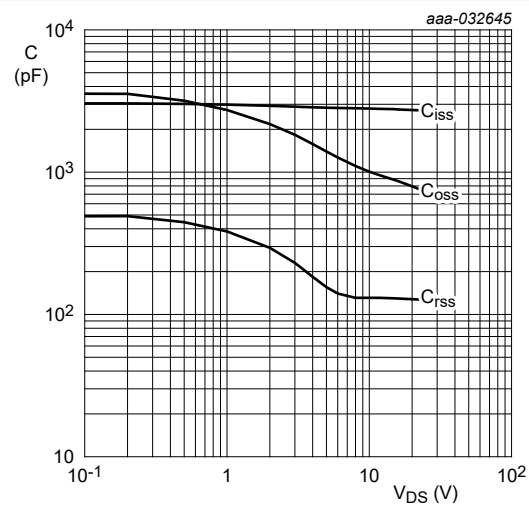


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

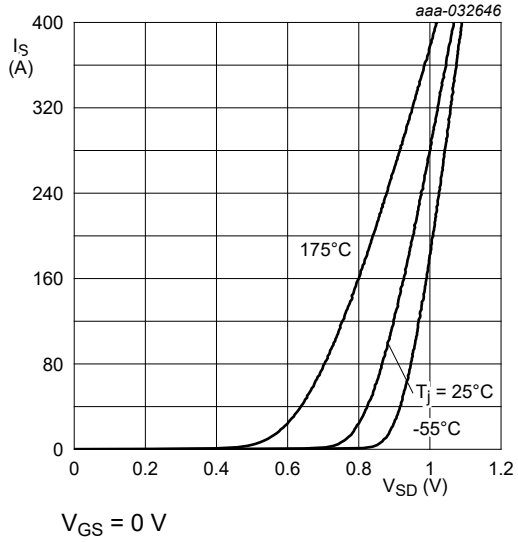


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

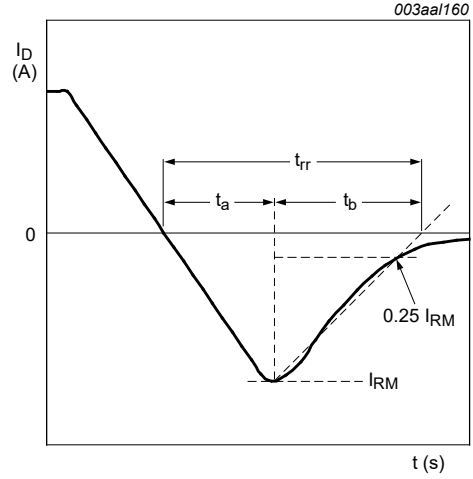


Fig. 17. Reverse recovery timing definition

11. Package outline

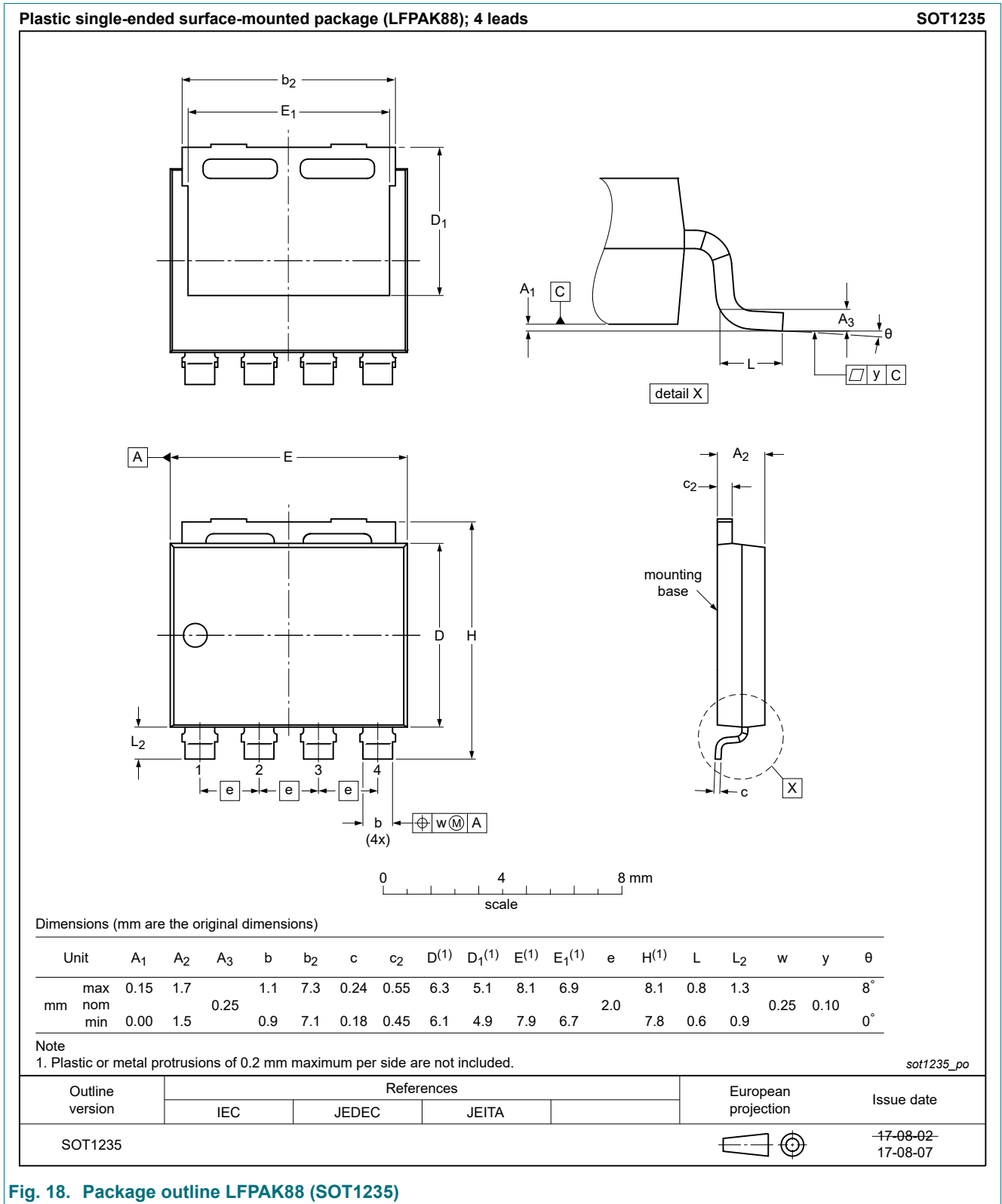


Fig. 18. Package outline LPAK88 (SOT1235)

12. Soldering

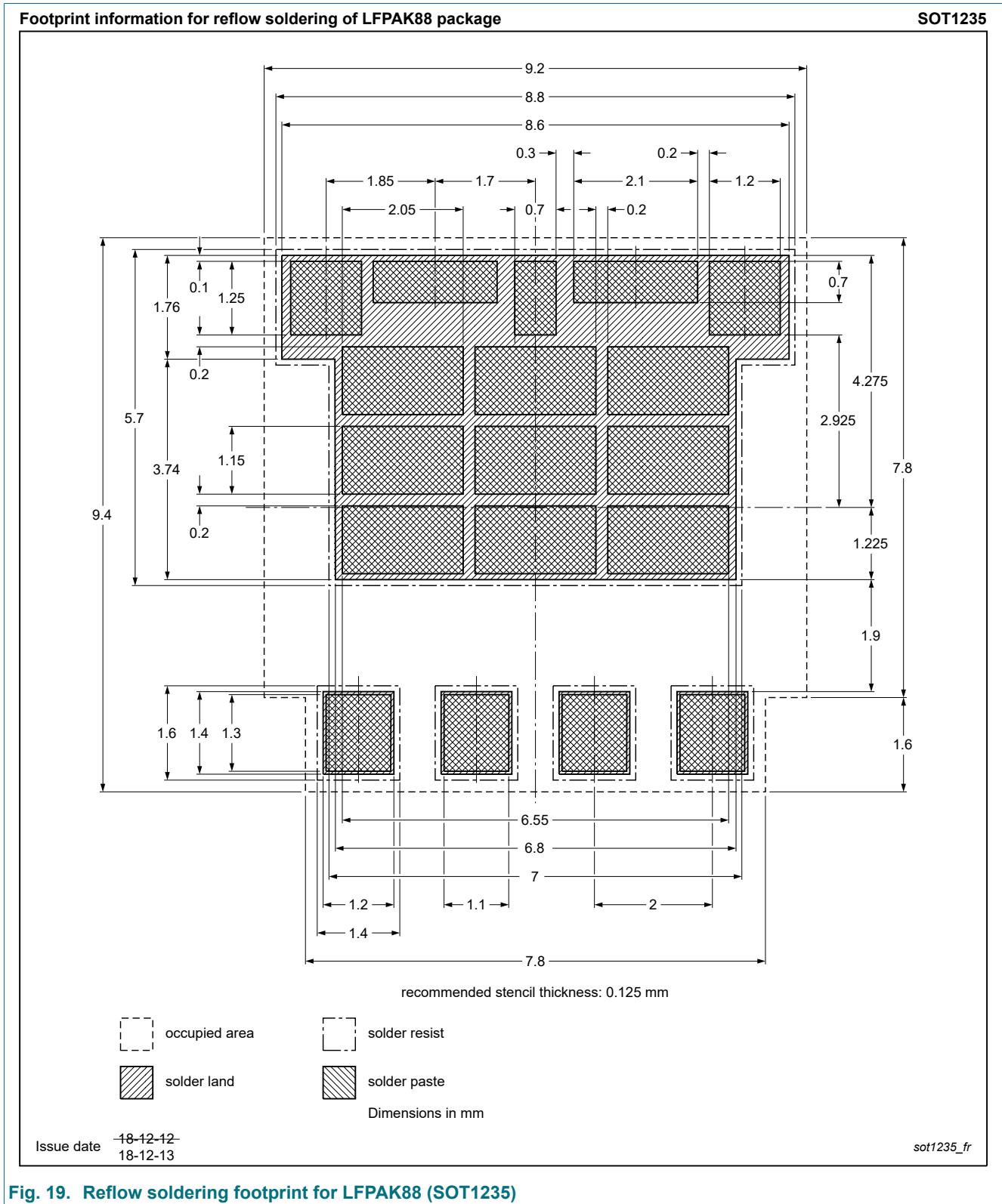


Fig. 19. Reflow soldering footprint for LPAK88 (SOT1235)

13. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 6 April 2021

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