



# BUK9D23-40E

40 V, N-channel Trench MOSFET

13 December 2017

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Extended temperature range  $T_j = 175\text{ °C}$
- Side wettable flanks for optical solder inspection
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

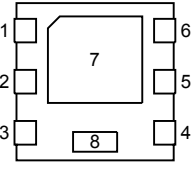
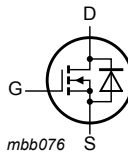
## 4. Quick reference data

Table 1. Quick reference data

| Symbol                        | Parameter                        | Conditions   | Min | Typ | Max | Unit       |
|-------------------------------|----------------------------------|--|-----|-----|-----|------------|
| $V_{DS}$                      | drain-source voltage             | $T_j = 25\text{ °C}$   | -   | -   | 40  | V          |
| $V_{GS}$                      | gate-source voltage              |  | -15 | -   | 15  | V          |
| $I_D$                         | drain current                    | $V_{GS} = 10\text{ V}; T_{sp} = 25\text{ °C}$                | -   | -   | 19  | A          |
| $P_{tot}$                     | total power dissipation          | $T_{sp} = 25\text{ °C}$                                      | -   | -   | 15  | W          |
| <b>Static characteristics</b> |                                  |  |     |     |     |            |
| $R_{DSon}$                    | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C}$ | -   | 18  | 23  | m $\Omega$ |

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline   | Graphic symbol  |
|-----|--------|-------------|--|---|
| 1   | D      | drain       |  <p>Transparent top view<br/><b>DFN2020MD-6 (SOT1220)</b></p> |  |
| 2   | D      | drain       |  |   |
| 3   | G      | gate        |  |   |
| 4   | S      | source      |  |   |
| 5   | D      | drain       |  |   |
| 6   | D      | drain       |  |   |
| 7   | D      | drain       |  |   |
| 8   | S      | source      |  |   |

## 6. Ordering information

Table 3. Ordering information

| Type number | Package     |   |         |
|-------------|-------------|---|---------|
|             | Name        | Description   | Version |
| BUK9D23-40E | DFN2020MD-6 | DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals | SOT1220 |

## 7. Marking

Table 4. Marking codes

| Type number | Marking code <sup>[1]</sup> |
|-------------|-----------------------------|
| BUK9D23-40E | %4B                         |

[1] % = placeholder for manufacturing site code

## 8. Limiting values

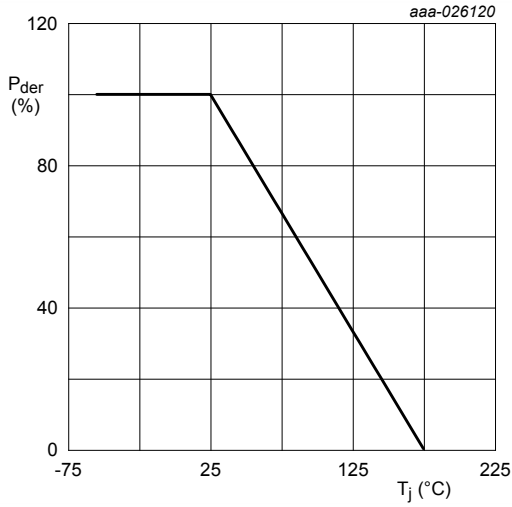
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions   |     | Min | Max  | Unit |
|-----------------------------|--|--|-----|-----|------|------|
| $V_{DS}$                    | drain-source voltage                         | $T_j = 25\text{ °C}$   |     | -   | 40   | V    |
| $V_{GS}$                    | gate-source voltage                          |  |     | -15 | 15   | V    |
| $I_D$                       | drain current                                | $V_{GS} = 10\text{ V}; T_{sp} = 25\text{ °C}$  |     | -   | 19   | A    |
|                             |  | $V_{GS} = 10\text{ V}; T_{sp} = 100\text{ °C}$   |     | -   | 12   | A    |
|                             |  | $V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$   | [1] | -   | 8    | A    |
| $I_{DM}$                    | peak drain current                           | $T_{sp} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$                |     | -   | 76   | A    |
| $P_{tot}$                   | total power dissipation                      | $T_{sp} = 25\text{ °C}$  |     | -   | 15   | W    |
|                             |  | $T_{amb} = 25\text{ °C}$   | [1] | -   | 2.3  | W    |
| $T_j$                       | junction temperature                         |  |     | -55 | 175  | °C   |
| $T_{amb}$                   | ambient temperature                          |  |     | -55 | 175  | °C   |
| $T_{stg}$                   | storage temperature                          |  |     | -65 | 175  | °C   |
| <b>Source-drain diode</b>   |  |  |     |     |      |      |
| $I_S$                       | source current                               | $T_{sp} = 25\text{ °C}$  |     | -   | 15   | A    |
|                             |  | $T_{amb} = 25\text{ °C}$   | [1] | -   | 2.3  | A    |
| $I_{SM}$                    | peak source current                          | single pulse; $t_p \leq 10\text{ }\mu\text{s}; T_{sp} = 25\text{ °C}$                  |     | -   | 62   | A    |
| <b>ESD maximum rating</b>   |  |  |     |     |      |      |
| $V_{ESD}$                   | electrostatic discharge voltage              | HBM  | [2] | -   | 500  | V    |
| <b>Avalanche ruggedness</b> |  |  |     |     |      |      |
| $E_{DS(AL)S}$               | non-repetitive drain-source avalanche energy | $T_{j(\text{init})} = 25\text{ °C}; I_D = 1.35\text{ A};$ DUT in avalanche (unclamped) |     | -   | 28.4 | mJ   |

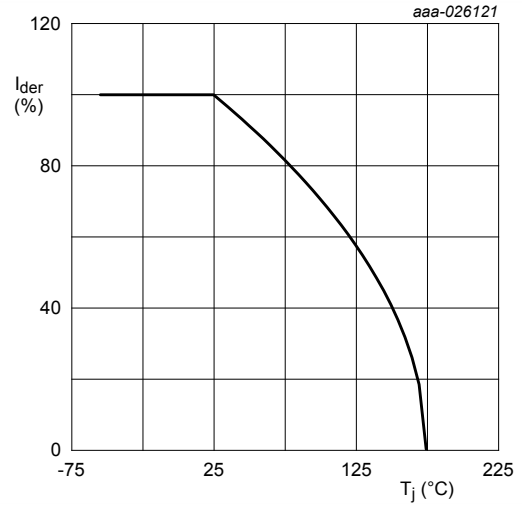
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .

[2] Measured between all pins.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature

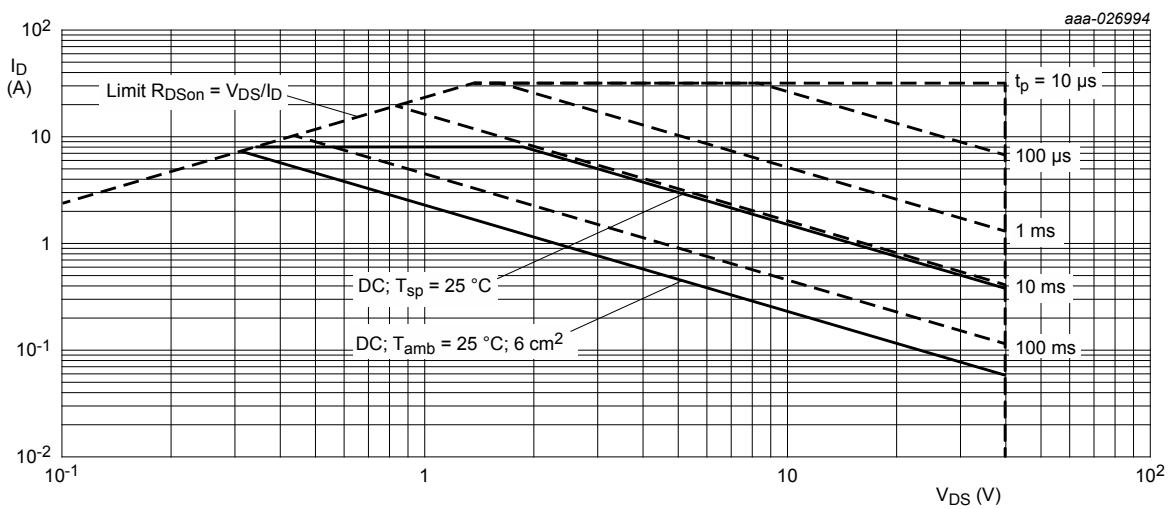


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

### 9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol         | Parameter  | Conditions  | Min | Typ | Max | Unit |
|----------------|--|-------------|-----|-----|-----|------|
| $R_{th(j-a)}$  | thermal resistance from junction to ambient      | in free air | [1] | 57  | 66  | K/W  |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point |             | -   | 6   | 10  | K/W  |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

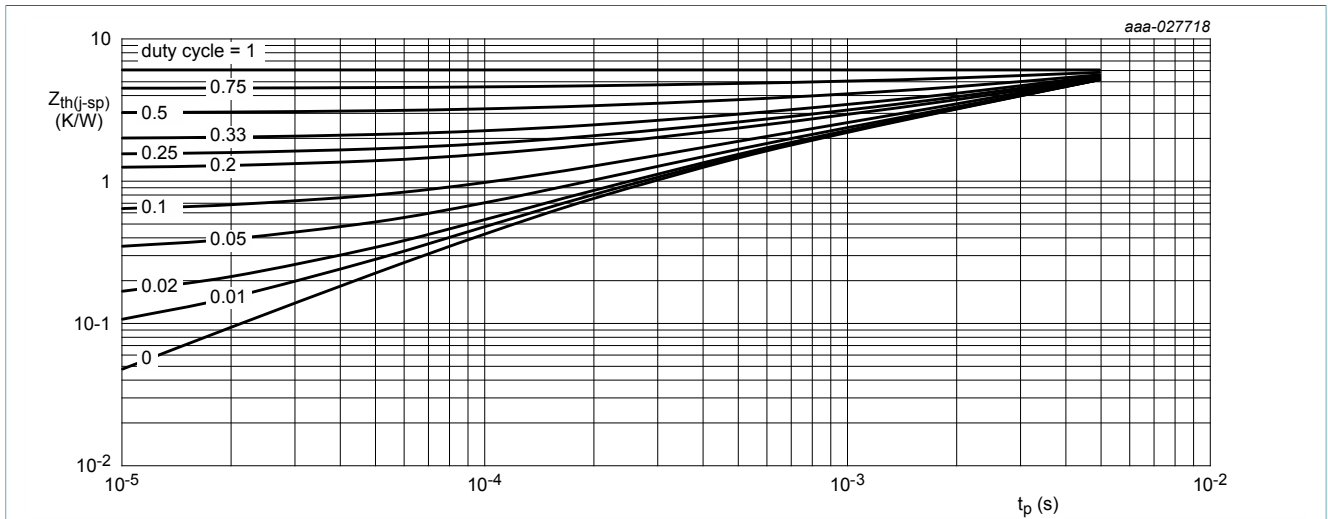
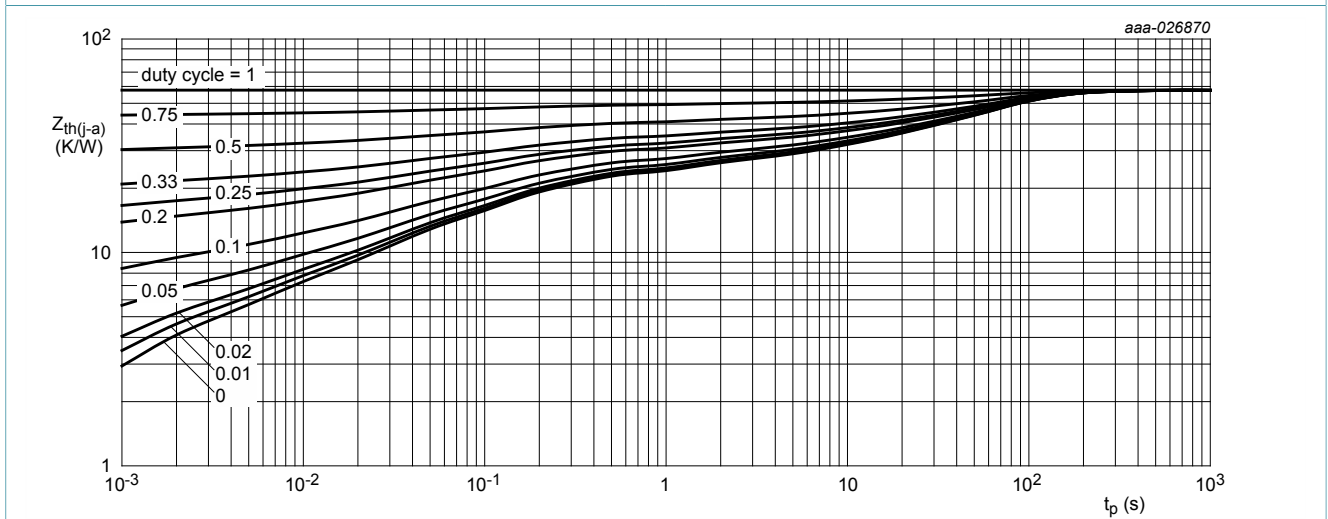


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

| Symbol                         | Parameter                        | Conditions   | Min | Typ  | Max  | Unit       |
|--------------------------------|----------------------------------|--|-----|------|------|------------|
| <b>Static characteristics</b>  |                                  |  |     |      |      |            |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage   | $I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$   | 40  | -    | -    | V          |
| $V_{GSth}$                     | gate-source threshold voltage    | $I_D = 250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$  | 1.4 | 1.7  | 2.1  | V          |
| $I_{DSS}$                      | drain leakage current            | $V_{DS} = 40 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$   | -   | -    | 1    | $\mu A$    |
|                                |                                  | $V_{DS} = 40 V$ ; $V_{GS} = 0 V$ ; $T_j = 175 \text{ }^\circ C$  | -   | -    | 500  | $\mu A$    |
| $I_{GSS}$                      | gate leakage current             | $V_{GS} = 15 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$   | -   | -    | 100  | nA         |
|                                |                                  | $V_{GS} = -15 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$  | -   | -    | -100 | nA         |
| $R_{DSon}$                     | drain-source on-state resistance | $V_{GS} = 10 V$ ; $I_D = 8 A$ ; $T_j = 25 \text{ }^\circ C$  | -   | 18   | 23   | m $\Omega$ |
|                                |                                  | $V_{GS} = 10 V$ ; $I_D = 8 A$ ; $T_j = 175 \text{ }^\circ C$   | -   | 33   | 43   | m $\Omega$ |
|                                |                                  | $V_{GS} = 4.5 V$ ; $I_D = 6.4 A$ ; $T_j = 25 \text{ }^\circ C$   | -   | 22   | 30   | m $\Omega$ |
| $g_{fs}$                       | forward transconductance         | $V_{DS} = 10 V$ ; $I_D = 8 A$ ; $T_j = 25 \text{ }^\circ C$  | -   | 39   | -    | S          |
| $R_G$                          | gate resistance                  | $f = 1 \text{ MHz}$  | -   | 1.8  | -    | $\Omega$   |
| <b>Dynamic characteristics</b> |                                  |  |     |      |      |            |
| $Q_{G(tot)}$                   | total gate charge                | $V_{DS} = 20 V$ ; $I_D = 8 A$ ; $V_{GS} = 10 V$ ;<br>$T_j = 25 \text{ }^\circ C$                             | -   | 11.5 | 17   | nC         |
| $Q_{GS}$                       | gate-source charge               |  | -   | 1.7  | -    | nC         |
| $Q_{GD}$                       | gate-drain charge                |  | -   | 2.1  | -    | nC         |
| $C_{iss}$                      | input capacitance                | $V_{DS} = 20 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ;<br>$T_j = 25 \text{ }^\circ C$                      | -   | 637  | -    | pF         |
| $C_{oss}$                      | output capacitance               |  | -   | 102  | -    | pF         |
| $C_{rss}$                      | reverse transfer capacitance     |  | -   | 52   | -    | pF         |
| $t_{d(on)}$                    | turn-on delay time               | $V_{DS} = 20 V$ ; $I_D = 8 A$ ; $V_{GS} = 10 V$ ;<br>$R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ C$   | -   | 2    | -    | ns         |
| $t_r$                          | rise time                        |  | -   | 6    | -    | ns         |
| $t_{d(off)}$                   | turn-off delay time              |  | -   | 12   | -    | ns         |
| $t_f$                          | fall time                        |  | -   | 4    | -    | ns         |
| <b>Source-drain diode</b>      |                                  |  |     |      |      |            |
| $V_{SD}$                       | source-drain voltage             | $I_S = 2.3 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$   | -   | 0.8  | 1.2  | V          |
| $t_{rr}$                       | reverse recovery time            | $I_S = 2.3 A$ ; $di_S/dt = -100 A/\mu s$ ;<br>$V_{GS} = 0 V$ ; $V_{DS} = 20 V$ ; $T_j = 25 \text{ }^\circ C$ | -   | 12.9 | -    | ns         |
| $Q_r$                          | recovered charge                 |  | -   | 5.3  | -    | nC         |

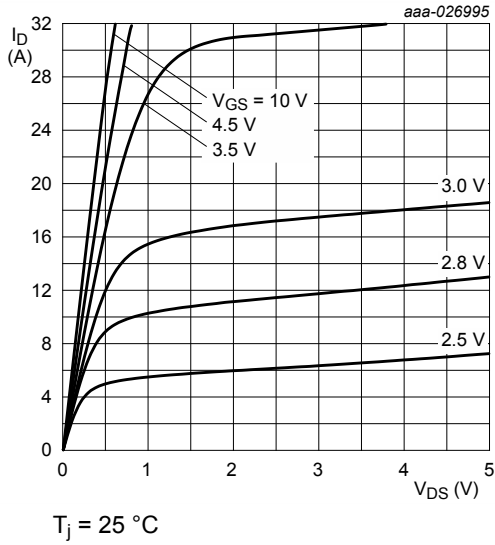


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

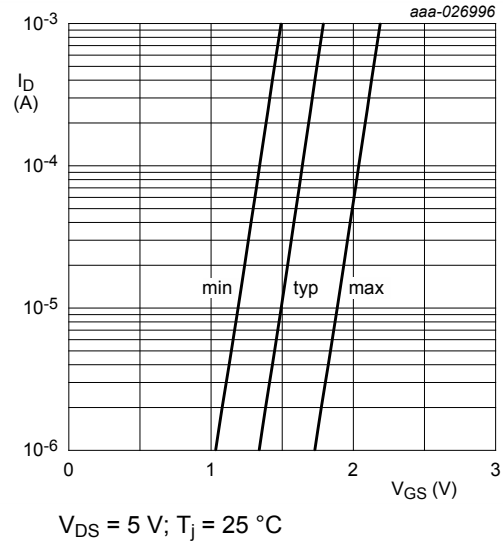


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

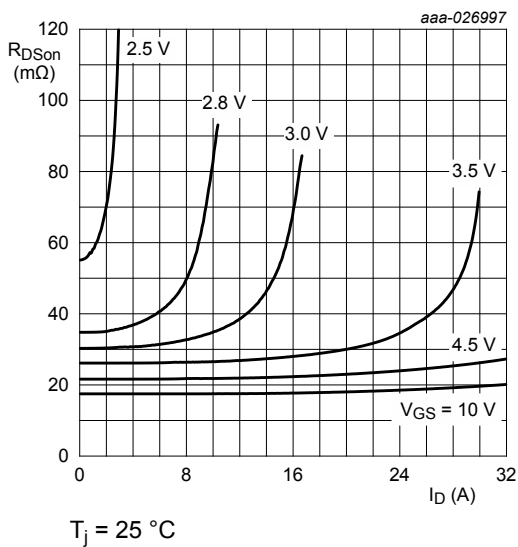


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

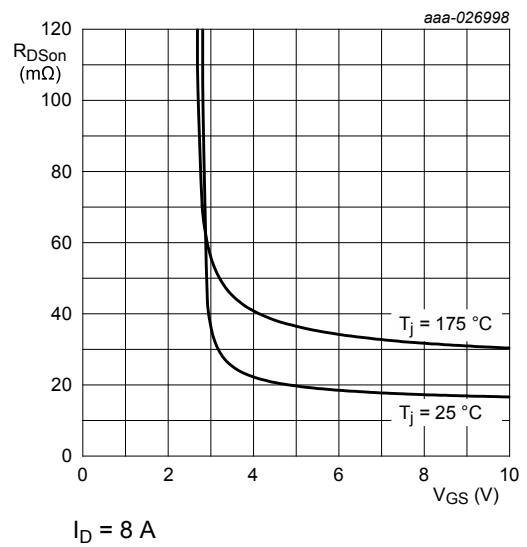
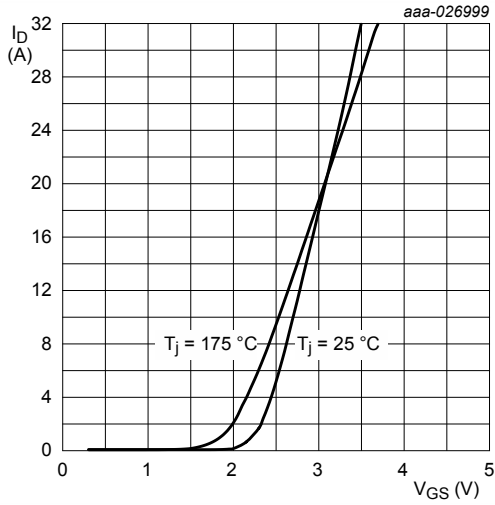
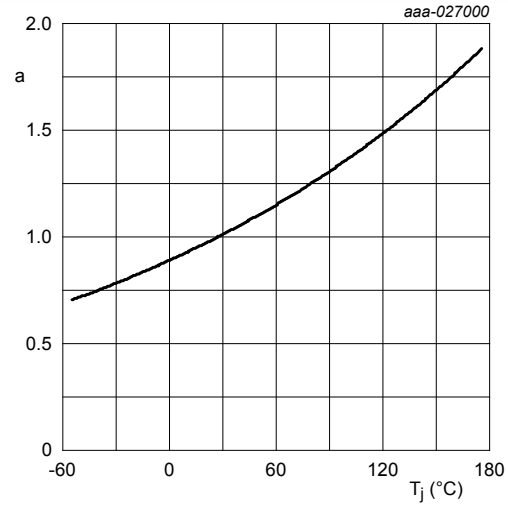


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

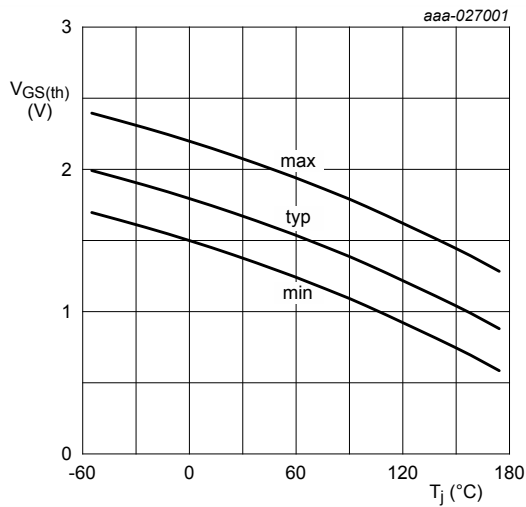


**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



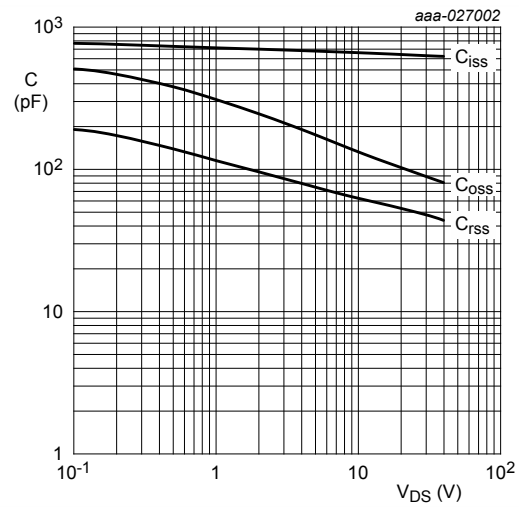
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**



$I_D = 250 \mu A; V_{DS} = V_{GS}$

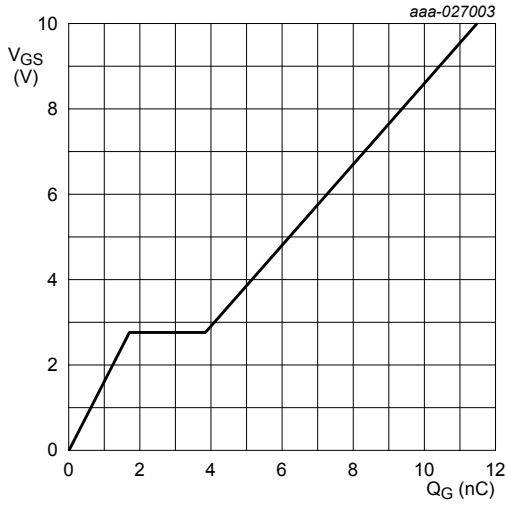
**Fig. 12. Gate-source threshold voltage as a function of junction temperature**



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**





$V_{DS} = 20 \text{ V}; I_D = 8 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

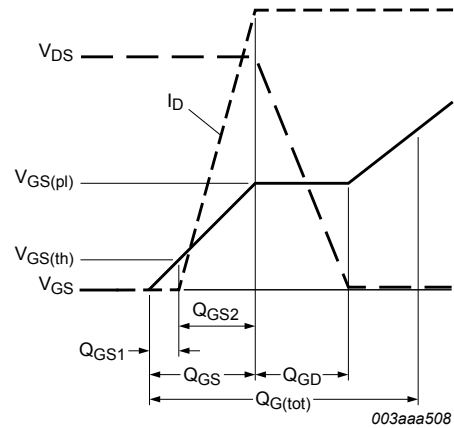
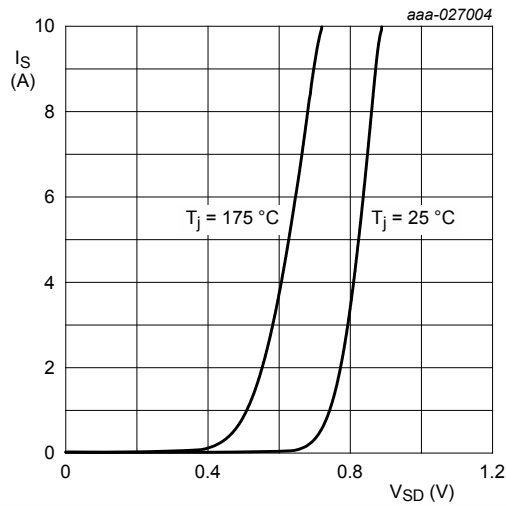


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

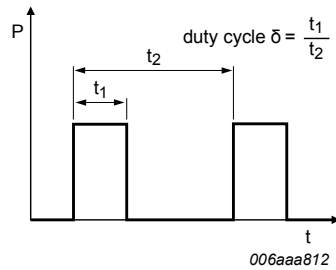


Fig. 17. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## 12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads;  
6 terminals; body 2 x 2 x 0.65 mm

SOT1220

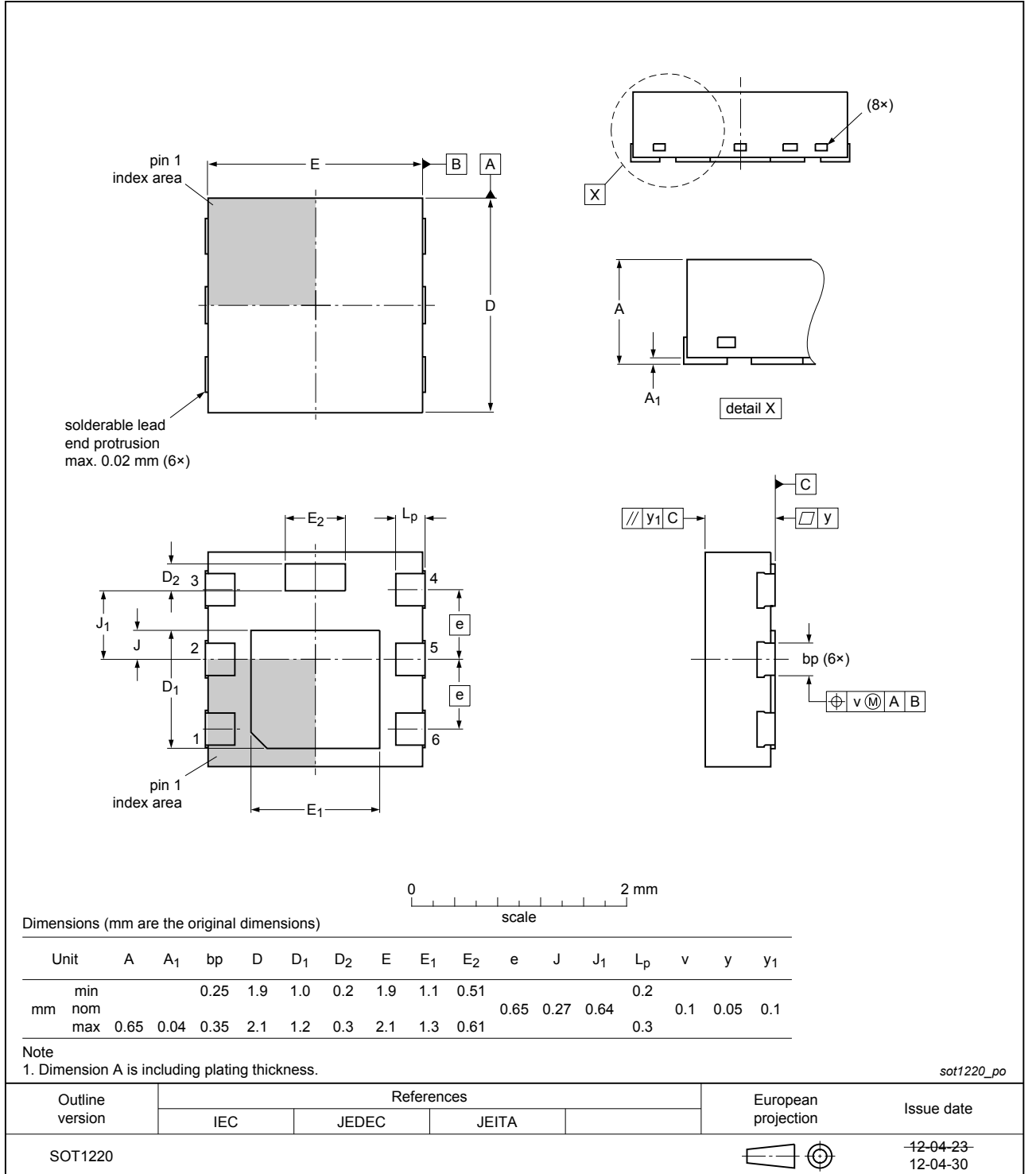


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

### 13. Soldering

Footprint information for reflow soldering of DFN2020MD-6 package

SOT1220

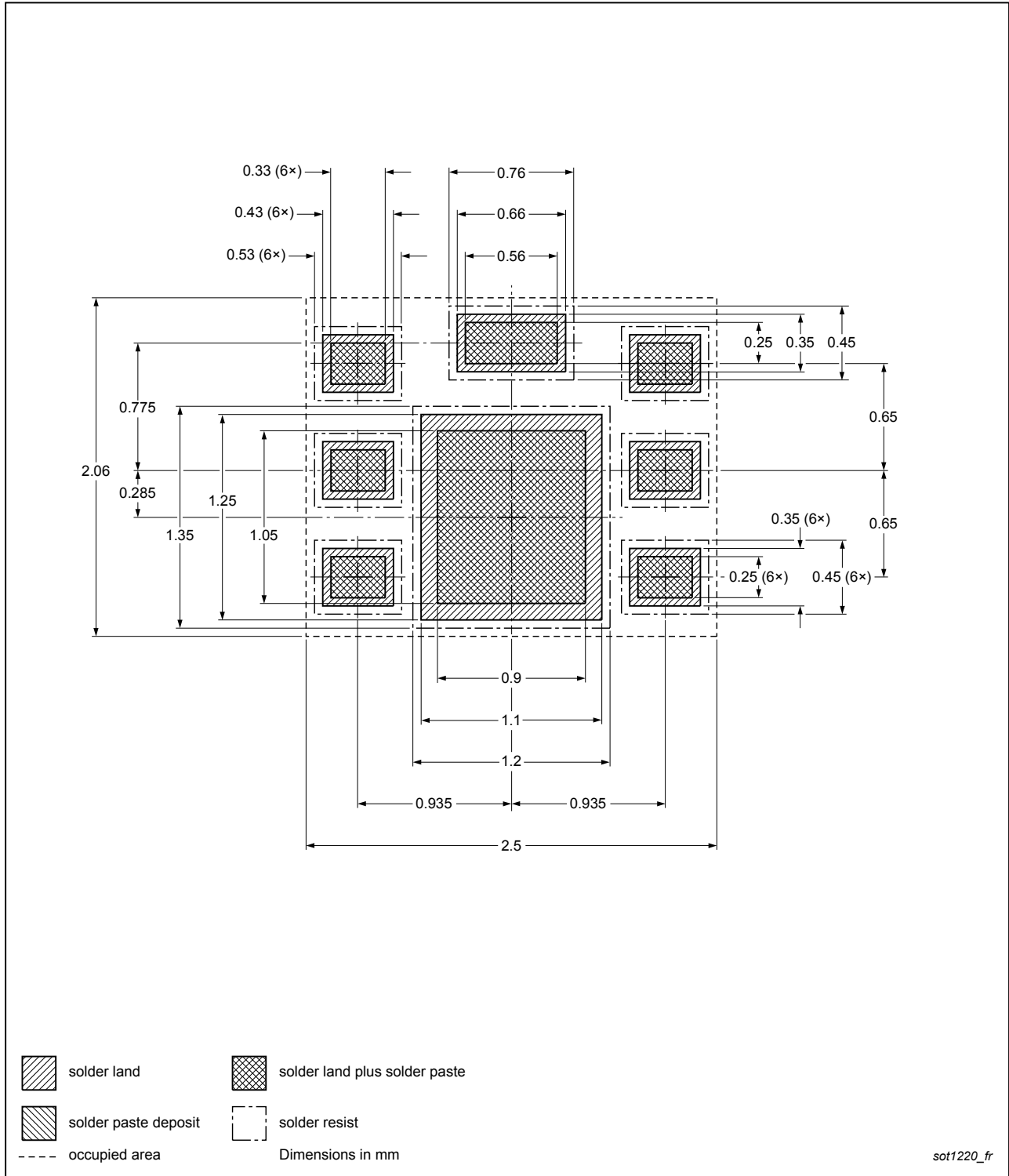


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

## 14. Revision history

Table 8. Revision history

| Data sheet ID   | Release date | Data sheet status  | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| BUK9D23-40E v.1 | 20171213     | Product data sheet | -             | -          |

## 15. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
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