



BUK9K17-60E

Dual N-channel 60 V, 17 mΩ logic level MOSFET

19 March 2014

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

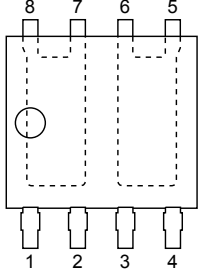
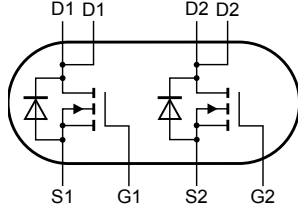
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|--|-----|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | - | 60 | V |
| I_D | drain current | $V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2 | [1] | - | 26 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ Fig. 1 | - | - | 53 | W |
| Static characteristics FET1 and FET2 | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 5\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C};$ Fig. 11 | - | 14 | 17 | mΩ |
| Dynamic characteristics FET1 and FET2 | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 10\text{ A}; V_{DS} = 48\text{ V}; V_{GS} = 5\text{ V};$ $T_j = 25\text{ °C};$ Fig. 13 ; Fig. 14 | - | 5.7 | - | nC |

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|---|---|
| 1 | S1 | source1 |  <p>LFPAK56D (SOT1205)</p> |  <p>mbk725</p> |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | |
| 6 | D2 | drain2 | | |
| 7 | D1 | drain1 | | |
| 8 | D1 | drain1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|-------------|----------|--|---------|
| | Name | Description | |
| BUK9K17-60E | LFPAK56D | Plastic single ended surface mounted package (LFPAK56D); 8 leads | SOT1205 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| BUK9K17-60E | 91760E |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|--------|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$ | - | 60 | V |
| V_{DGR} | drain-gate voltage | $R_{GS} = 20\text{ k}\Omega$ | - | 60 | V |
| V_{GS} | gate-source voltage | $T_j \leq 175\text{ °C}$; DC | -10 | 10 | V |
| | | $T_j \leq 175\text{ °C}$; Pulsed | [1][2] | 15 | V |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | 53 | W |
| I_D | drain current | $T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2 | [3] | 26 | A |
| | | $T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2 | - | 26 | A |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|--|--|------------------------|-----|-----|------|
| I_{DM} | peak drain current | $T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3 | | - | 148 | A |
| T_{stg} | storage temperature | | | -55 | 175 | °C |
| T_j | junction temperature | | | -55 | 175 | °C |
| Source-drain diode FET1 and FET2 | | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | [3] | - | 26 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$ | | - | 148 | A |
| Avalanche Ruggedness FET1 and FET2 | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 26\text{ A}$; $V_{sup} \leq 60\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; Fig. 4 | [4][5] | - | 64 | mJ |

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS} .
- [3] Continuous current is limited by package.
- [4] Refer to application note AN10273 for further information
- [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

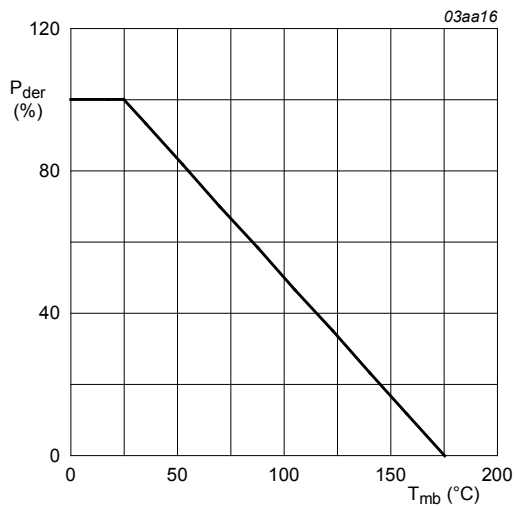


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

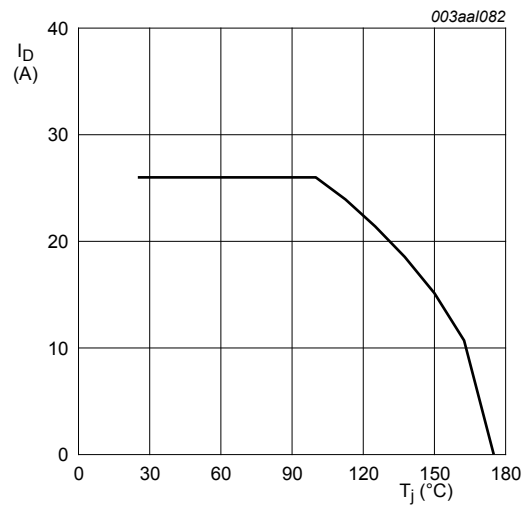


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5V$$

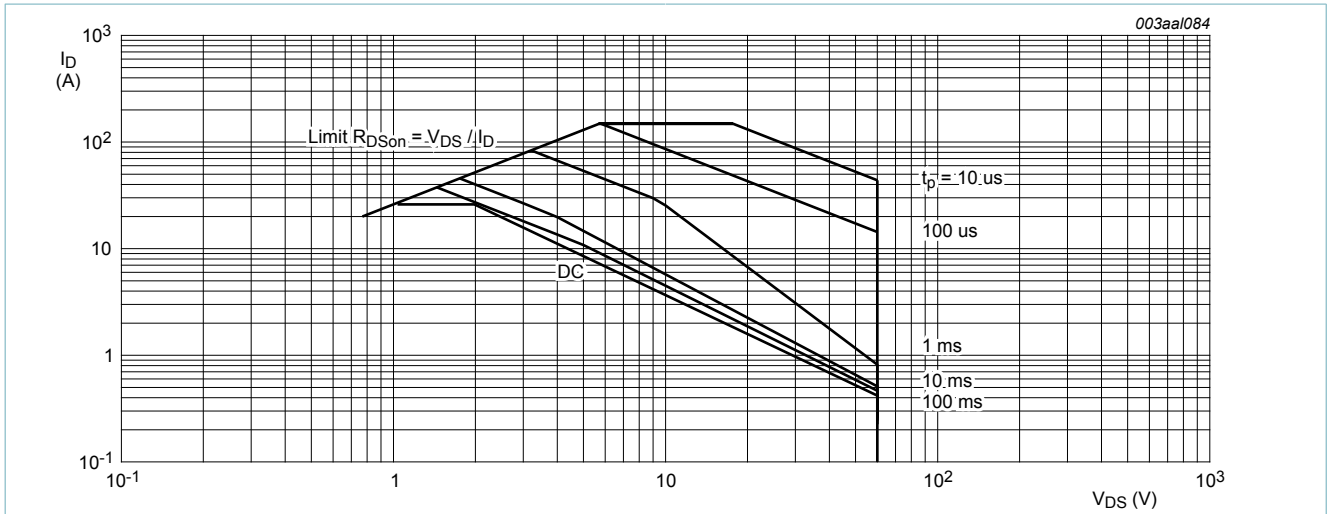


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

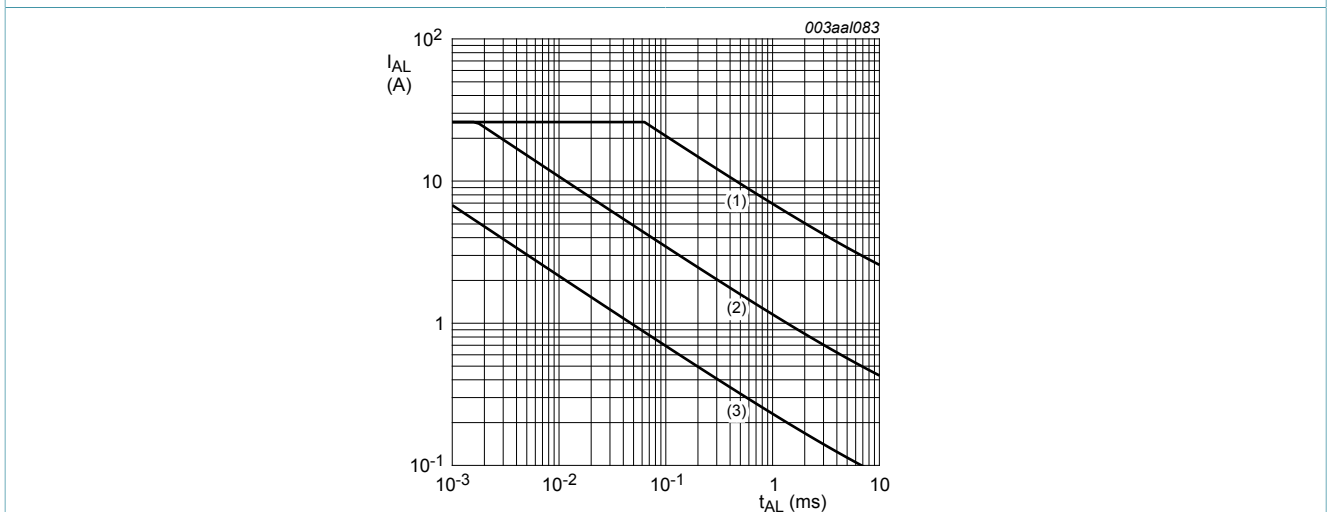


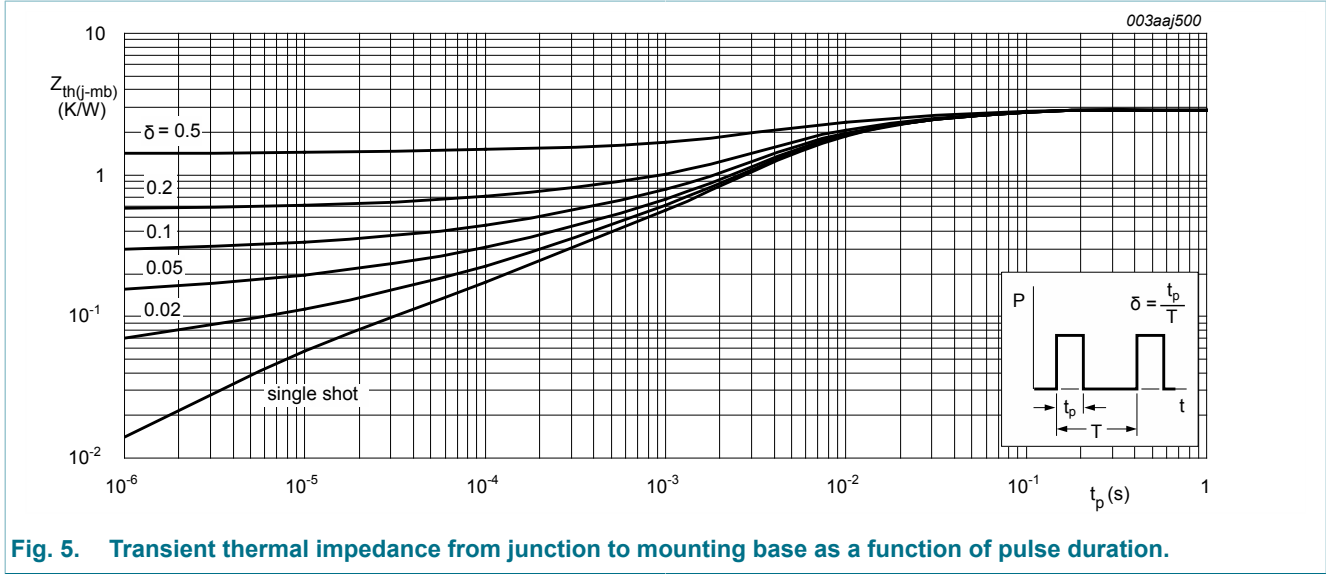
Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (init)} = 25^\circ C$; (2) $T_{j (init)} = 150^\circ C$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | - | 2.84 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Minimum footprint; mounted on a printed circuit board | - | 95 | - | K/W |

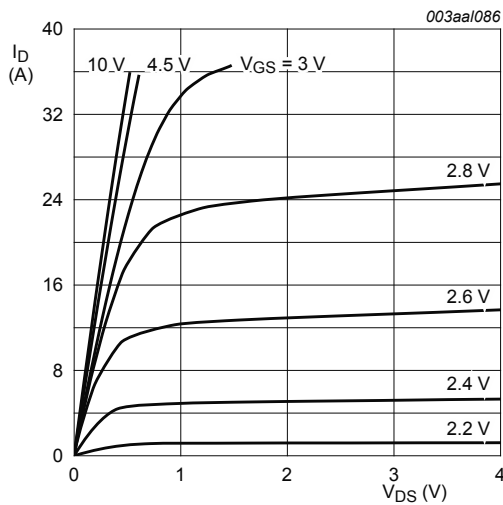


10. Characteristics

Table 7. Characteristics

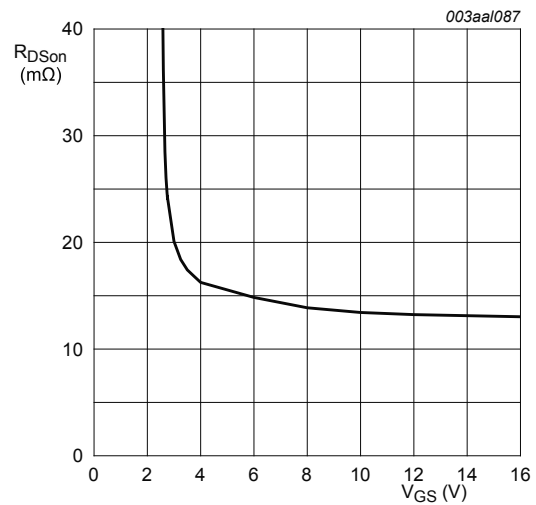
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|---|-----|------|------|---------|
| Static characteristics FET1 and FET2 | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 54 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 60 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 9; Fig. 10 | 1.4 | 1.7 | 2.1 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 9; Fig. 10 | 0.5 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 9; Fig. 10 | - | - | 2.45 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 1 | μA |
| | | $V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| | | $V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 5 V; I_D = 10 A; T_j = 25 \text{ }^\circ C;$ Fig. 11 | - | 14 | 17 | mΩ |
| | | $V_{GS} = 5 V; I_D = 10 A; T_j = 175 \text{ }^\circ C;$ Fig. 11; Fig. 12 | - | 31.6 | 38.4 | mΩ |
| | | $V_{GS} = 10 V; I_D = 10 A; T_j = 25 \text{ }^\circ C;$ Fig. 11 | - | 12.4 | 15.6 | mΩ |
| Dynamic characteristics FET1 and FET2 | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 10 A; V_{DS} = 48 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14 | - | 16.5 | - | nC |
| Q_{GS} | gate-source charge | | - | 3.3 | - | nC |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|------------------------------|---|-----|------|------|------|
| Q_{GD} | gate-drain charge | | - | 5.7 | - | nC |
| C_{iss} | input capacitance | $V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15 | - | 1667 | 2223 | pF |
| C_{oss} | output capacitance | | - | 160 | 193 | pF |
| C_{rss} | reverse transfer capacitance | $V_{GS} = 0\text{ V}; V_{DS} = 48\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15 | - | 91 | 124 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 48\text{ V}; R_L = 5\text{ }^\Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\text{ }^\Omega; T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$ | - | 10.7 | - | ns |
| t_r | rise time | | - | 20 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 23 | - | ns |
| t_f | fall time | | - | 19.2 | - | ns |
| Source-drain diode FET1 and FET2 | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16 | - | 0.78 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ | - | 20.3 | - | ns |
| Q_r | recovered charge | $V_{DS} = 30\text{ V}; T_j = 25\text{ }^\circ\text{C}$ | - | 16.7 | - | nC |



$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }^\mu\text{s}$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

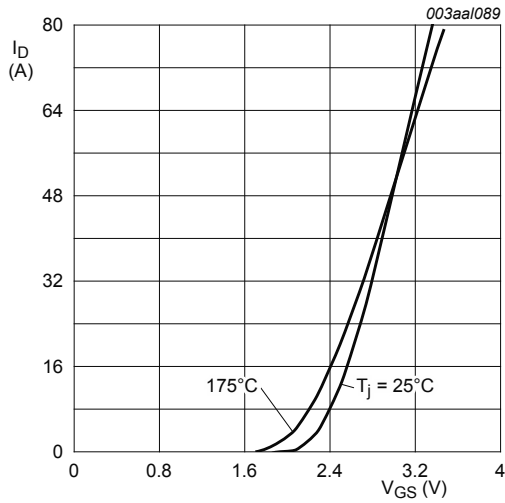


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10V$$

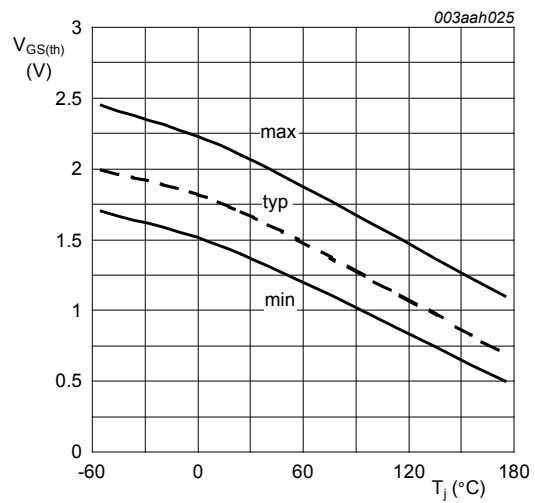


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

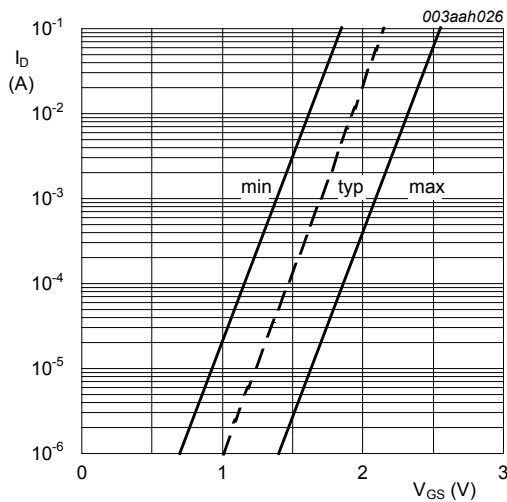
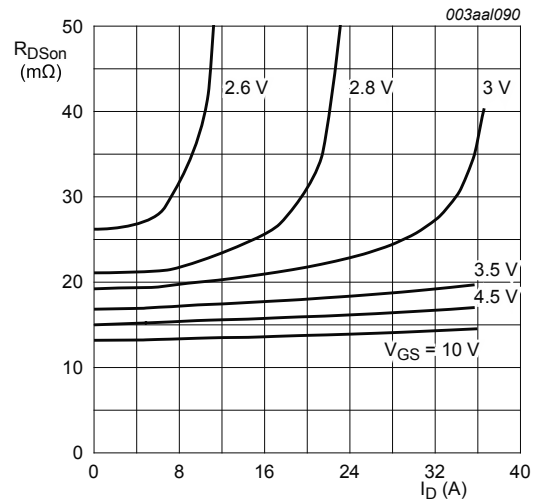


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5V$$



$$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

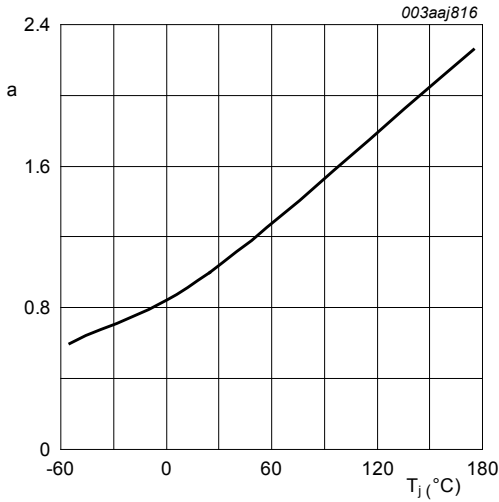


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$

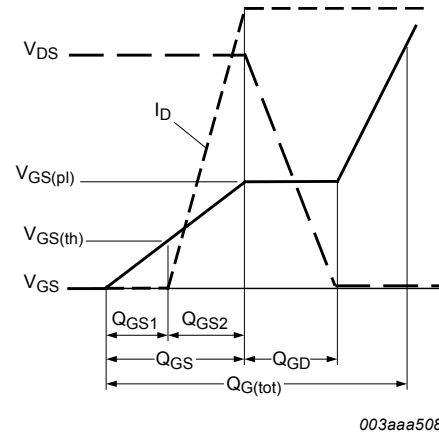


Fig. 13. Gate charge waveform definitions

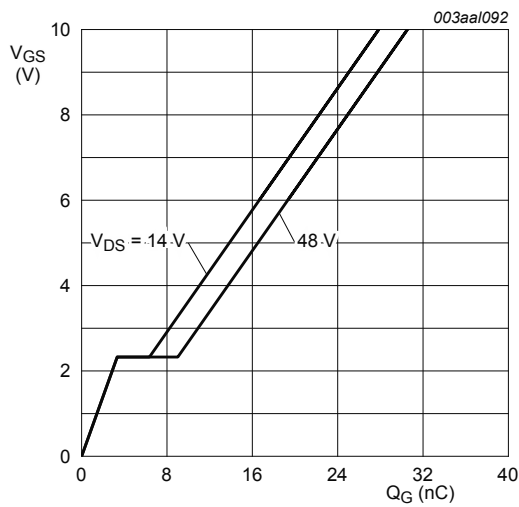


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ C; I_D = 10A$$

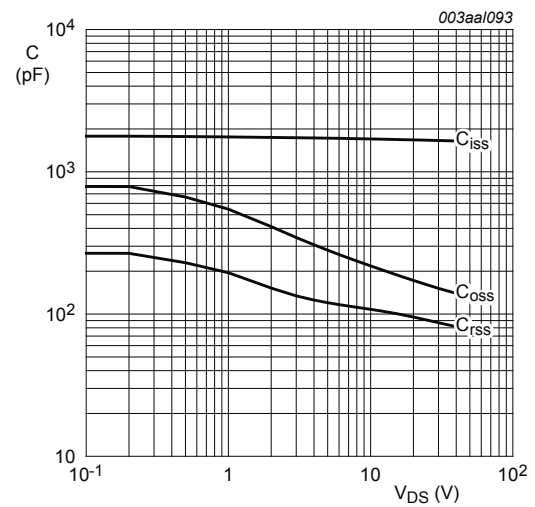


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

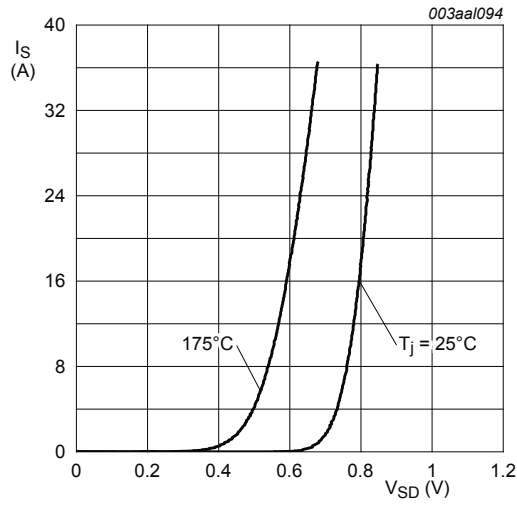


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

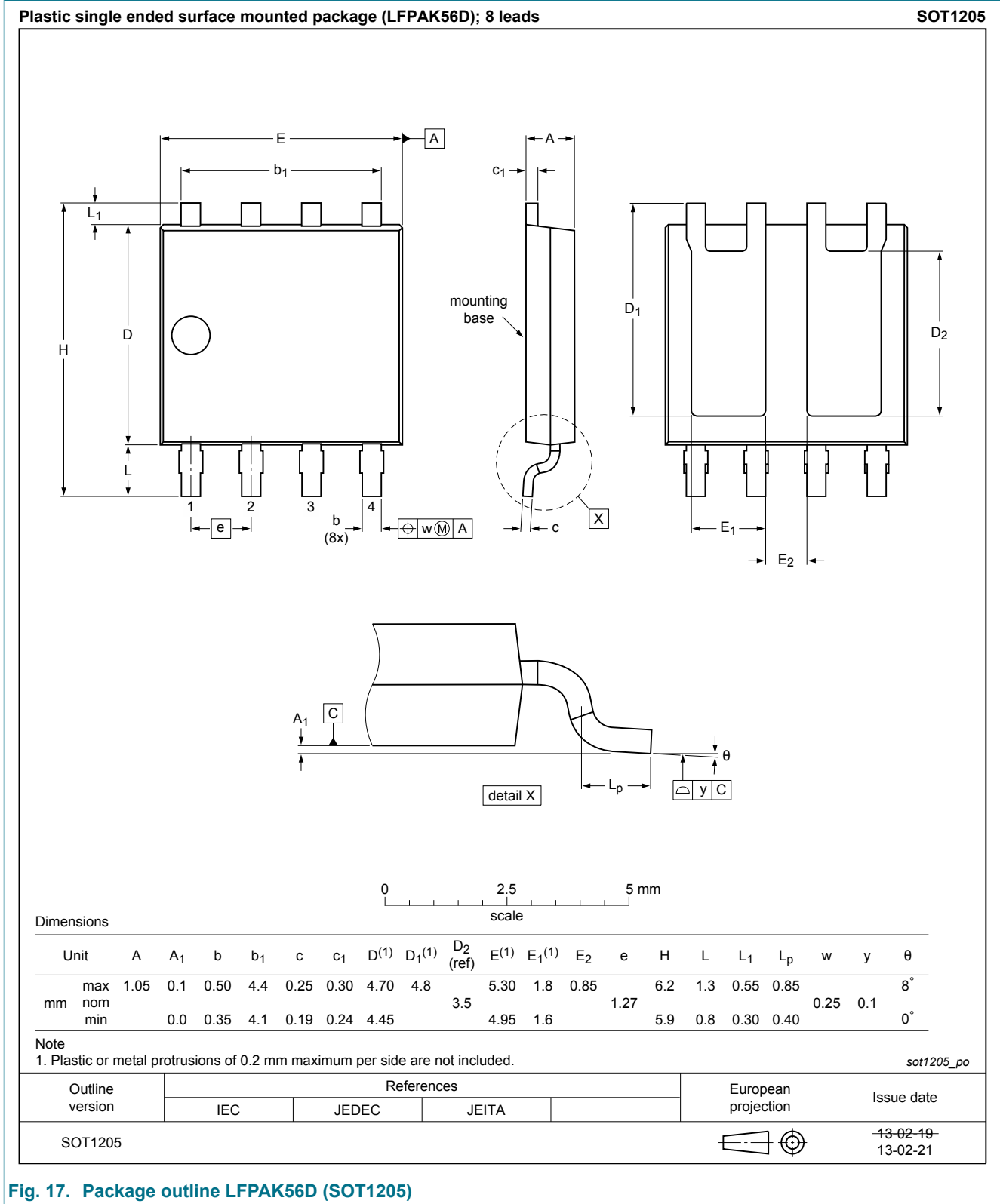


Fig. 17. Package outline LPAK56D (SOT1205)

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|--------------------------------|--------------------|---|
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