BUK9K25-40RA

Dual N-channel 40 V, 29 mOhm logic level MOSFET in LFPAK56D using Repetitive Avalanche technology

2 December 2020 Product data sheet

1. General description

Dual, logic level N-channel MOSFET in an LFPAK56D package, using Application Specific (ASFET) repetitive avalanche silicon technology. This product has been designed and qualified to AEC-Q101 for use in repetitive avalanche applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Repetitive Avalanche rated to 30 °C T_j rise:
  - Tested to 1 Bn avalanche events
- LFPAK copper clip package technology:
  - High robustness and reliability
  - Gull wing leads for high manufacturability and AOI

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Repetitive avalanche topologies
- Engine control
- Transmission control
- Actuator and auxiliary loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2		-	-	18.2	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	32	W
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; Fig. 14		-	24	29	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	I_D = 5 A; V_{DS} = 32 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 16; Fig. 17		-	2.4	-	nC

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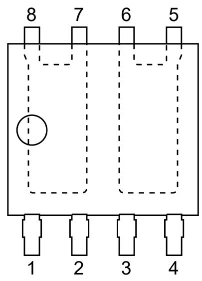
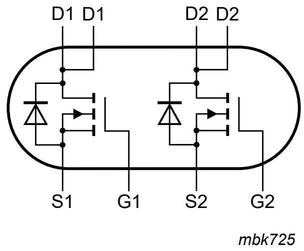
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D; Dual LFPAK (SOT1205)	
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K25-40RA	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K25-40RA	92540RA

8. Limiting values

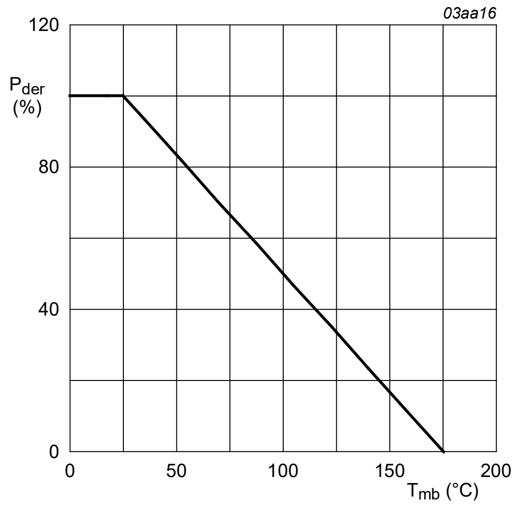
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage	Pulsed; T_j ≤ 175 °C	[1] [2]	-15	15	V
		DC; T_j ≤ 175 °C		-10	10	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	32	W
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2		-	18.2	A
		V_{GS} = 5 V; T_{mb} = 100 °C; Fig. 2		-	16.6	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	94	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I_S	source current	T_{mb} = 25 °C		-	18.2	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	94	A

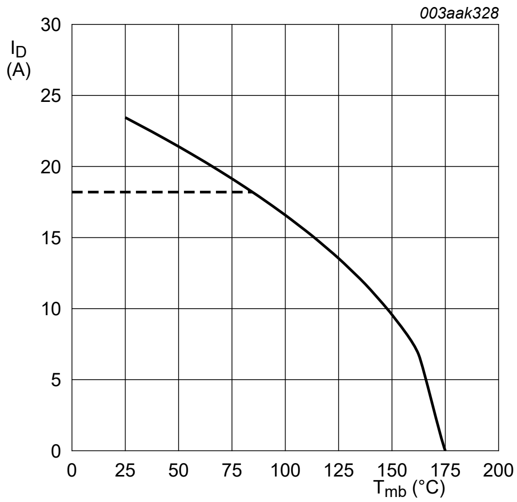
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	I_D = 0.73 A; V_{sup} ≤ 40 V; R_{GS} = 10 Ω; V_{GS} =10 V; $T_{j(rise)}$ ≤ 30 °C; unclamped; Fig. 4; Fig. 5; Fig. 6	[3] [4] [5]	-	19	mJ
Avalanche ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 18.2 A; V_{sup} ≤ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; Fig. 7	[6] [7]	-	15	mJ

[1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm.
[2] Significantly longer life times are achieved by lowering T_j and or V_{GS}.
[3] Repetitive avalanche rating is limited by maximum junction temperature of 175 °C and junction rise of 30 °C
[4] Refer to Fig. 5 for the limiting number of avalanche events
[5] Refer to Fig. 6 Rdson at Vgs=5V will increase as a function of repetitive avalanche cycles
[6] Refer to application note AN10273 for further information
[7] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



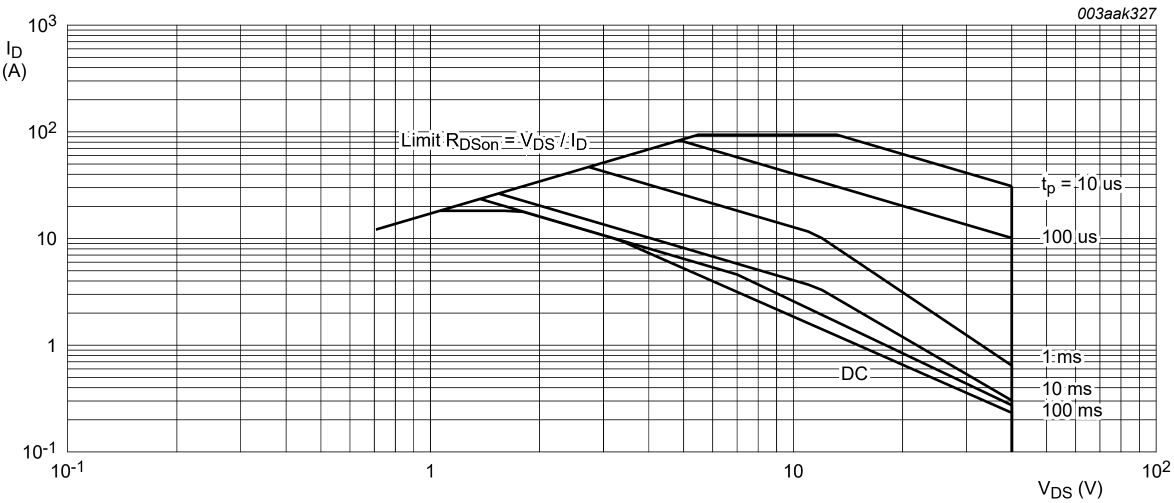
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



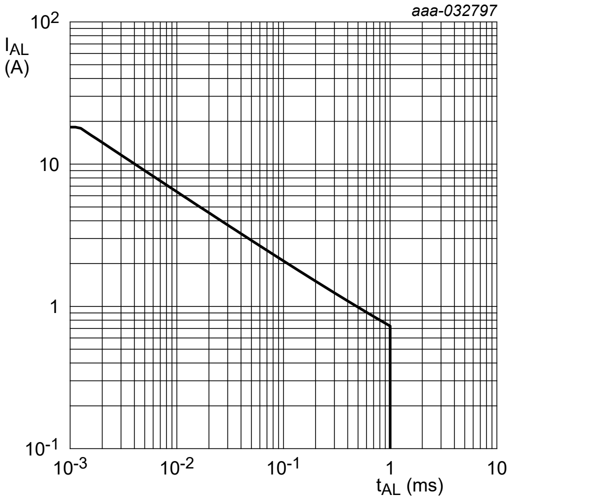
$$V_{GS} \geq 5V$$

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse

Fig. 3. Safe operating area; continuous and peak drain current as a function of drain-source voltage



T_j is limited to 175 °C and $T_{j(rise)}$ is limited to 30 °C

Fig. 4. Repetitive avalanche rating; avalanche current as a function of avalanche time

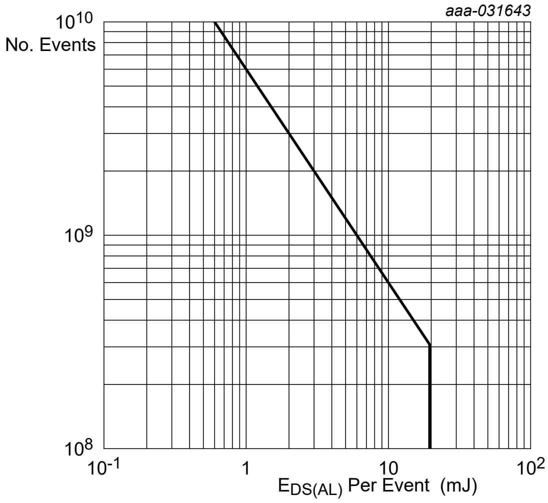


Fig. 5. Repetitive avalanche rating; maximum number of avalanche events as a function of avalanche energy

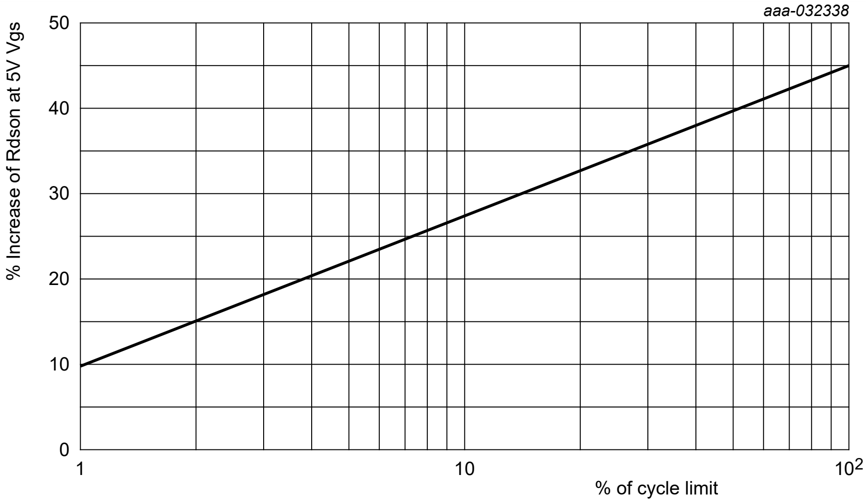
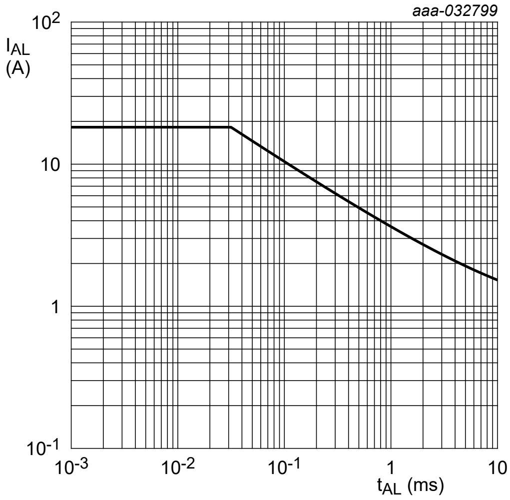


Fig. 6. Percentage Rdson at 5V increase as a function of avalanche cycles



$T_{j\ (init)}$ = 25 °C

Fig. 7. Single pulse avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 8		-	-	4.68	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board		-	95	-	K/W

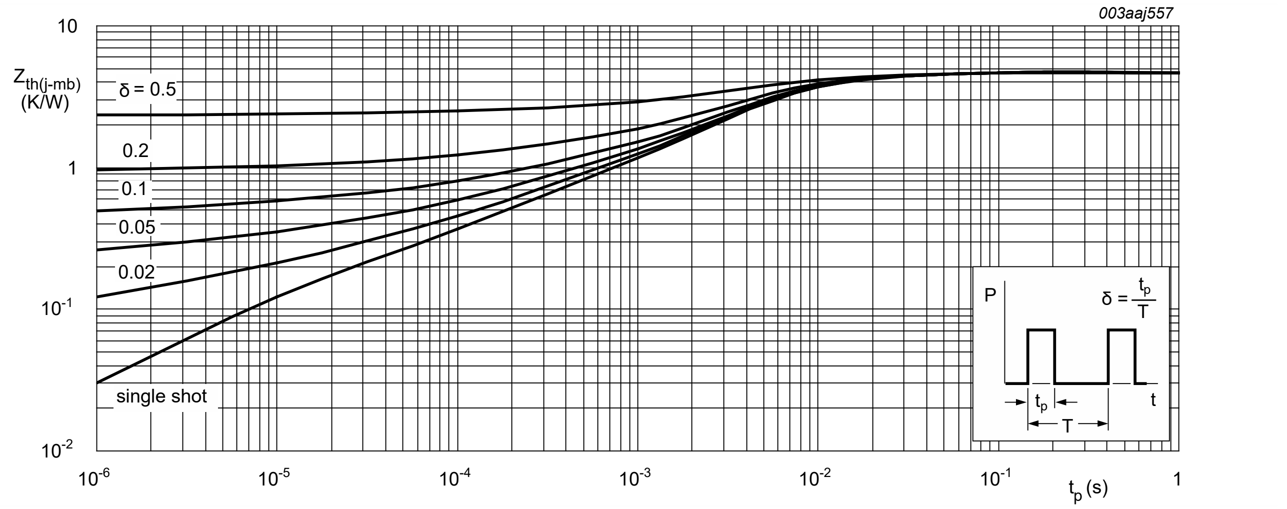


Fig. 8. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 12; Fig. 13		1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 12; Fig. 13		0.5	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 12; Fig. 13		-	-	2.45	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.02	1	µA
I_{GSS}	gate leakage current	V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; Fig. 14		-	24	29	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 175 °C; Fig. 14; Fig. 15		-	48.2	58	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 14		-	19	24	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 32 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 16; Fig. 17		-	6.3	-	nC
Q_{GS}	gate-source charge			-	1.4	-	nC
Q_{GD}	gate-drain charge			-	2.4	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 18		-	528	701	pF
C_{oss}	output capacitance			-	95	114	pF
C_{rss}	reverse transfer capacitance			-	56	76	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 32 V; R_L = 6.4 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	6.2	-	ns
t_r	rise time			-	9.2	-	ns
$t_{d(off)}$	turn-off delay time			-	10.8	-	ns
t_f	fall time			-	8.9	-	ns
Source-drain diode FET1 and FET2							
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 19		-	0.83	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C		-	15.9	-	ns
Q_r	recovered charge			-	7.6	-	nC

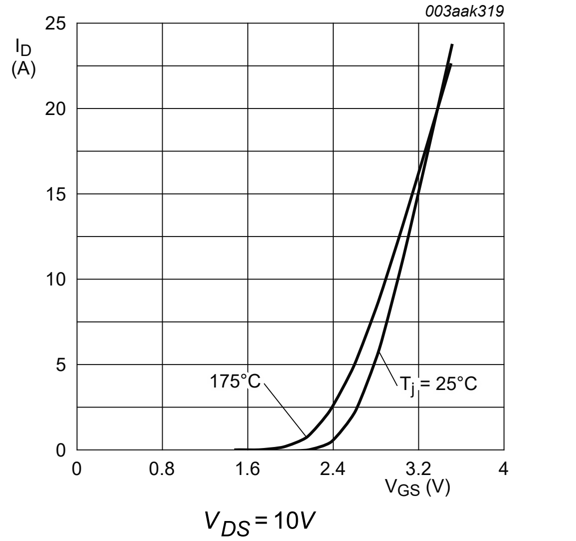


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

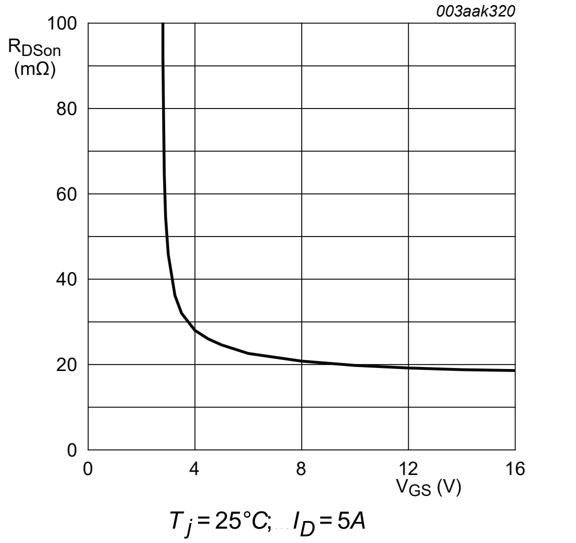
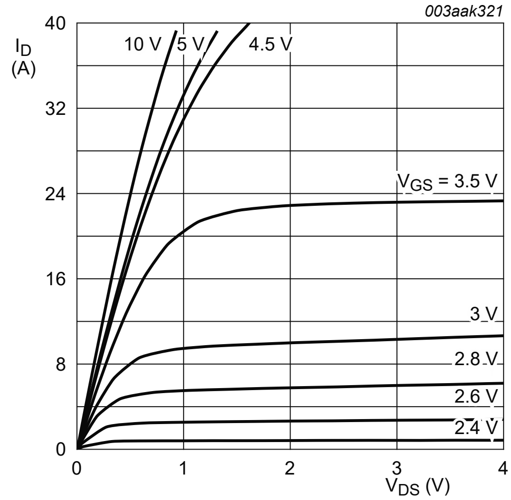
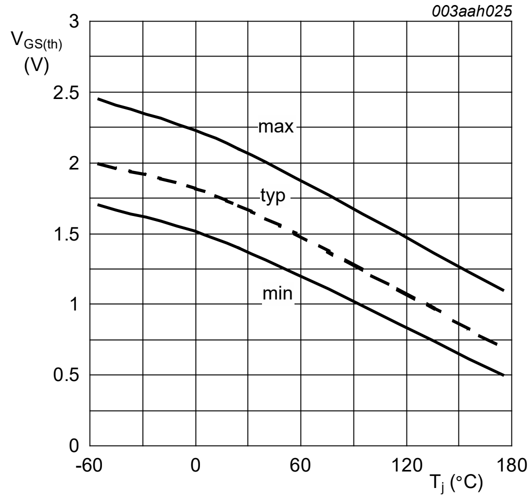


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



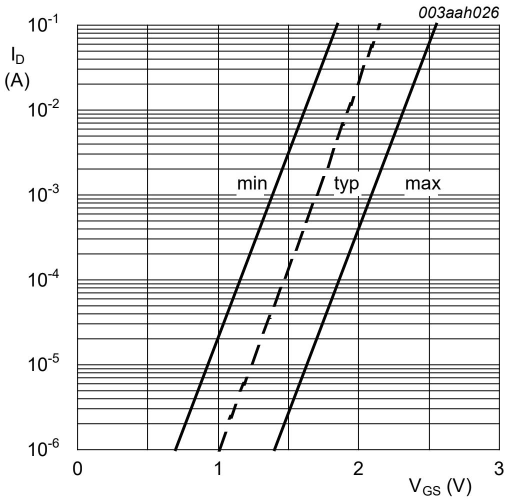
T_j = 25 °C; t_p = 300 μs

Fig. 11. Output characteristics; drain current as a function of drain-source voltage; typical values



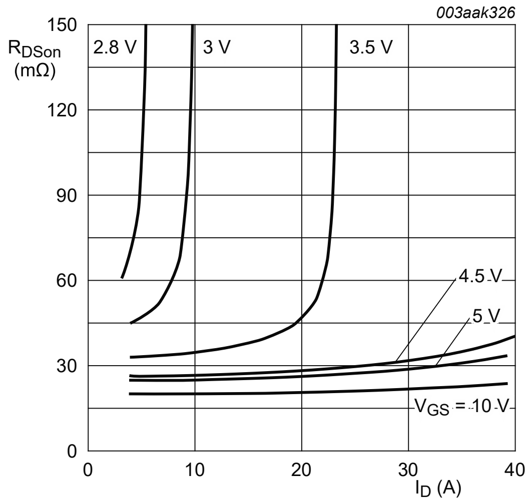
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



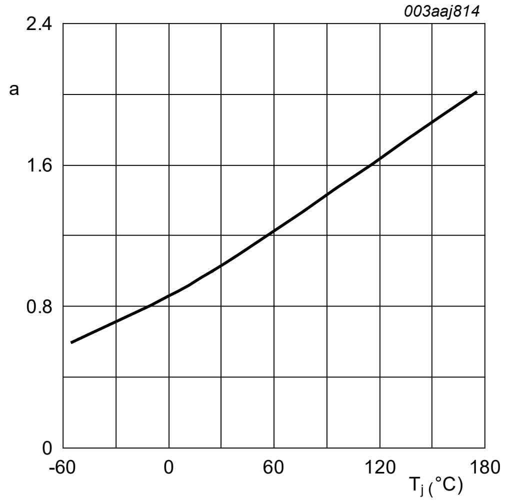
$T_j = 25°C$; $V_{DS} = 5V$

Fig. 13. Sub-threshold drain current as a function of gate-source voltage



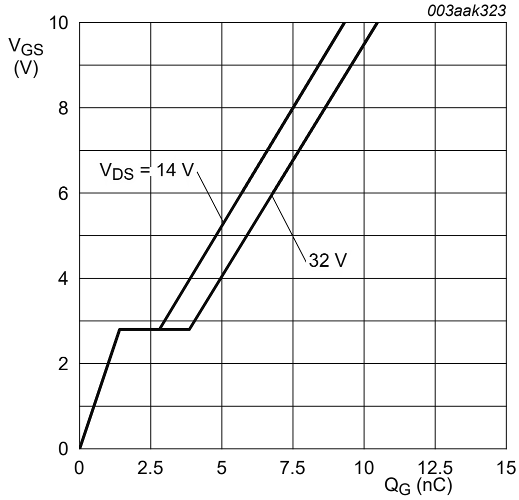
T_j = 25 °C; t_p = 300 μs

Fig. 14. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 15. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25°C$; $I_D = 5A$

Fig. 16. Gate-source voltage as a function of gate charge; typical values

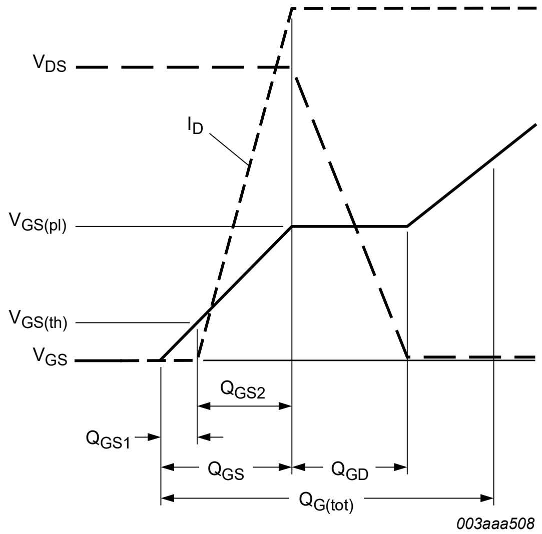
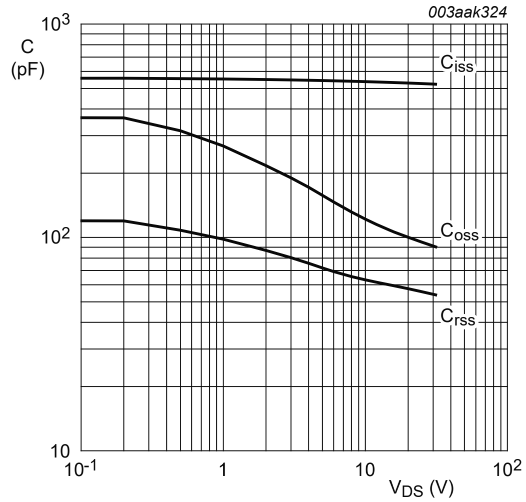


Fig. 17. Gate charge waveform definitions



$V_{GS} = 0V$; $f = 1MHz$

Fig. 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

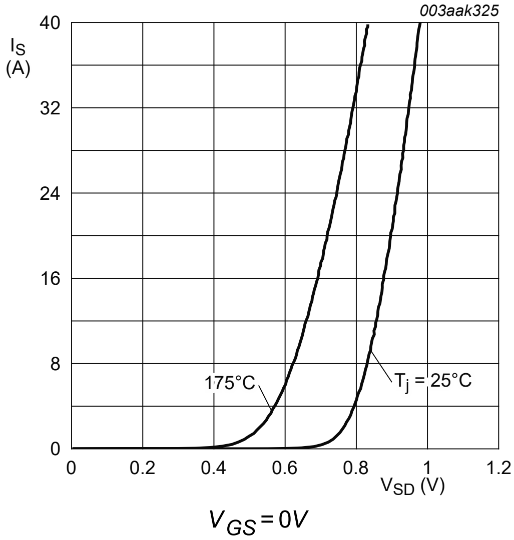
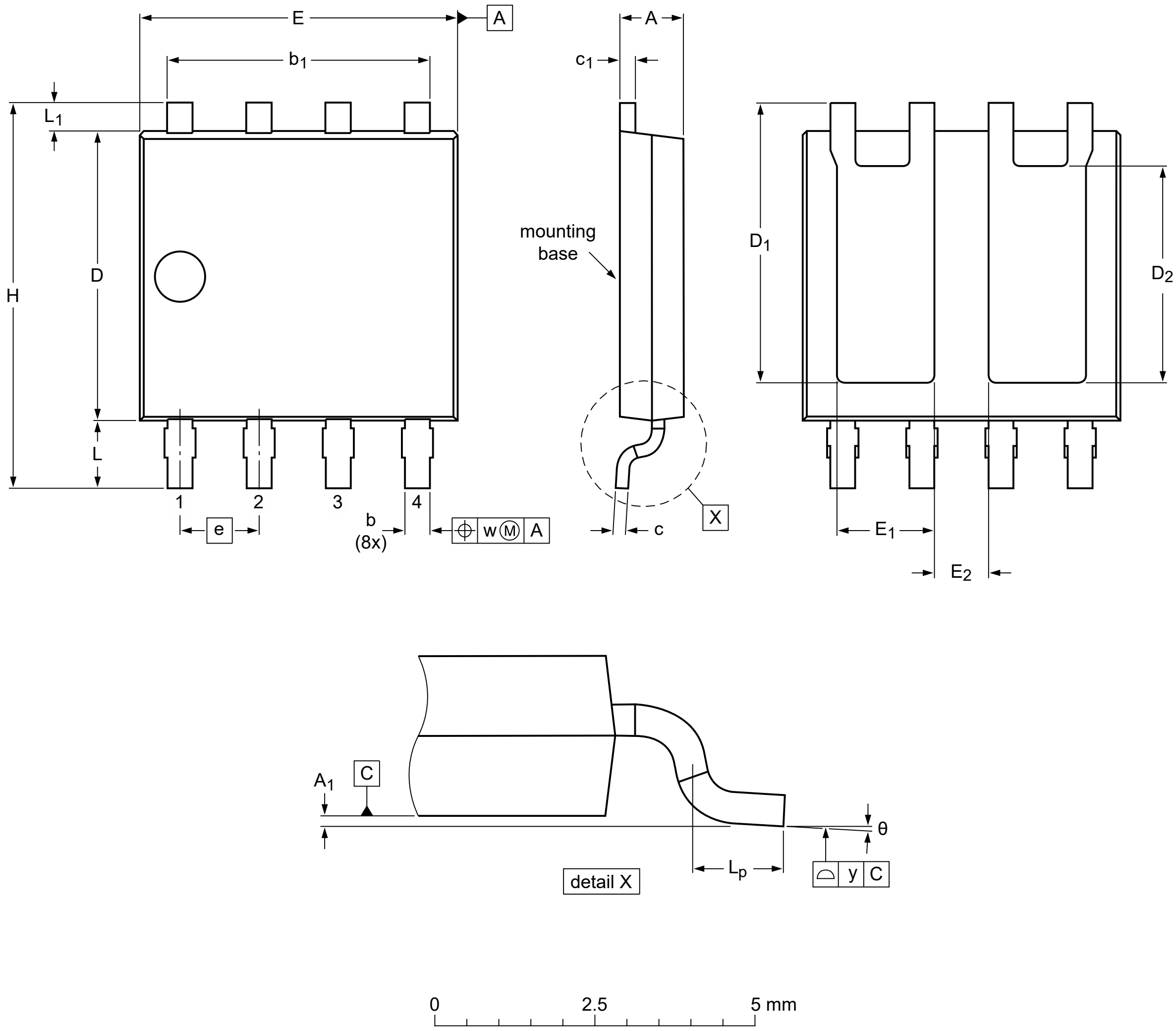


Fig. 19. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads **SOT1205**



Dimensions

Unit		A	A_1	b	b_1	c	c_1	$D^{(1)}$	$D_1^{(1)}$	D_2 (ref)	$E^{(1)}$	$E_1^{(1)}$	E_2	e	H	L	L_1	L_p	w	y	θ
mm	max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85			8°
	nom													1.27					0.25	0.1	
	min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						~~14-08-21~~ 14-10-28

Fig. 20. Package outline LFPAK56D; Dual LFPAK (SOT1205)

12. Soldering

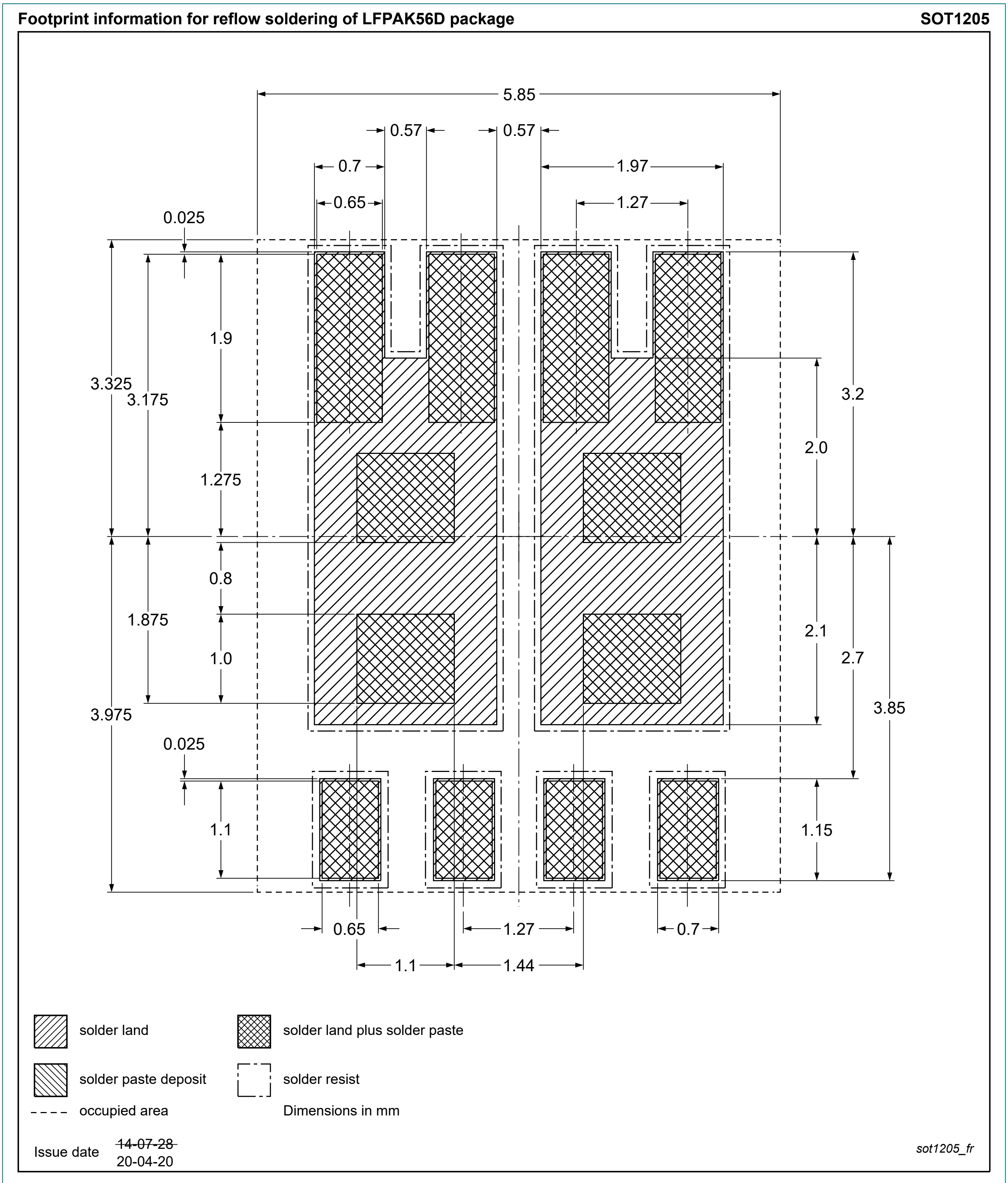


Fig. 21. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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