



# BUK9K45-100E

Dual N-channel TrenchMOS logic level FET

26 March 2013

Product data sheet

## 1. General description

Dual logic level N-channel MOSFET in a LFAK56D package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)} > 0.5 \text{ V @ } 175 \text{ °C}$

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

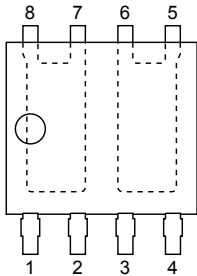
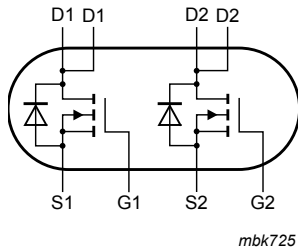
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25 \text{ °C}; T_j \leq 175 \text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C}; \text{Fig. 1}$	-	-	21	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ °C}; \text{Fig. 2}$	-	-	53	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}; \text{Fig. 12}$	-	38.3	45	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ °C}; \text{Fig. 15}; \text{Fig. 14}$	-	7.3	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9K45-100E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K45-100E	94510E

## 8. Limiting values

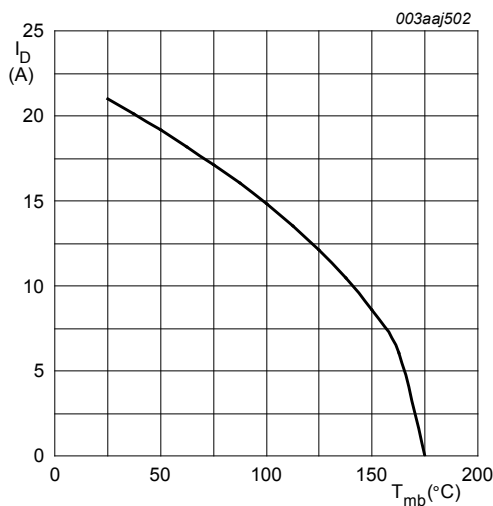
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$ ; $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	100	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC	-10	10	V
		$T_j \leq 175\text{ °C}$ ; Pulsed	[1][2]	15	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	21	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	15	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4	-	83	A

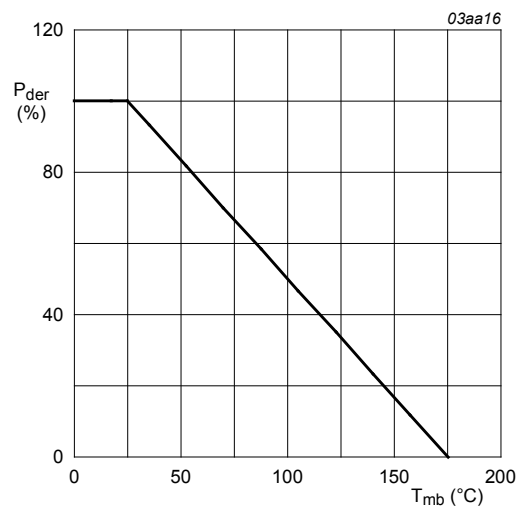
Symbol	Parameter	Conditions	Min	Max	Unit
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	53	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode FET1 and FET2</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	21	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	83	A
<b>Avalanche Ruggedness FET1 and FET2</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 21\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>	<a href="#">[3][4]</a>	-	48 mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering  $T_j$  and or  $V_{GS}$ .
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



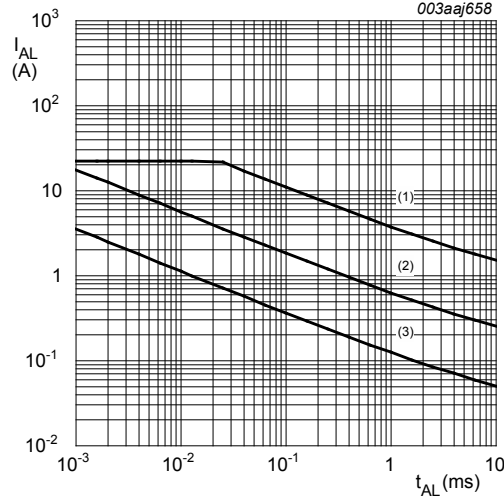
**Fig. 1. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 5V$$



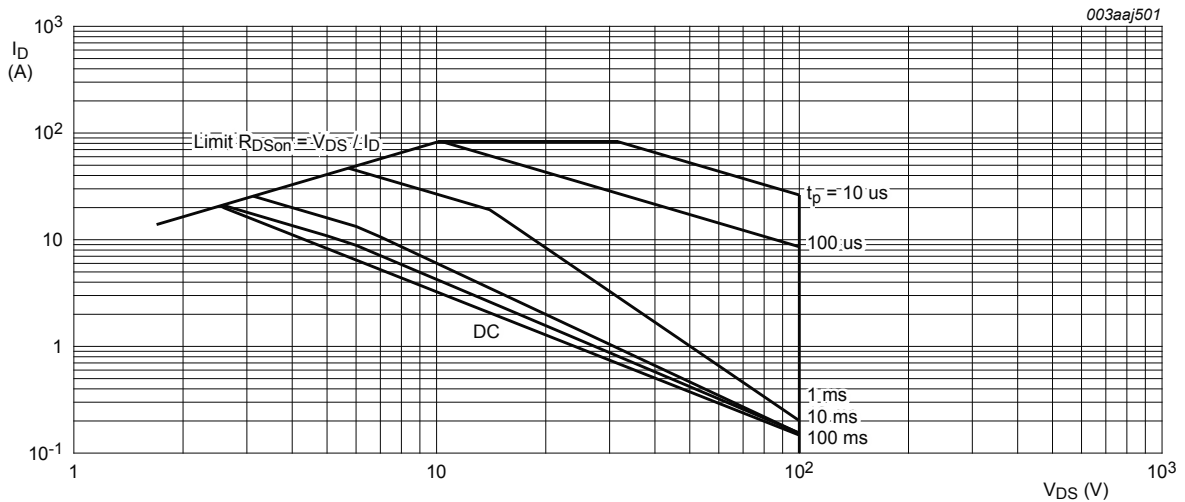
**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ }^\circ\text{C})}} \times 100\%$$



**Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2**

- (1) Single-pulse;  $T_j = 25\text{ }^\circ\text{C}$ .
- (2) Single-pulse;  $T_j = 150\text{ }^\circ\text{C}$ .
- (3) Repetitive.



**Fig. 4. Safe operating area; continuous and peak drain current as a function of drain-source voltage**

$T_{mb} = 25\text{ }^\circ\text{C}; I_{DM}$  is single pulse

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	2.84	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

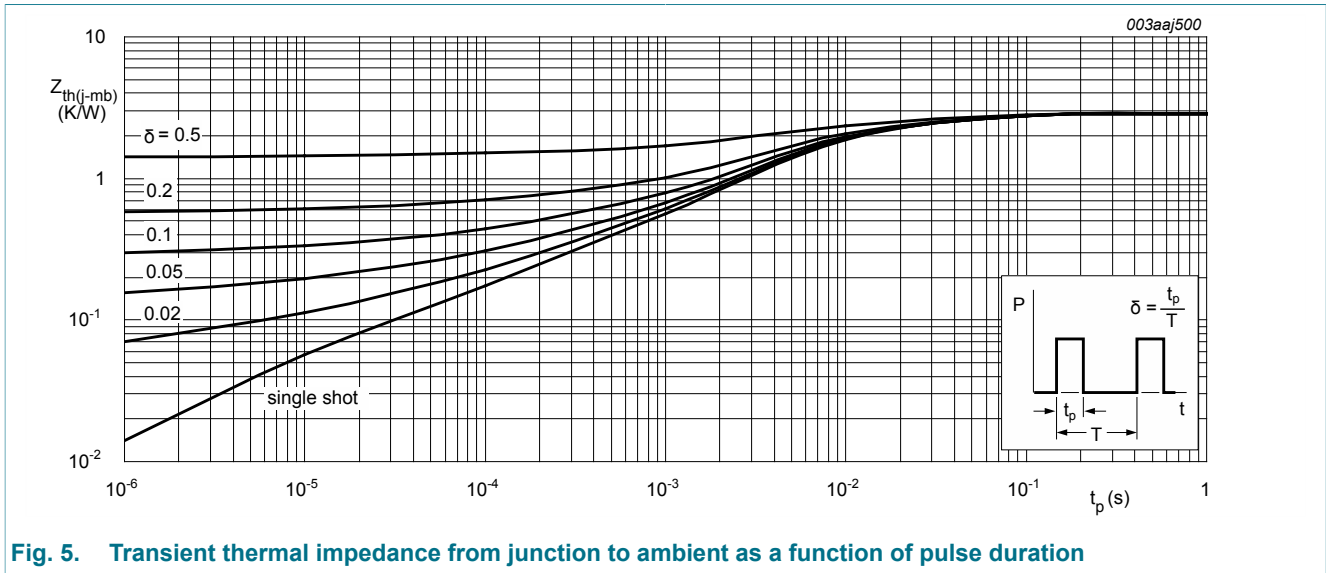


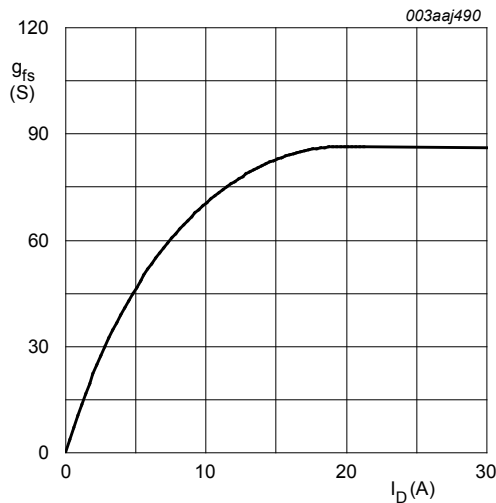
Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

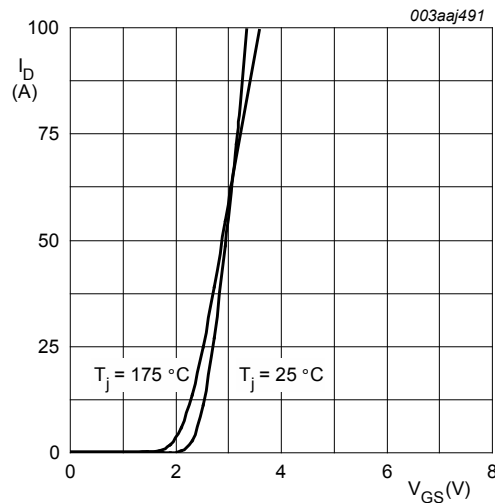
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	38.3	45	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	103	124	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	35.3	42	m $\Omega$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V};$ $T_J = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	33.5	-	nC
$Q_{GS}$	gate-source charge	$T_J = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	3.5	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V};$ $T_J = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	7.3	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_J = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	1614	2152	pF
$C_{oss}$	output capacitance	$T_J = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	113	136	pF
$C_{rss}$	reverse transfer capacitance		-	72	99	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 80 \text{ V}; R_L = 16 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(\text{ext})} = 10 \text{ } \Omega; T_J = 25 \text{ }^\circ\text{C}; I_D = 5 \text{ A}$	-	4	-	ns
$t_r$	rise time		-	8.47	-	ns
$t_{d(\text{off})}$	turn-off delay time	$V_{DS} = 80 \text{ V}; R_L = 16 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(\text{ext})} = 10 \text{ } \Omega; I_D = 18 \text{ A}; T_J = 25 \text{ }^\circ\text{C};$ $I_D = 5 \text{ A}$	-	41.34	-	ns
$t_f$	fall time		-	27.75	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 17</a>	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 50 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	29.6	-	ns
$Q_r$	recovered charge		-	42.9	-	nC



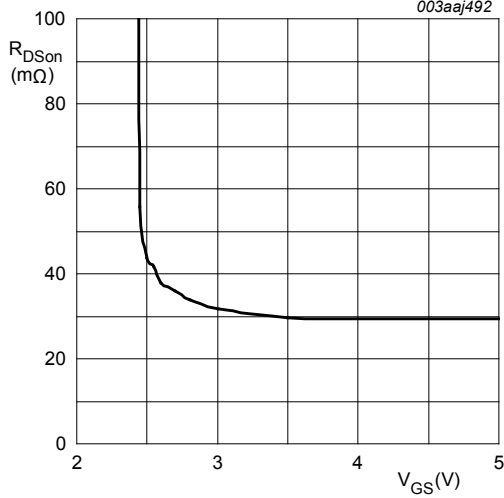
**Fig. 6. Forward transconductance as a function of drain current; typical values**

$$T_J = 25 \text{ }^\circ\text{C}; V_{DS} = 15 \text{ V}$$



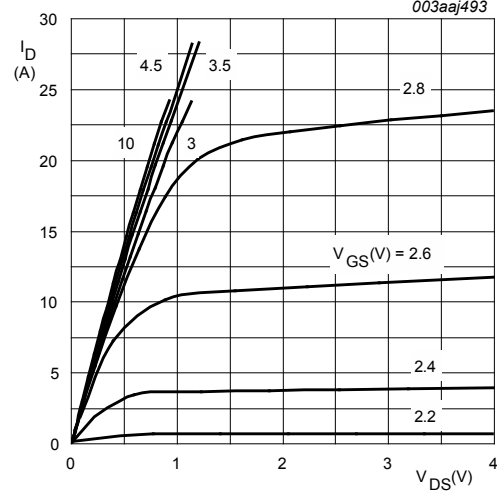
**Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

$$V_{DS} = 10 \text{ V}$$



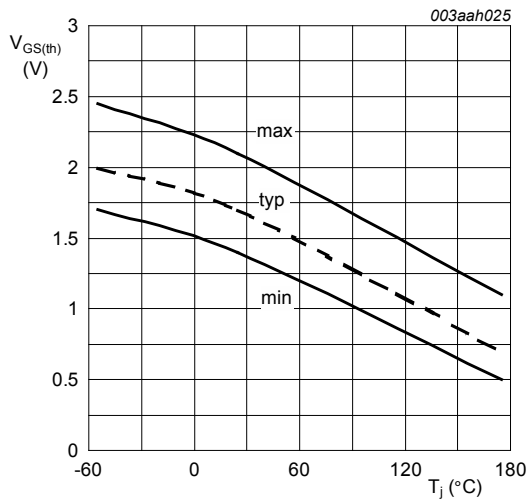
**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25^\circ\text{C}; I_D = 5\text{ A}$



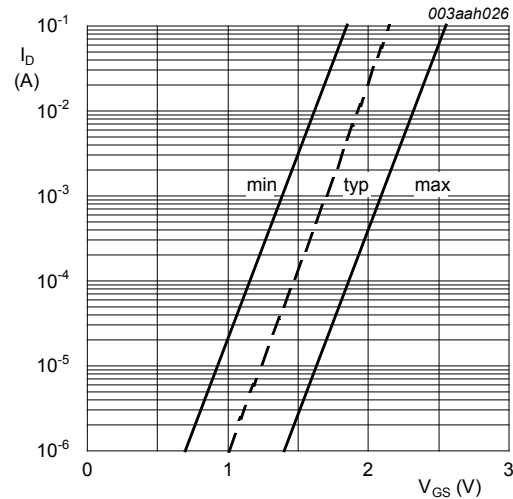
**Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values**

$T_j = 25^\circ\text{C}$



**Fig. 10. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$



**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$

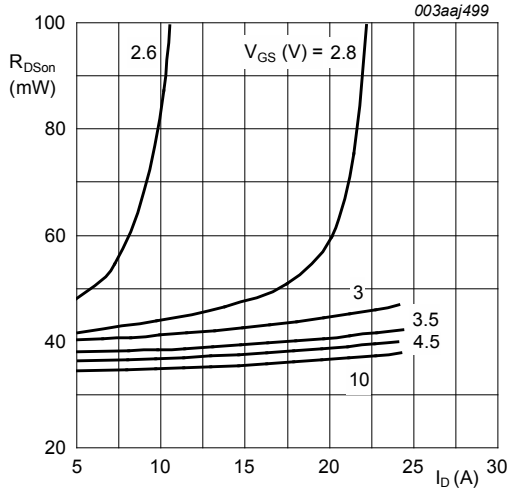


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

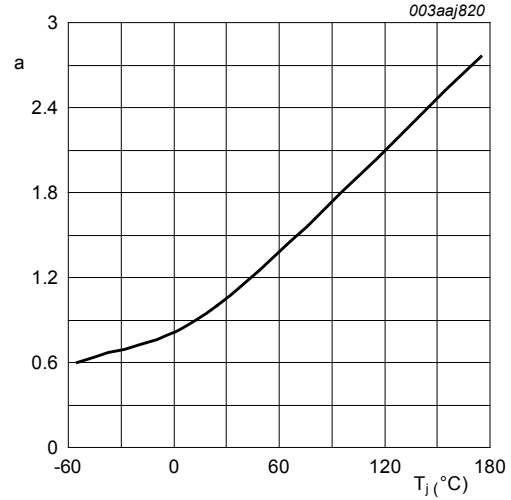


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

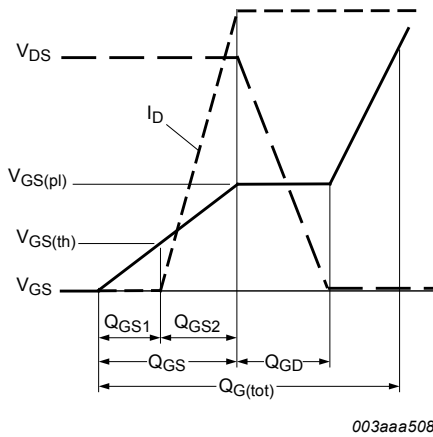


Fig. 14. Gate charge waveform definitions

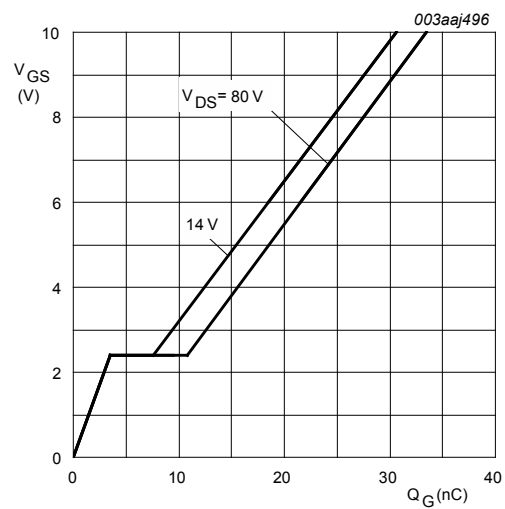
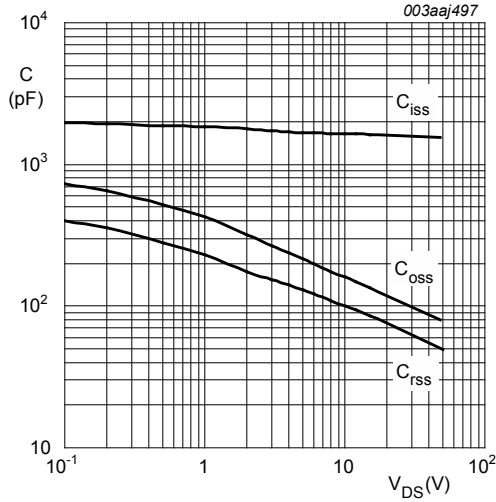


Fig. 15. Gate-source voltage as a function of gate charge; typical values

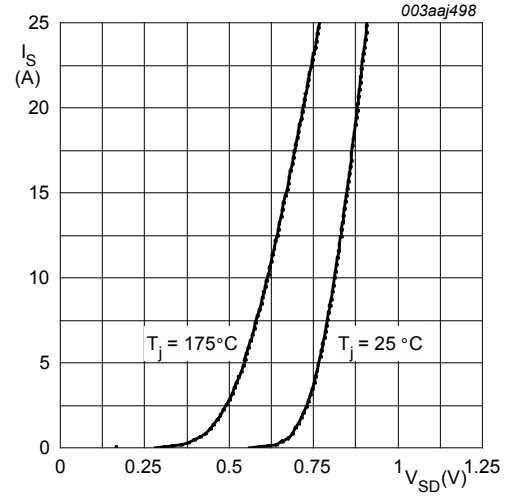
$$T_j = 25^\circ\text{C}; I_D = 5\text{A}$$





**Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$



**Fig. 17. Source current as a function of source-drain voltage; typical values**

$$V_{GS} = 0\text{ V}$$

### 11. Package outline

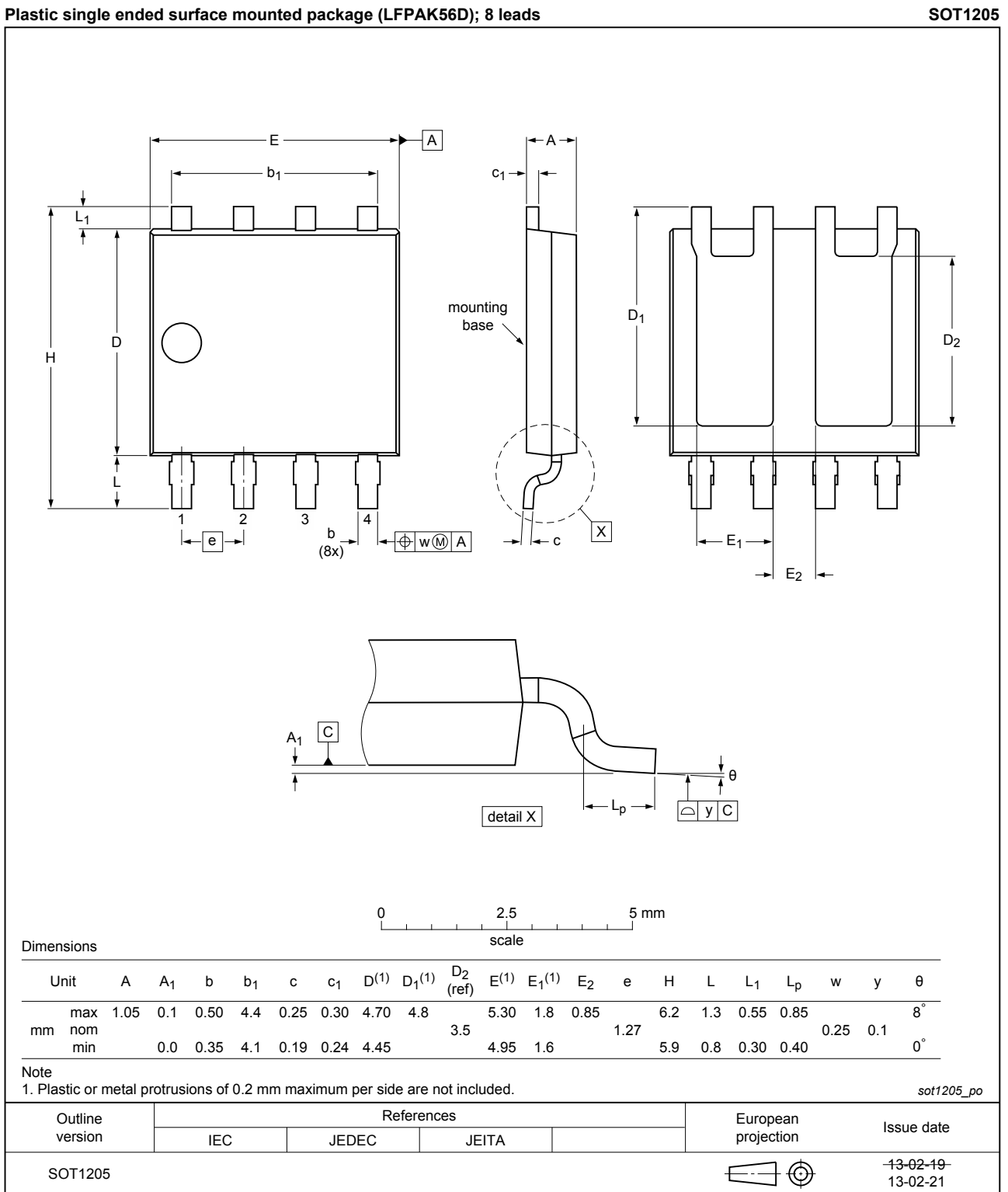


Fig. 18. Package outline LPAK56D (SOT1205)

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
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