



# BUK9K5R1-30E

Dual N-channel 30 V, 5.3 mΩ logic level MOSFET

2 September 2015

Product data sheet

## 1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)}$  rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

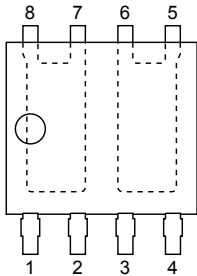
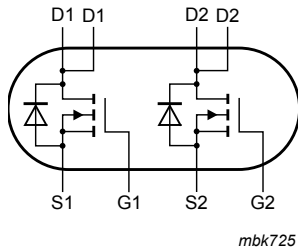
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	30	V
$I_D$	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	[1]	-	40	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1	-	-	68	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C};$ Fig. 11	-	4.2	5.3	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 10\text{ A}; V_{DS} = 24\text{ V}; V_{GS} = 5\text{ V}; T_j = 25\text{ °C};$ Fig. 13; Fig. 14	-	11	-	nC

[1] Continuous current is limited by package

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K5R1-30E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K5R1-30E	95E130

## 8. Limiting values

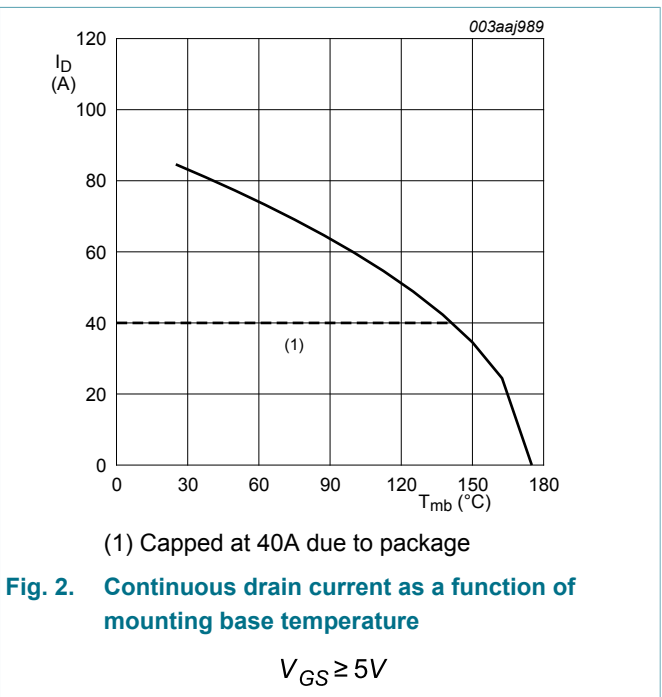
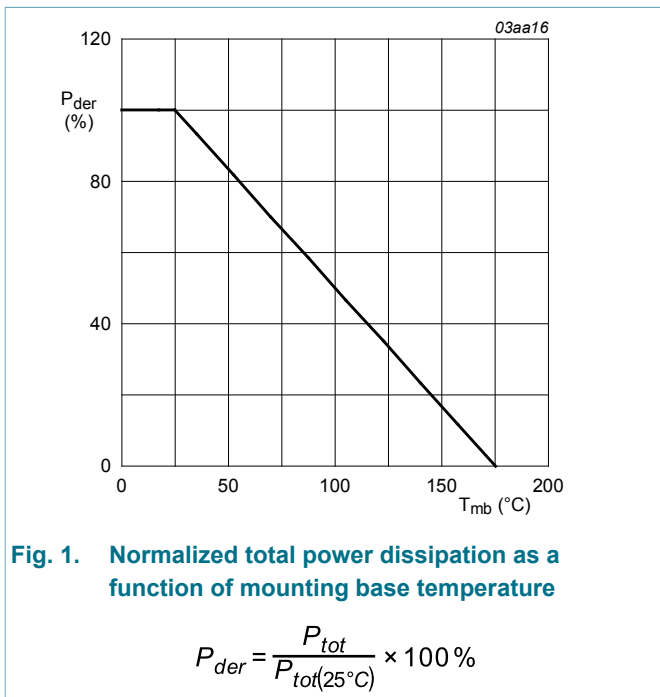
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC	-10	10	V
		$T_j \leq 175\text{ °C}$ ; Pulsed	[1][2]	15	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1	-	68	W
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 2	[3]	40	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 2	[3]	40	A

Symbol	Parameter	Conditions	Min	Max	Unit
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs; Fig. 3	-	329	A
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode FET1 and FET2</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[3]	40	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	329	A
<b>Avalanche Ruggedness FET1 and FET2</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 40 A; V <sub>sup</sub> ≤ 30 V; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; Fig. 4	[4][5]	214	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>.
- [3] Continuous current is limited by package
- [4] Refer to application note AN10273 for further information
- [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



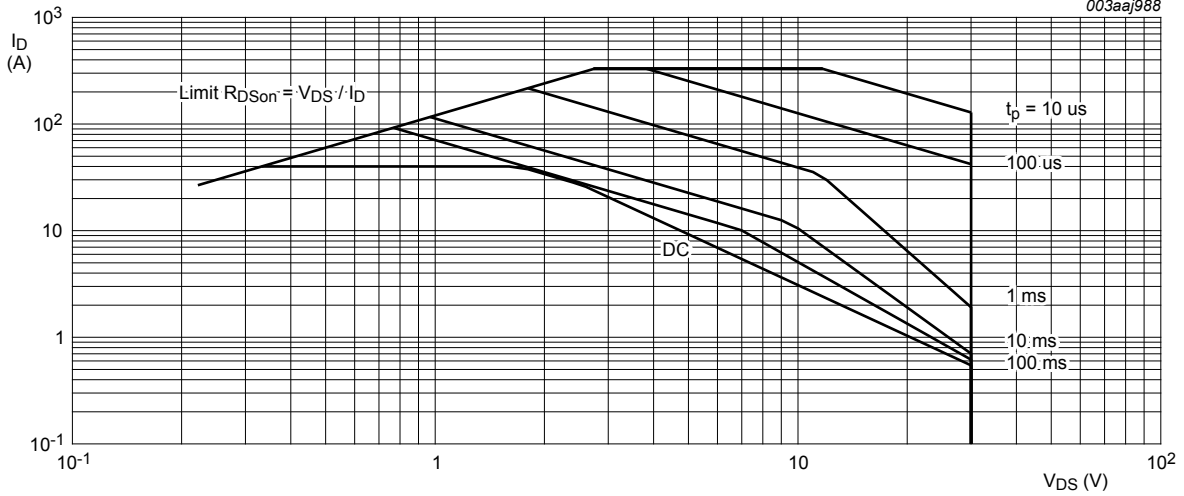


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$ ;  $I_{DM}$  is a single pulse

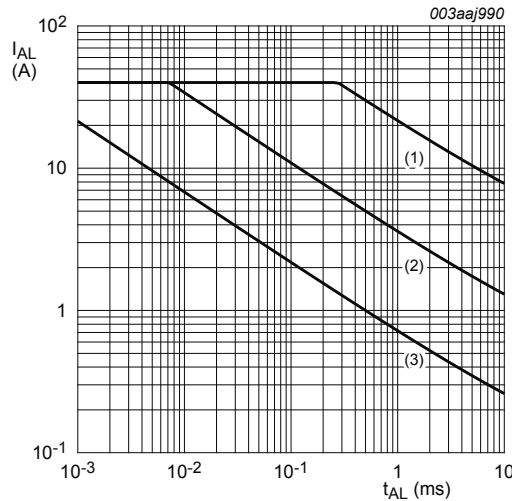


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j(init)} = 25^\circ C$ ; (2)  $T_{j(init)} = 150^\circ C$ ; (3) Repetitive Avalanche

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	2.21	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

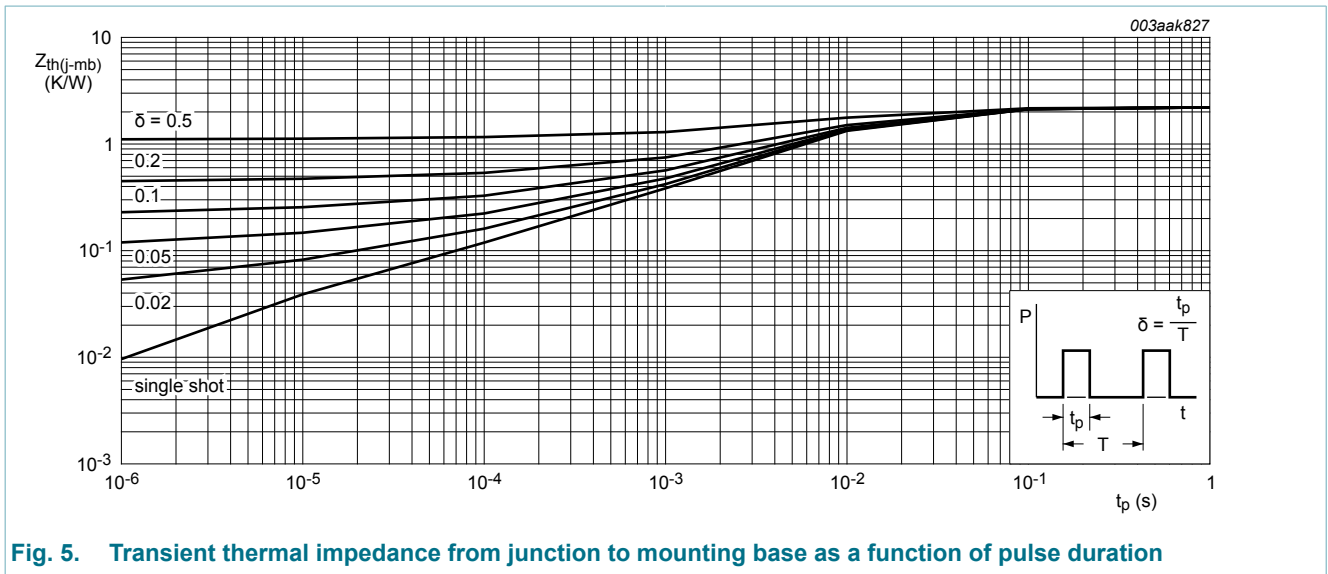


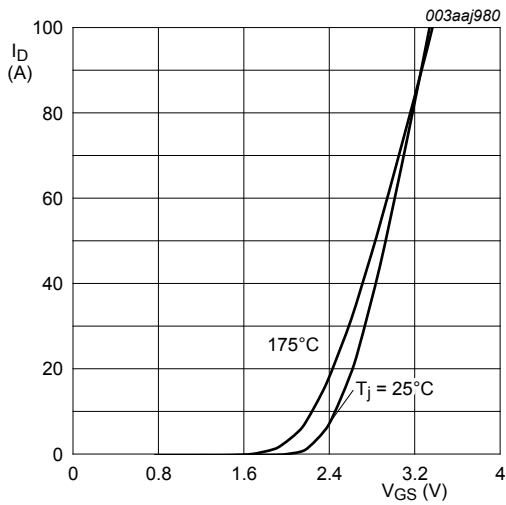
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

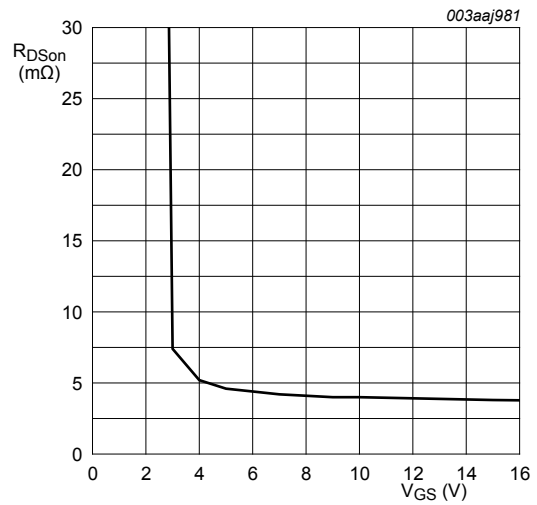
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 10 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	4.2	5.3	mΩ
		$V_{GS} = 5 V; I_D = 10 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 11</a>	-	7.5	10	mΩ
		$V_{GS} = 10 V; I_D = 10 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	3.5	4.4	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 10 A; V_{DS} = 24 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13; Fig. 14</a>	-	26.7	-	nC
$Q_{GS}$	gate-source charge		-	5.4	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{GD}$	gate-drain charge		-	11	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	2300	3065	pF
$C_{oss}$	output capacitance		-	421	506	pF
$C_{rss}$	reverse transfer capacitance		-	257	352	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 24\text{ V}; R_L = 2.4\text{ }\Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	14	-	ns
$t_r$	rise time		-	32	-	ns
$t_{d(off)}$	turn-off delay time		-	37	-	ns
$t_f$	fall time		-	31	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	0.79	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	25.8	-	ns
$Q_r$	recovered charge		-	16.2	-	nC



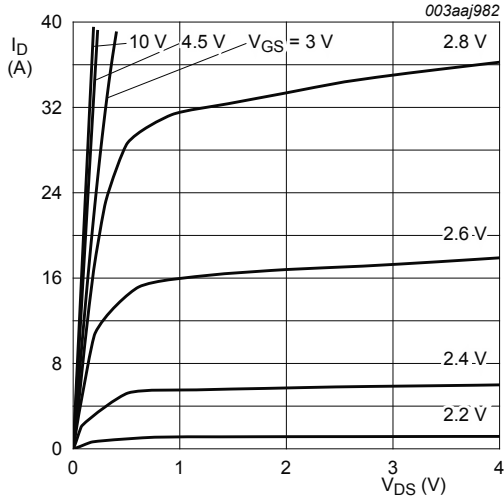
**Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10\text{ V}$



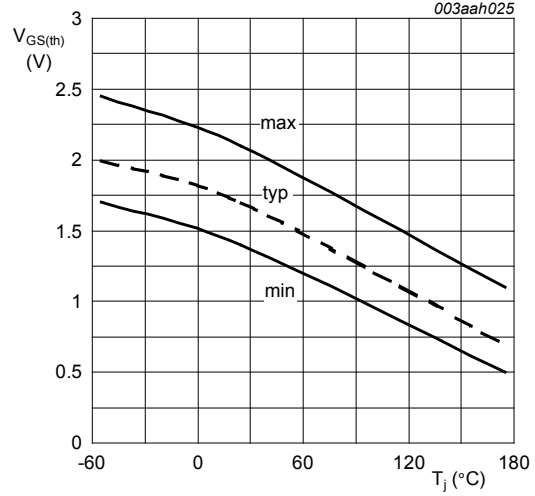
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$



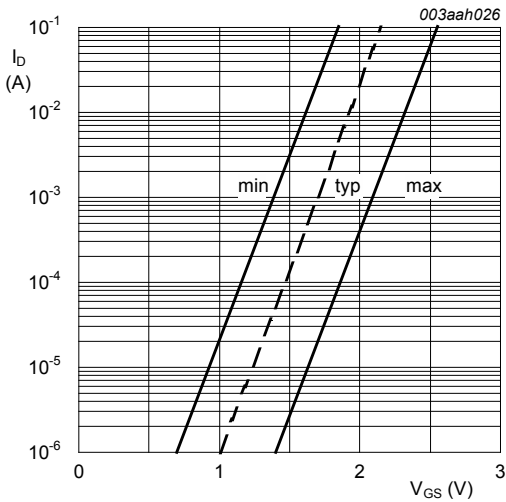
$T_j = 25\text{ }^\circ\text{C}$

**Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values**



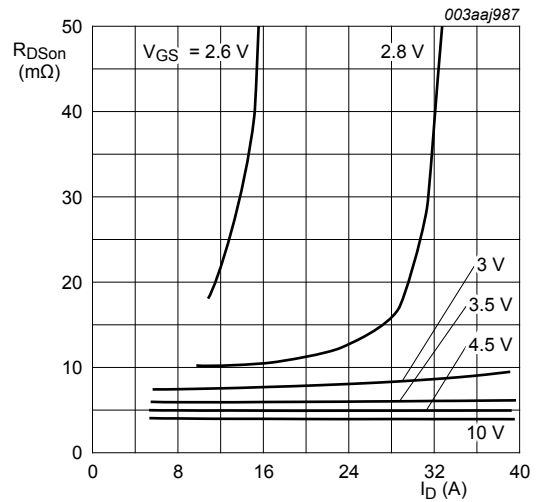
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$



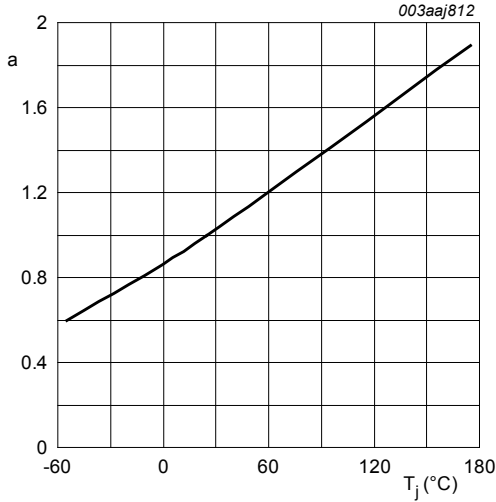
**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$



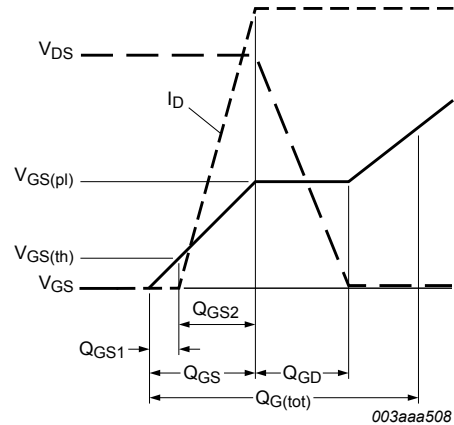
$T_j = 25\text{ }^\circ\text{C}$

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

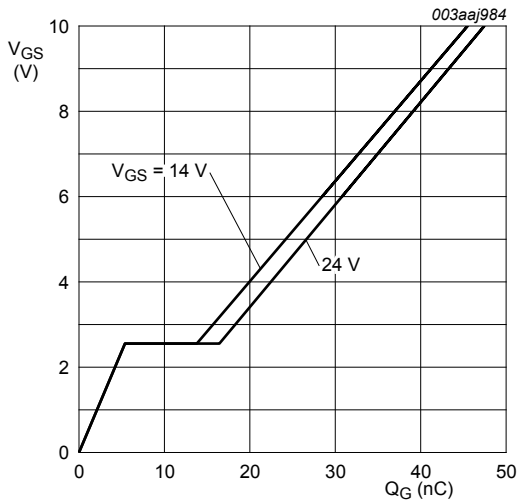


**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

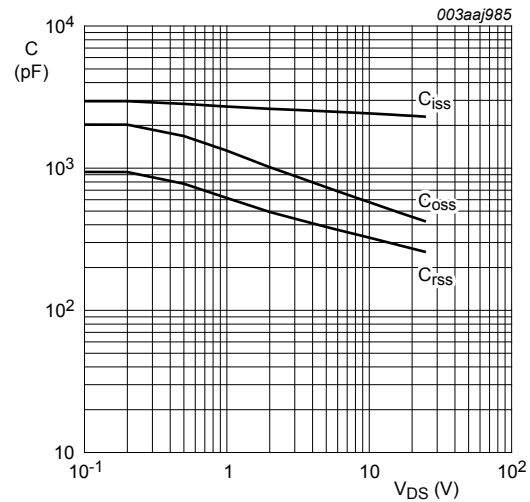


**Fig. 13. Gate charge waveform definitions**



**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

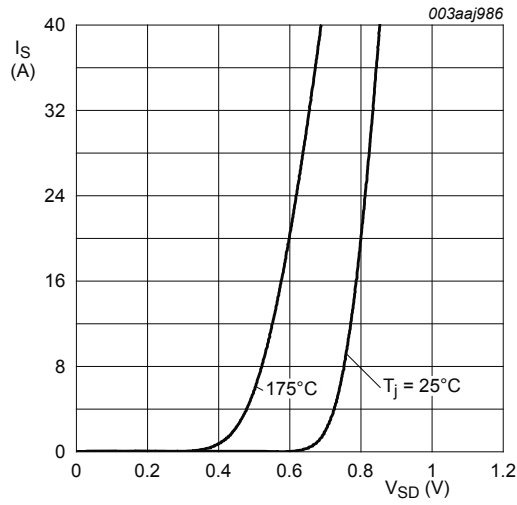
$$T_j = 25^{\circ}\text{C}; I_D = 10\text{A}$$



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

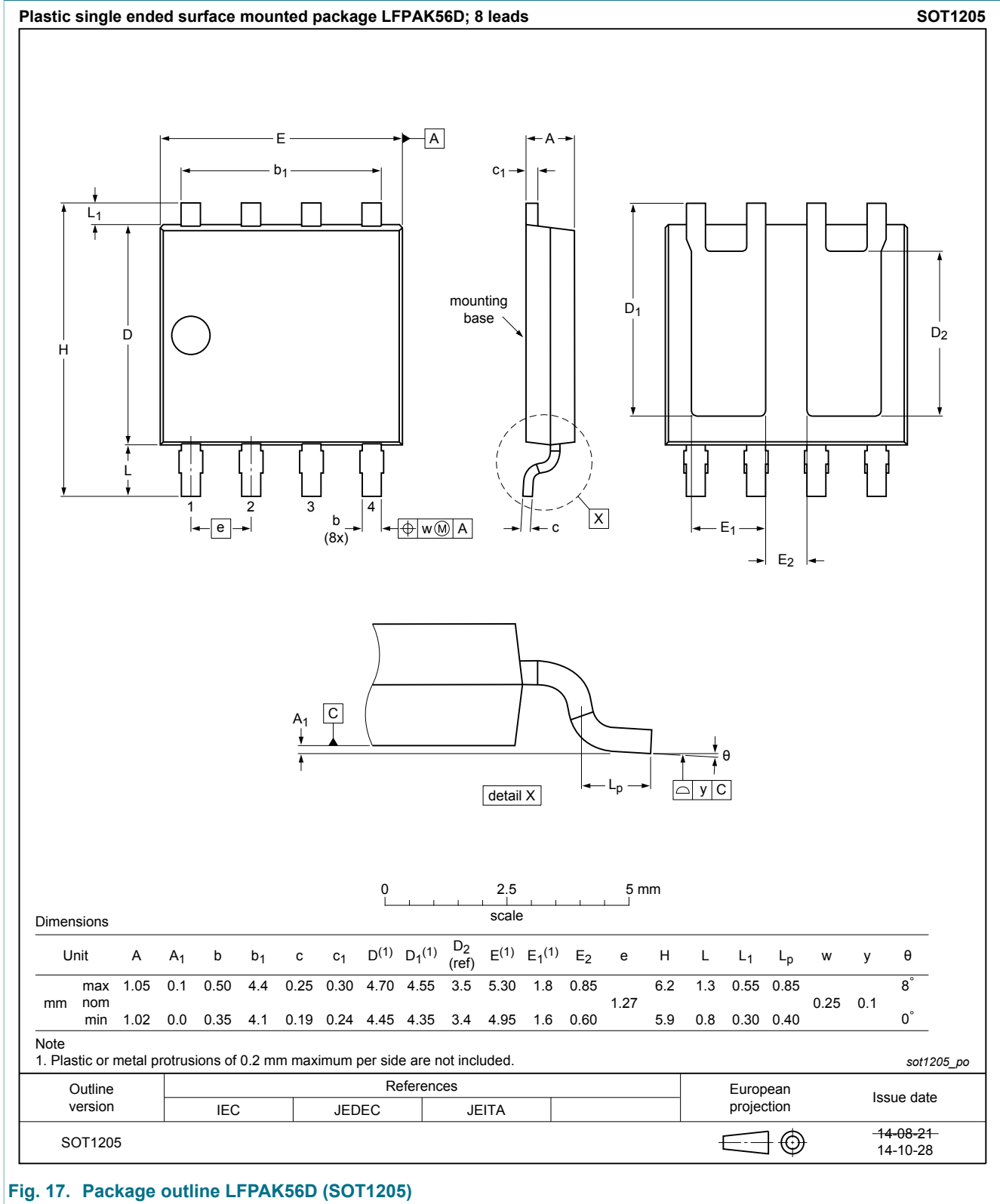




**Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

$$V_{GS} = 0V$$

### 11. Package outline



**Fig. 17. Package outline LFPAK56D (SOT1205)**

## 12. Legal information

### 12.1 Data sheet status

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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