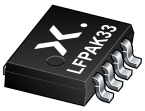


BUK9M67-60EL

Single N-channel 60 V, 44 mOhm logic level MOSFET in LFPAK33 using Enhanced SOA technology

7 April 2022 Product data sheet

1. General description

Single, logic level, N-channel MOSFET in LFPAK33 using Application specific (ASFET) Enhanced SOA technology. This product has been designed and qualified to AEC-Q101 for use in linear mode in airbag applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Enhanced SOA technology for improved linear mode performance
- LFPAK copper clip package technology:
  - High robustness and current handling capability
  - Gull wing leads for easy AOI inspection and exceptional board level reliability

3. Applications

- 12 V automotive systems
- Airbag squib voltage regulator MOSFET

4. Quick reference data

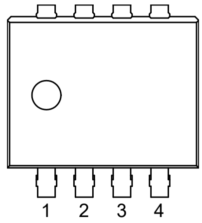
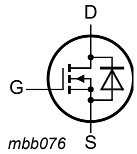
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	60	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	20	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	45	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 13		24.5	35	43.8	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 5 A; V_{DS} = 48 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 15; Fig. 16		-	3.1	6.2	nC

[1] 20 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9M67-60EL	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M67-60EL	9676EL

8. Limiting values

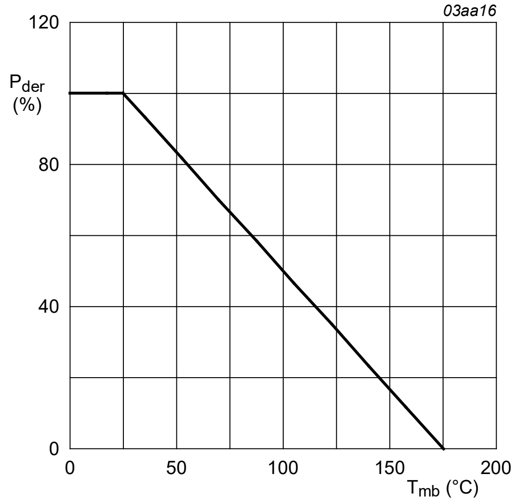
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	60	V
V_{GS}	gate-source voltage	DC; T_j ≤ 175 °C		-10	10	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	45	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	20	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	15	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3; Fig. 4		-	85	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	20	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	85	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 16.2 A; V_{sup} ≤ 60 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 22 µs; Fig. 5	[2] [3]	-	14.4	mJ

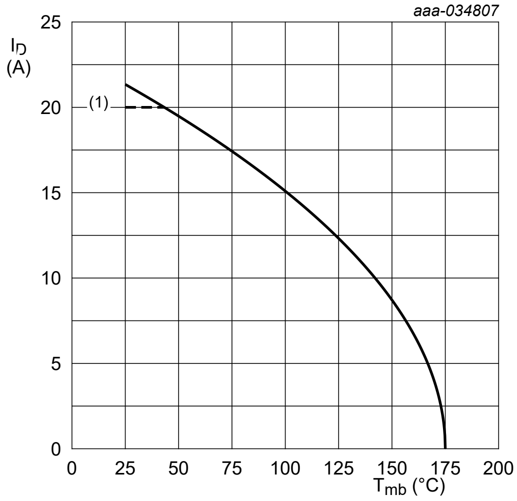
Symbol	Parameter	Conditions		Min	Max	Unit
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq$ 60 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 5	[2] [3] [4]	-	16.2	A

[1] 20 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Protected by 100% test.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

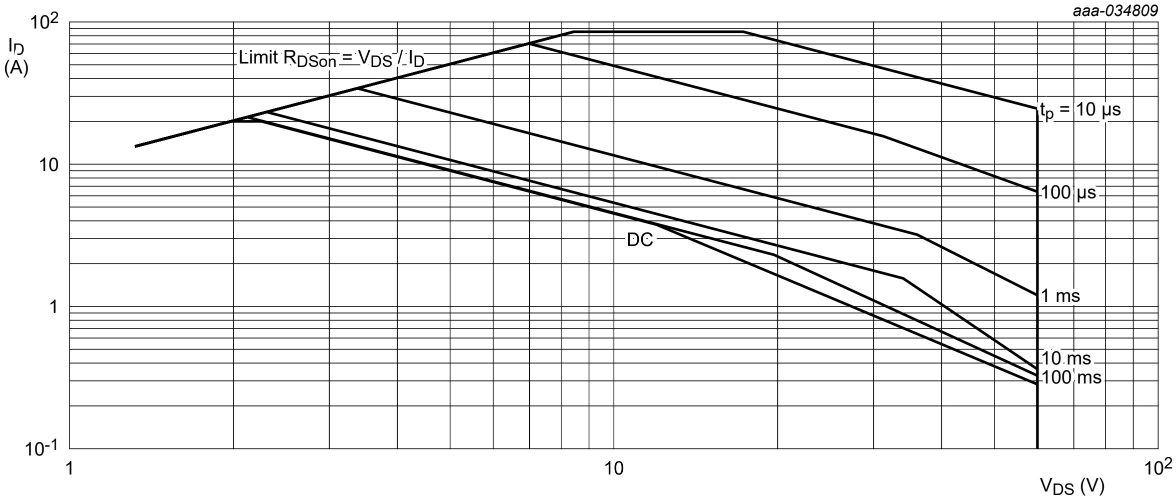
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq$ 10 V

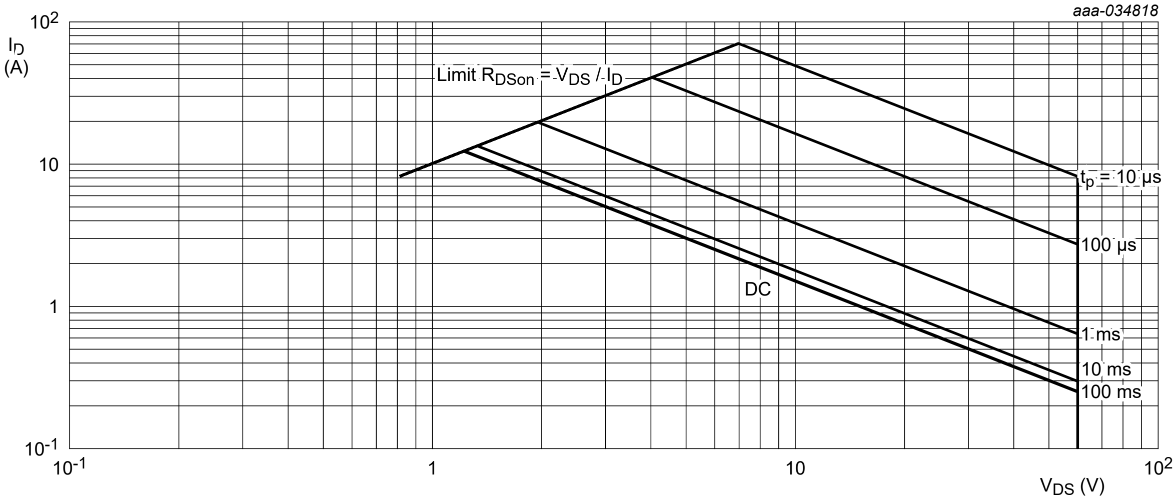
(1) 20 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



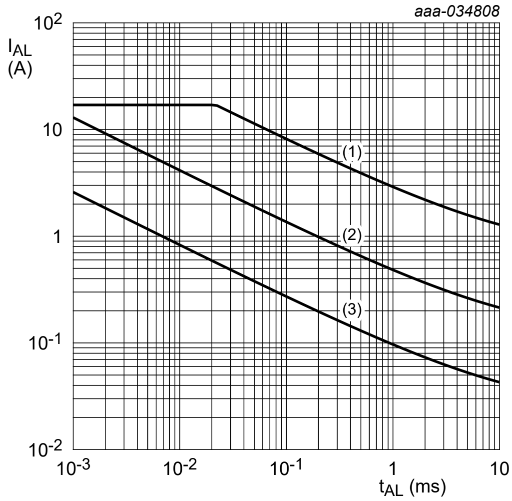
T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



T_{mb} = 125 °C; I_{DM} is a single pulse

Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	3.1	3.33	K/W

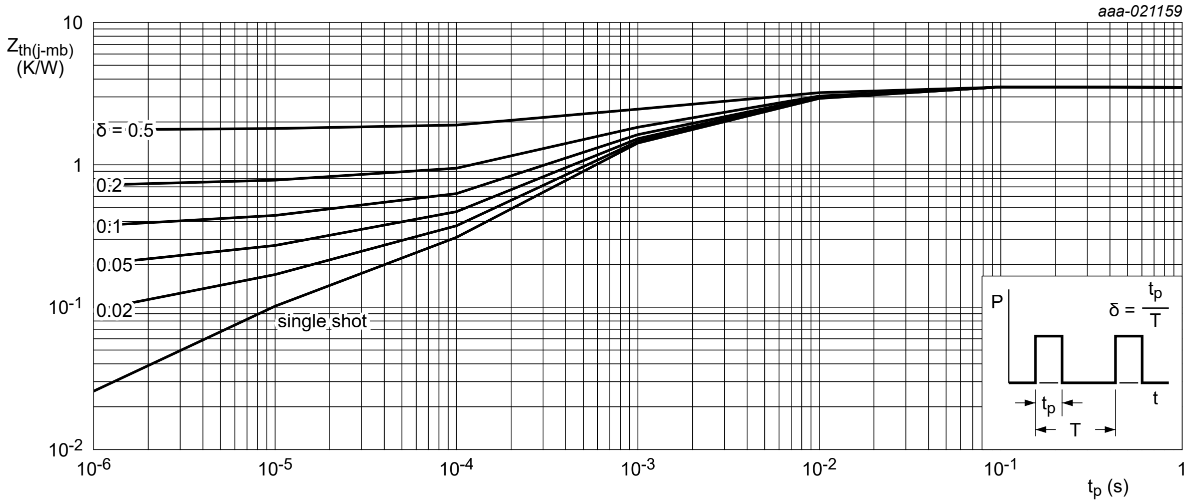


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

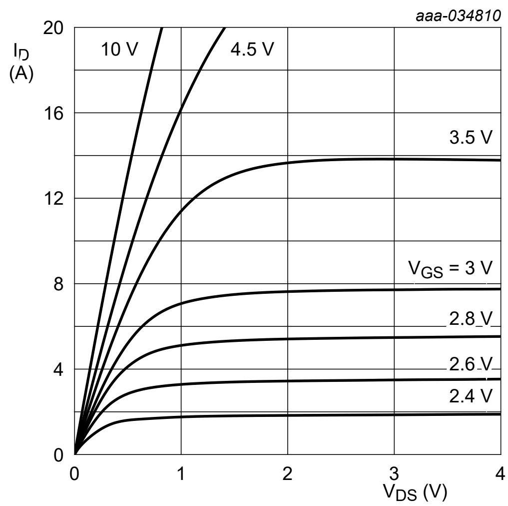
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		60	66	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	62.7	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		54	61.7	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 11; Fig. 12		1.4	1.65	2.1	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 12		-	-	2.45	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 12		0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C		-	0.003	1	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 °C		-	10	500	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 13		24.5	35	43.8	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 105 °C; Fig. 14		37.3	55.7	71	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 125 °C; Fig. 14		41	61	79	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 175 °C; Fig. 14		51	76	100	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C; Fig. 13		35	50	66.7	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 105 °C; Fig. 14		52	77	106	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 125 °C; Fig. 14		57	84.5	117.5	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 175 °C; Fig. 14		69	105	148	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		-	1.82	-	Ω

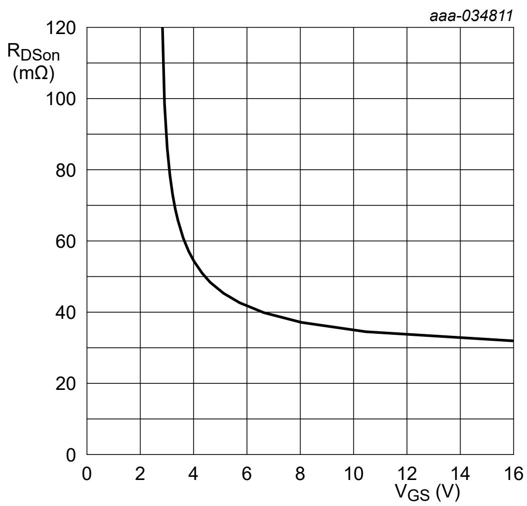
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 48 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 15; Fig. 16		-	7	10	nC
		I_D = 5 A; V_{DS} = 48 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 15; Fig. 16		-	14	19	nC
Q_{GS}	gate-source charge	I_D = 5 A; V_{DS} = 48 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 15; Fig. 16		-	1.8	2.7	nC
Q_{GD}	gate-drain charge			-	3.1	6.2	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 17		-	653	915	pF
C_{oss}	output capacitance			-	76	91	pF
C_{rss}	reverse transfer capacitance			-	46	63	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 48 V; R_L = 9.6 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	5	-	ns
t_r	rise time			-	9	-	ns
$t_{d(off)}$	turn-off delay time			-	10	-	ns
t_f	fall time			-	8	-	ns
g_{fs}	transfer conductance	V_{DS} = 8 V; I_D = 5 A; T_j = 25 °C; Fig. 9		-	12.3	-	S
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 18		-	0.83	1	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C; Fig. 19		-	23	-	ns
Q_r	recovered charge		[1]	-	22	-	nC

[1] includes capacitive recovery



T_j = 25 °C

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

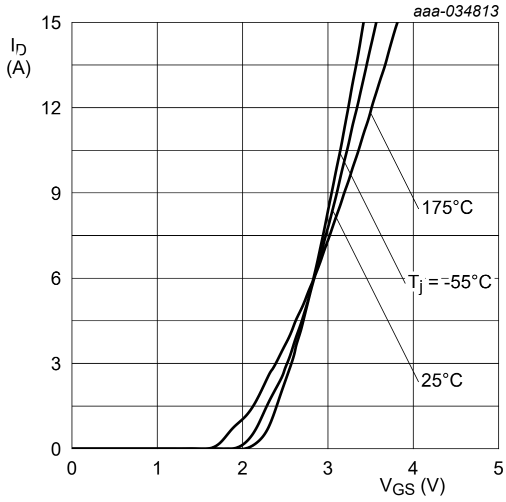


T_j = 25 °C; I_D = 5 A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

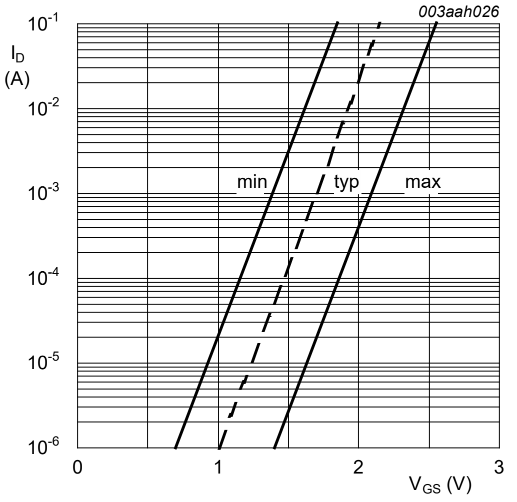
T_j = 25 °C; V_{DS} = 8 V

Fig. 9. Forward transconductance as a function of drain current; typical values



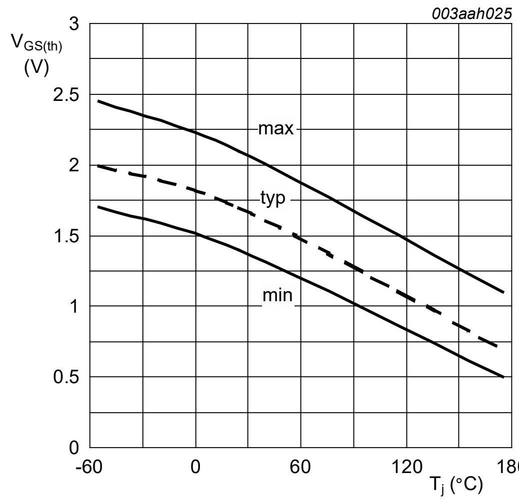
V_{DS} = 8 V

Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values



T_j = 25 °C; V_{DS} = 5 V

Fig. 11. Sub-threshold drain current as a function of gate-source voltage



I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 12. Gate-source threshold voltage as a function of junction temperature

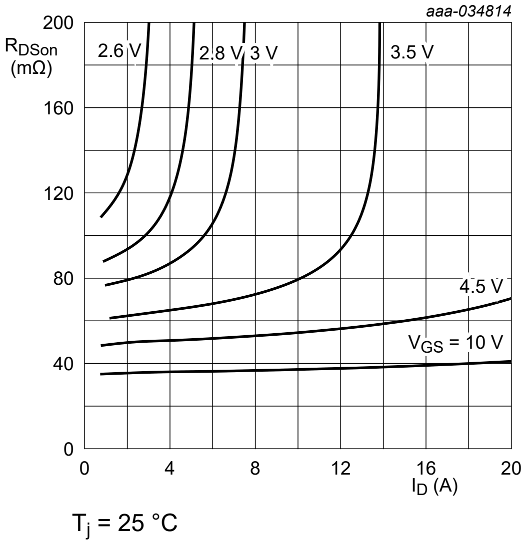
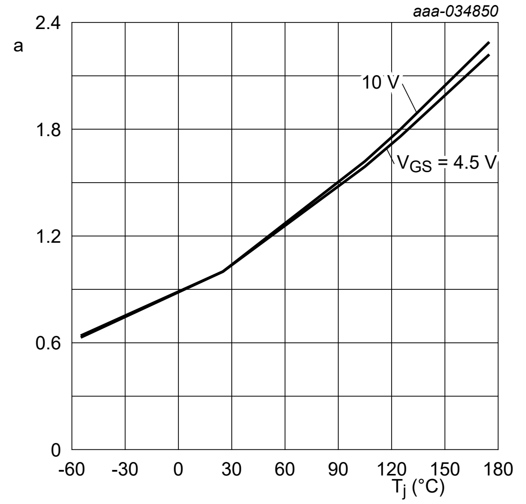


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 14. Normalized drain-source on-state resistance factor as a function of junction temperature

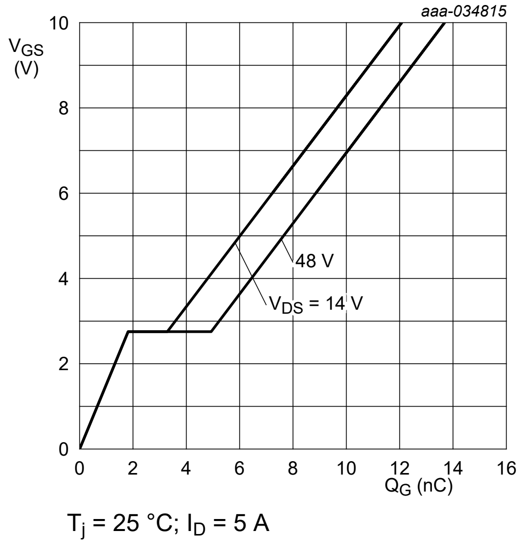


Fig. 15. Gate-source voltage as a function of gate charge; typical values

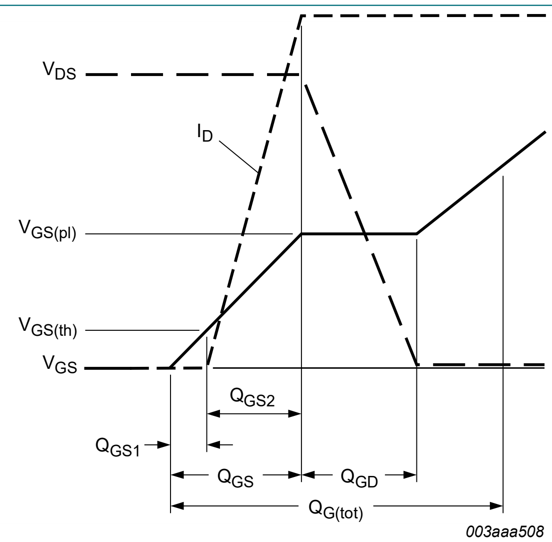
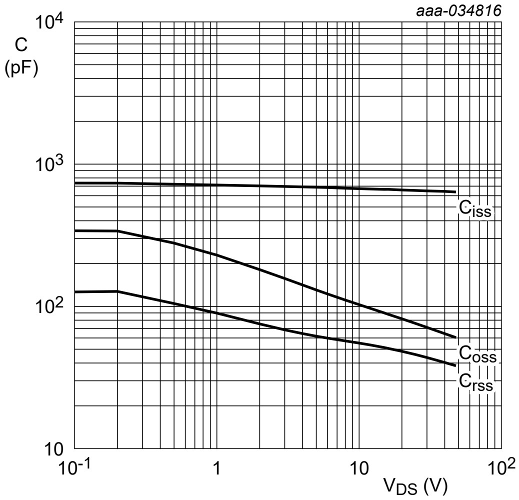
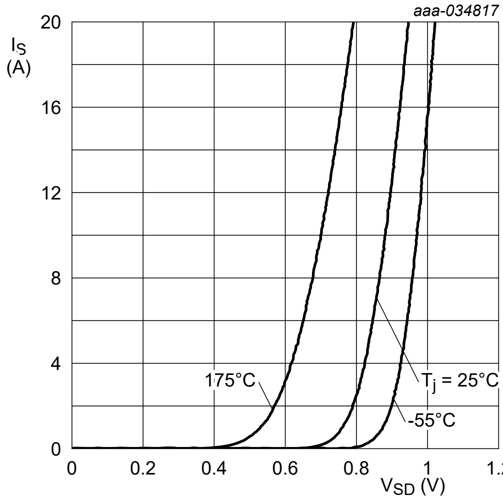


Fig. 16. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 18. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

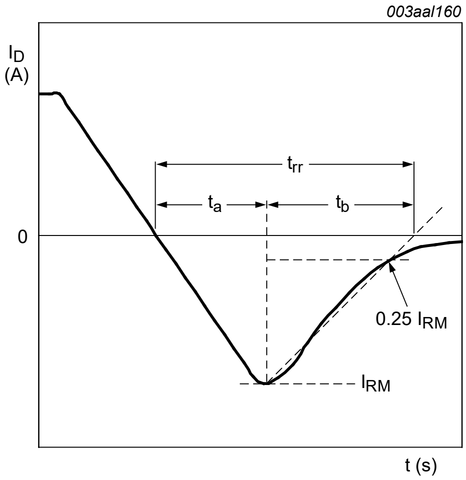
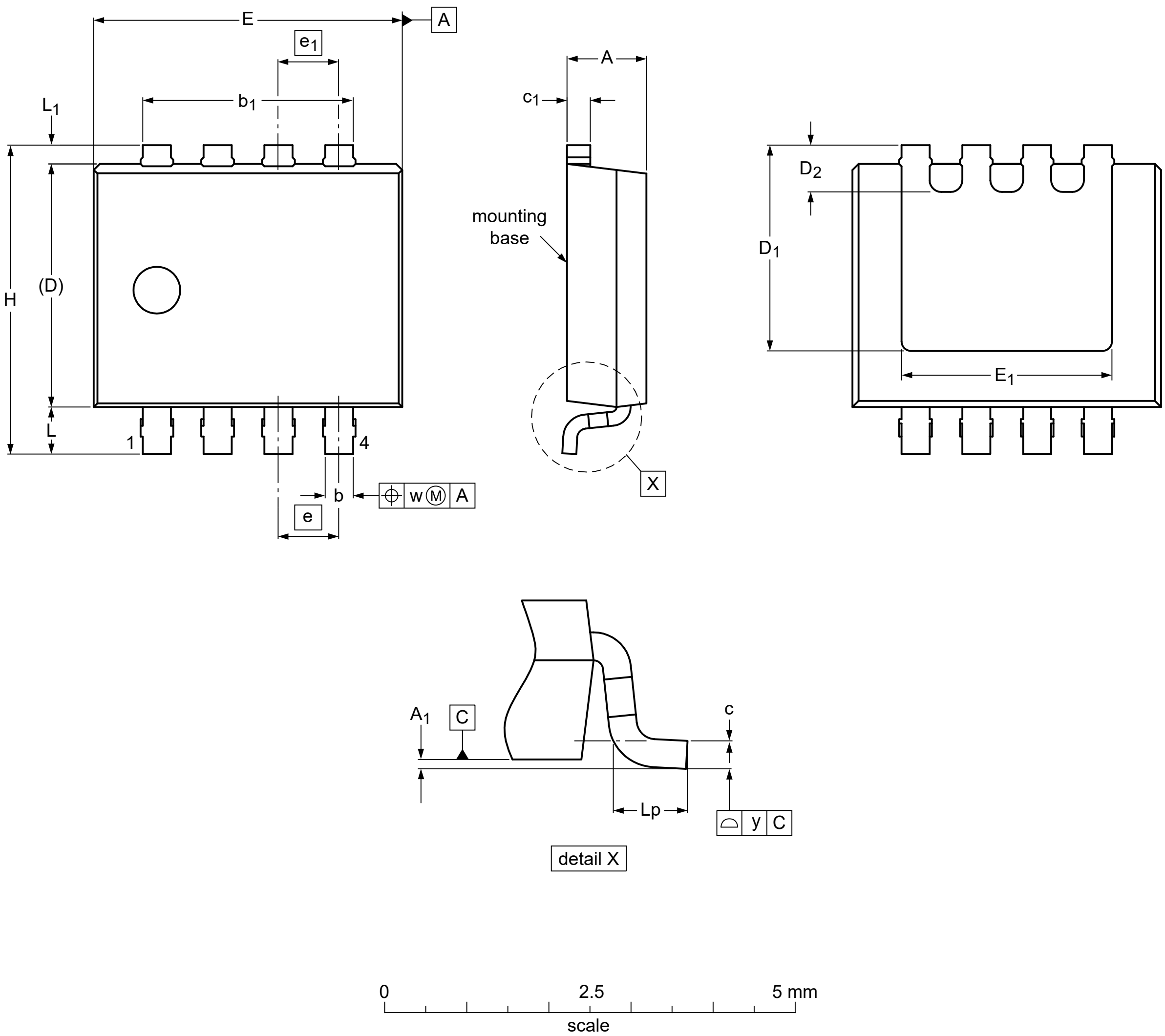


Fig. 19. Reverse recovery timing definition

11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit[(1)]		A	A_1	b[(1)]	b_1[(1)]	c	c_1	D ref	D_1	D_2	E[(1)]	E_1	e	e_1	H	L	L_1	L_p	w	y
mm	max	0.90	0.10	0.35	2.4	0.20	0.30		2.35		3.40	2.45			3.40	0.65	0.25	0.50		
	nom							2.60		0.50			0.65	0.65					0.20	0.10
	min	0.80	0.00	0.25	2.2	0.10	0.20		1.90		3.20	2.00			3.20	0.45	0.13	0.30		

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~14-04-25~~ 16-08-09

Fig. 20. Package outline LFPAK33 (SOT1210)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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