BUK9Y6R5-40H

N-channel 40 V, 6.5 mΩ logic level MOSFET in LFPAK56

1 May 2020 — Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced R_{th} and R_{DSon}
  - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

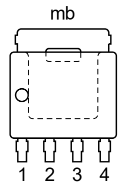
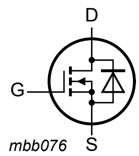
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	70	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	64	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 11		3.9	5.6	6.5	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 20 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 13; Fig. 14		-	2.2	4.5	nC
Source-drain diode							
Q_r	recovered charge	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 17		-	9.9	-	nC
S	softness factor	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 17		-	0.75	-	

[1] 70A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y6R5-40H	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y6R5-40H	96H540

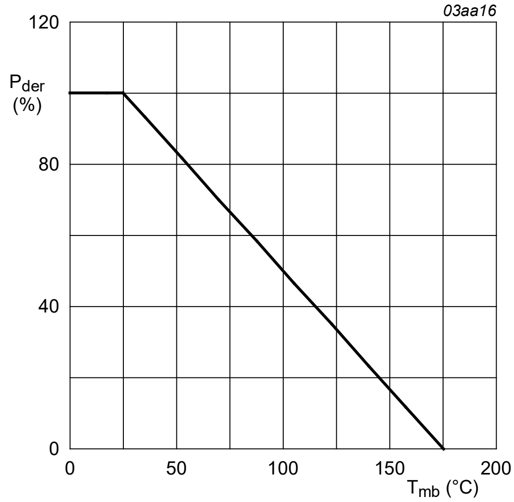
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

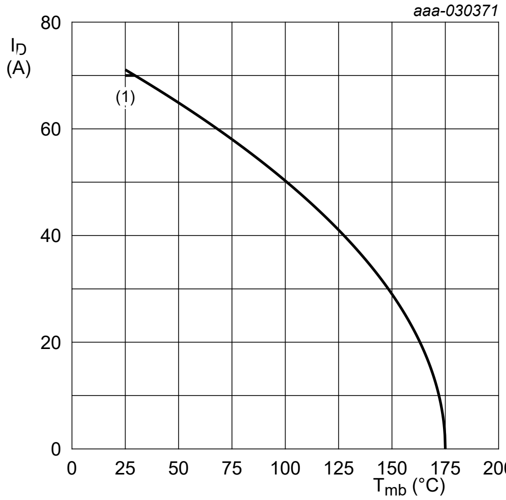
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	64	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	70	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	50	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	284	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	64	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	284	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 70 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[2] [3]	-	19.3	mJ

[1] 70A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

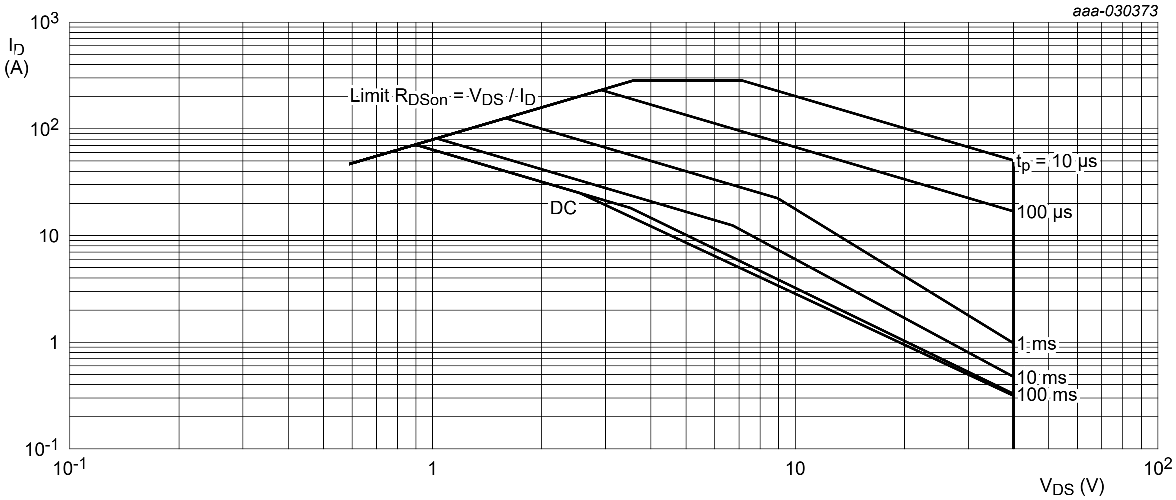
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 10 V

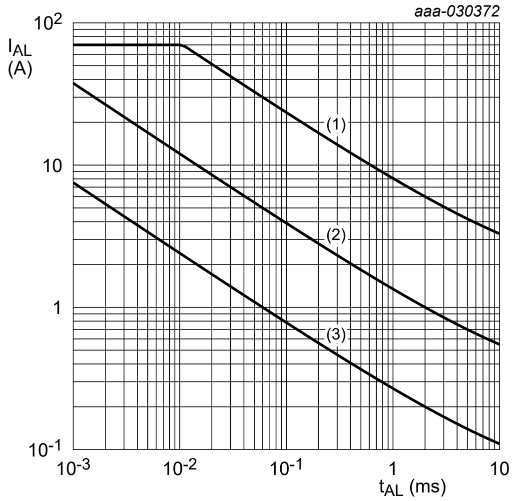
(1) 70A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\,(init)}$ = 25 °C; (2) $T_{j\,(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	2.17	2.35	K/W

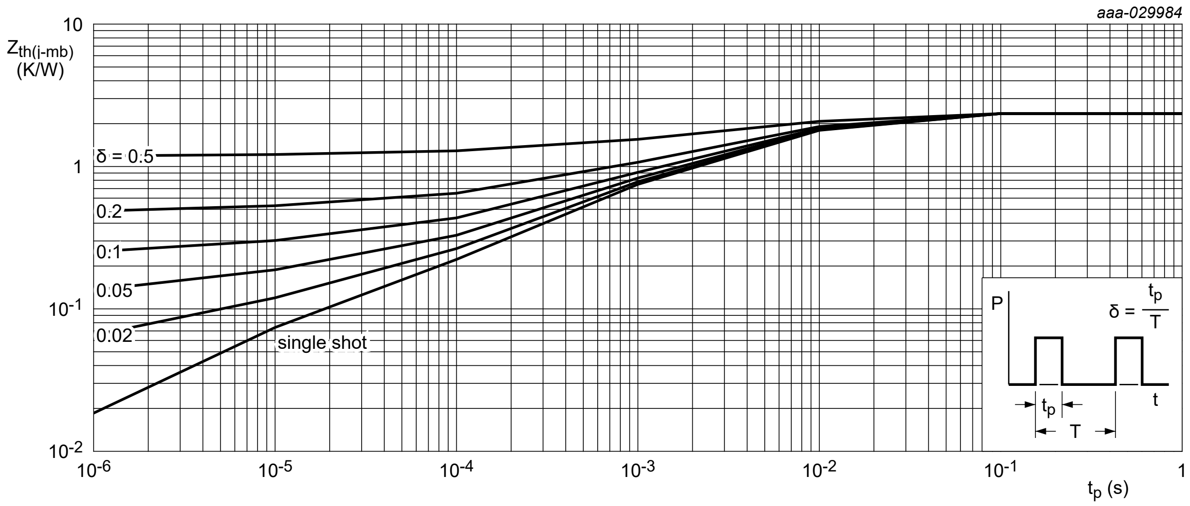


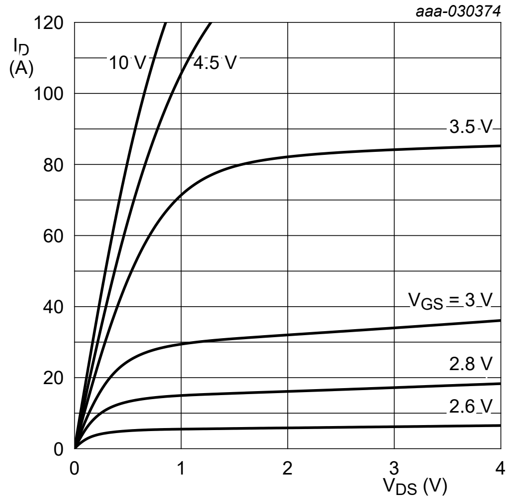
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

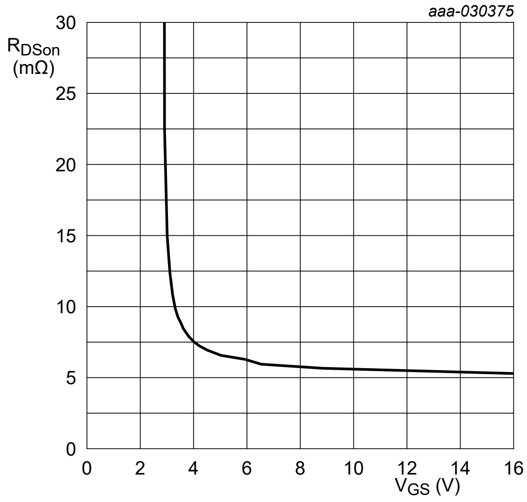
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	43	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	40.5	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		1.45	1.77	2.15	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 10		0.7	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	5	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	0.32	10	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	44	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 11		3.9	5.6	6.5	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 105 °C; Fig. 12		5.3	8.1	9.8	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 125 °C; Fig. 12		5.9	8.8	10.5	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 175 °C; Fig. 12		7.1	10.6	12.6	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 °C; Fig. 11		5	7.1	8.6	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 105 °C; Fig. 12		6.9	10.1	12.9	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 125 °C; Fig. 12		7.6	11	13.9	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 175 °C; Fig. 12		9.2	13.1	16.7	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.3	0.7	1.8	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 13; Fig. 14		-	21	29	nC
		I_D = 20 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 13; Fig. 14		-	9.5	13.3	nC
Q_{GS}	gate-source charge			-	4.1	6.2	nC
Q_{GD}	gate-drain charge			-	2.2	4.5	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	1454	2036	pF
C_{oss}	output capacitance			-	383	536	pF
C_{rss}	reverse transfer capacitance			-	54	119	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 1 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	10	-	ns
t_r	rise time			-	12	-	ns
$t_{d(off)}$	turn-off delay time			-	10	-	ns
t_f	fall time			-	6.3	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16		-	0.83	1	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 17		-	19	-	ns
Q_r	recovered charge			-	9.9	-	nC
S	softness factor	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 17		-	0.75	-	
		I_S = 20 A; dI_S/dt = -500 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 17		-	0.62	-	



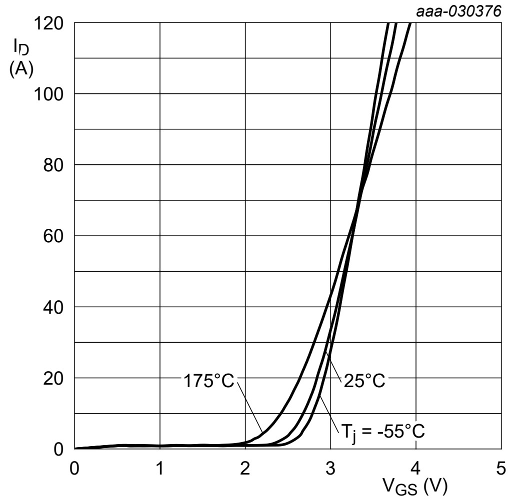
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



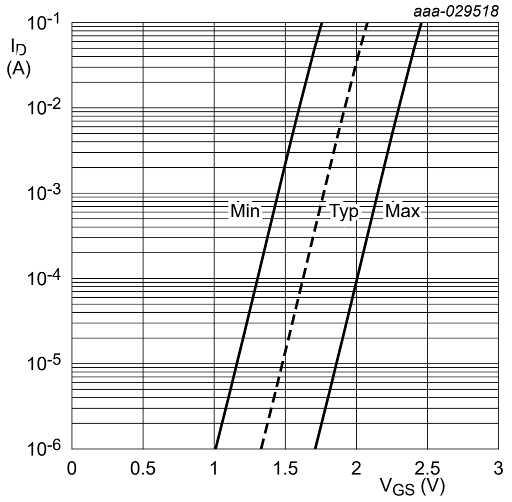
T_j = 25 °C; I_D = 20 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



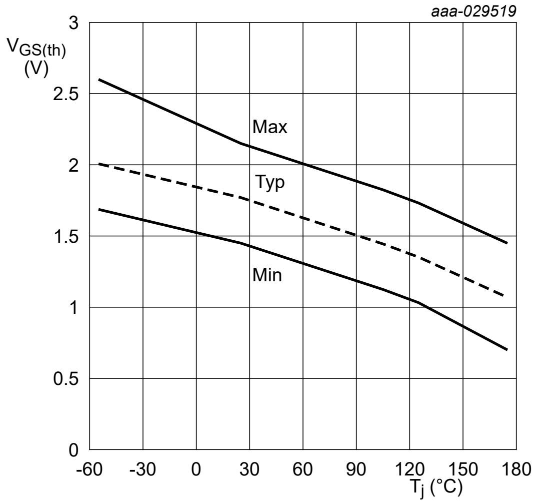
V_{DS} = 8 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



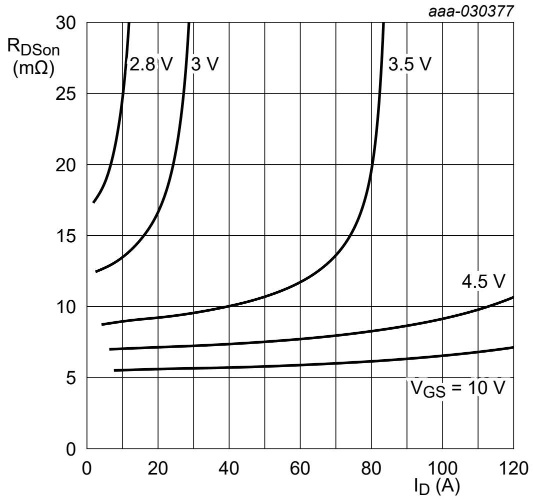
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage



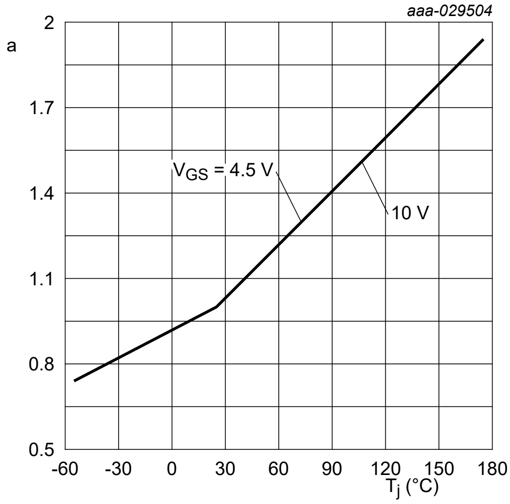
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 10. Gate-source threshold voltage as a function of junction temperature



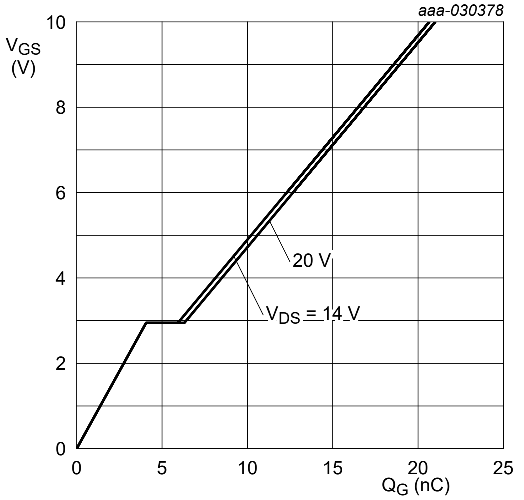
T_j = 25 °C

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 20 A

Fig. 13. Gate-source voltage as a function of gate charge; typical values

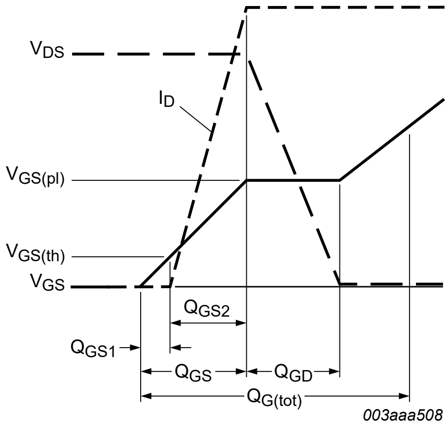
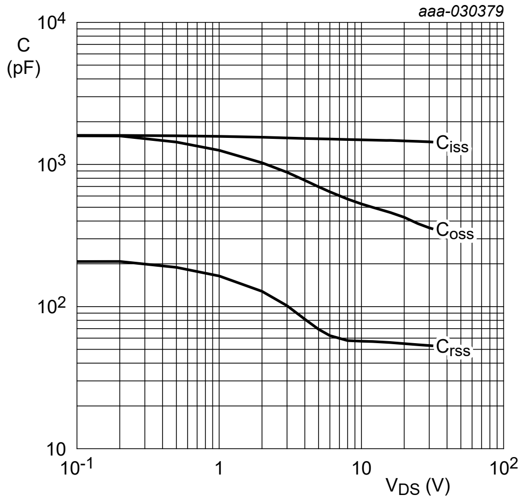
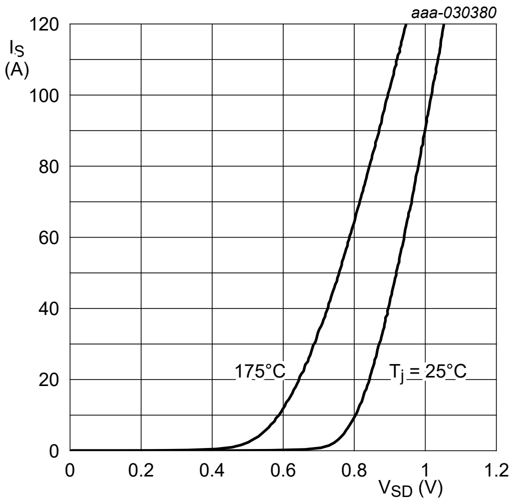


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

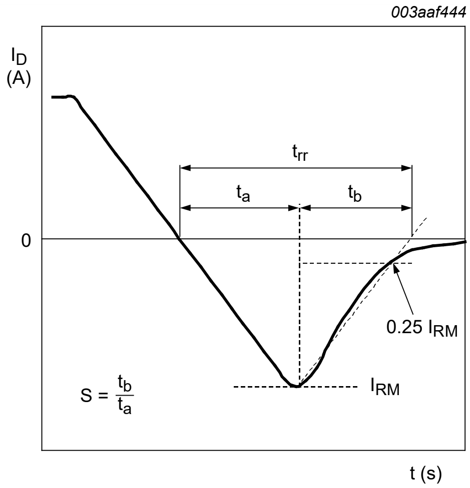
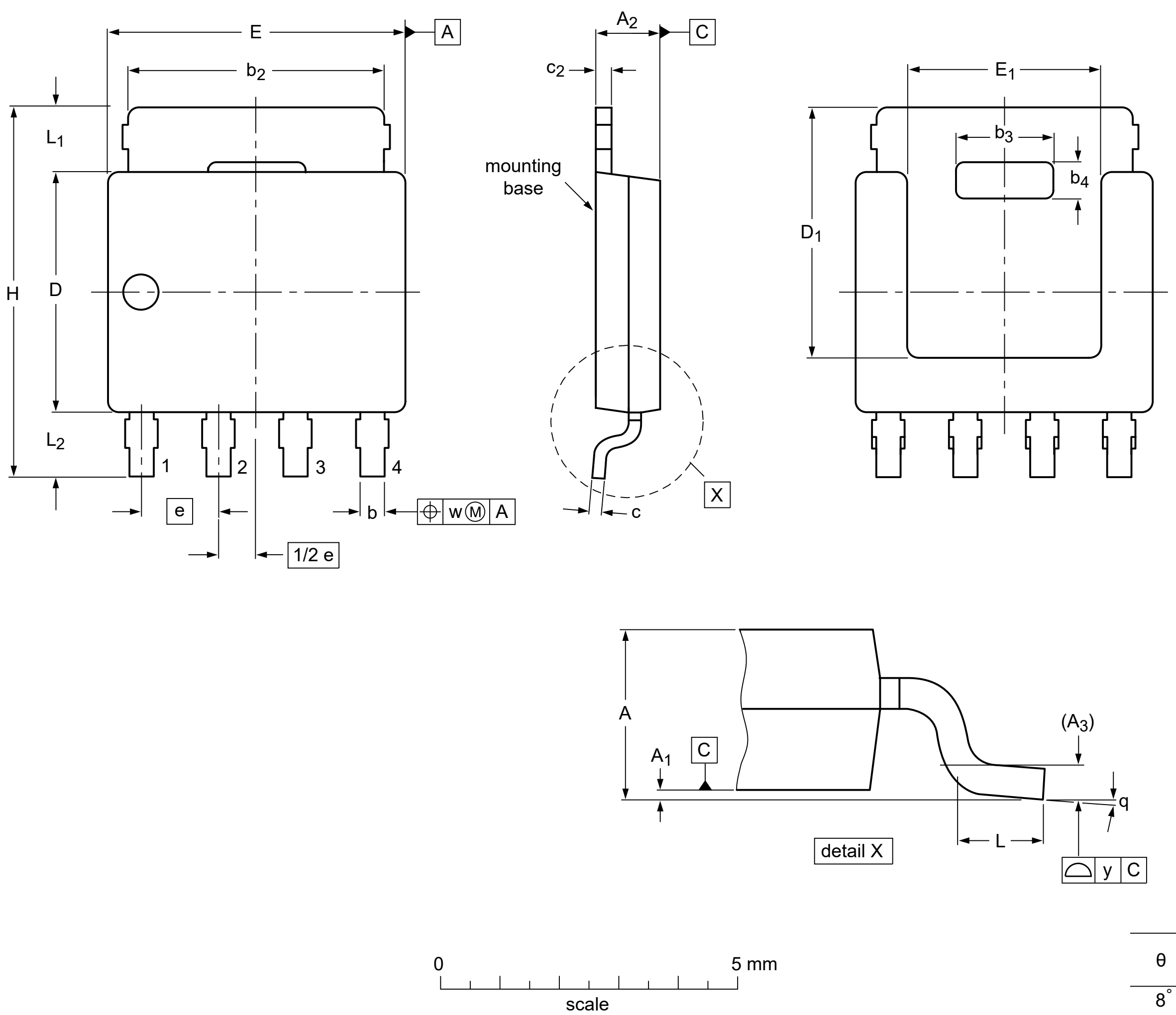


Fig. 17. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit(1)		A	A1	A2	A3	b	b2	b3	b4	c	c2	D(1)	D1(1)	E(1)	E1(1)	e	H	L	L1	L2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 18. Package outline LFPAK56; Power-SO8 (SOT669)

12. Soldering

Footprint information for reflow soldering **SOT669**

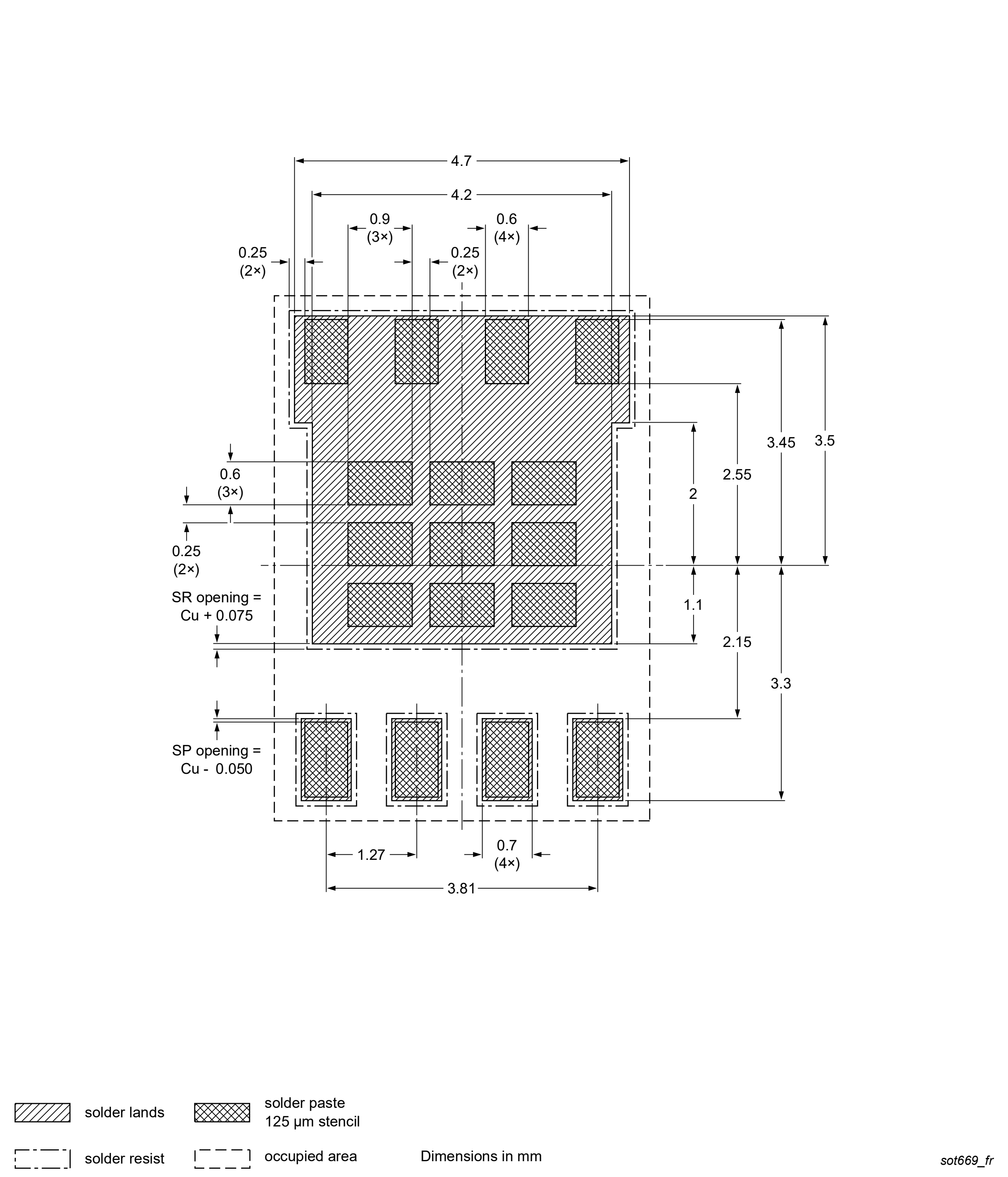


Fig. 19. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package **SOT669**

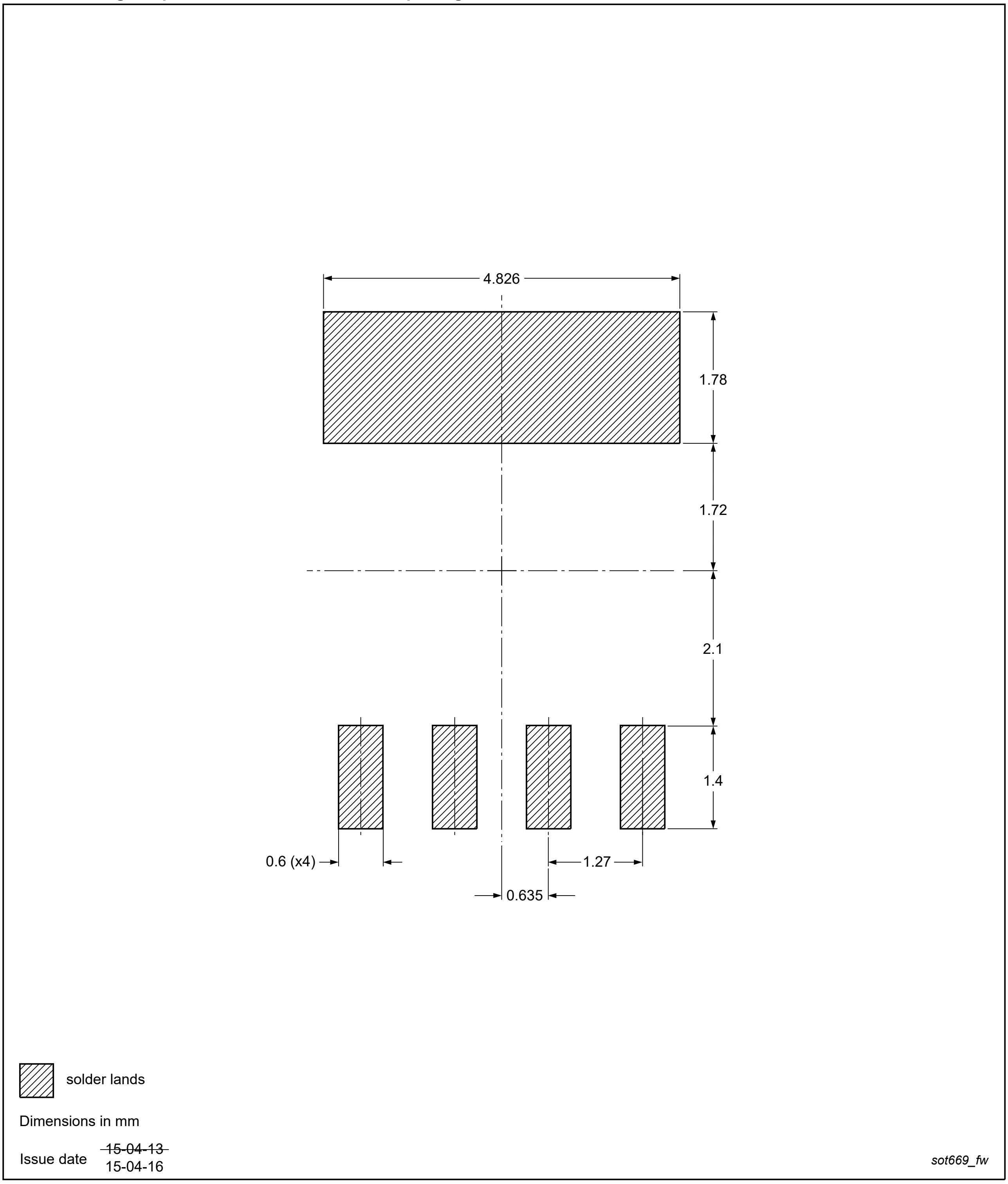


Fig. 20. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 1 May 2020