BUK9Y7R6-40E

N-channel 40 V, 7.6 mΩ logic level MOSFET in LFPAK56

7 May 2013 Product data sheet

1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 1		-	-	79	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	-	95	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A; T_j = 25 °C; Fig. 11		-	6.4	7.6	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 5 V; I_D = 20 A; V_{DS} = 32 V; T_j = 25 °C; Fig. 13; Fig. 14		-	5.5	-	nC

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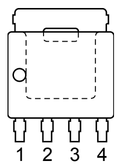
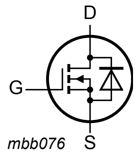
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y7R6-40E	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y7R6-40E	97E640

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage	T_j ≤ 175 °C; DC		-10	10	V
		T_j ≤ 175 °C; Pulsed	[1][2]	-15	15	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 5 V; Fig. 1		-	79	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Fig. 1		-	56	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Fig. 4		-	315	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	95	W

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	79	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	315	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 79 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3	[3][4]	-	43	mJ

[1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
[2] Significantly longer life times are achieved by lowering T_j and or V_{GS}
[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[4] Refer to application note AN10273 for further information.

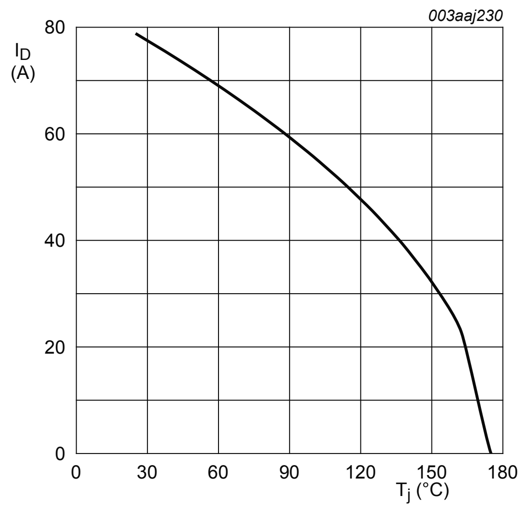


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5V$$

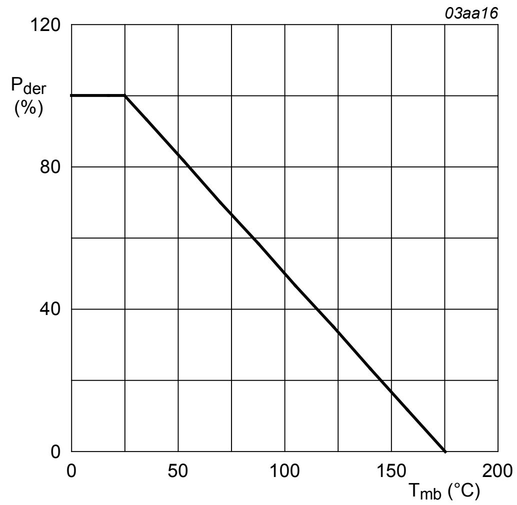


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

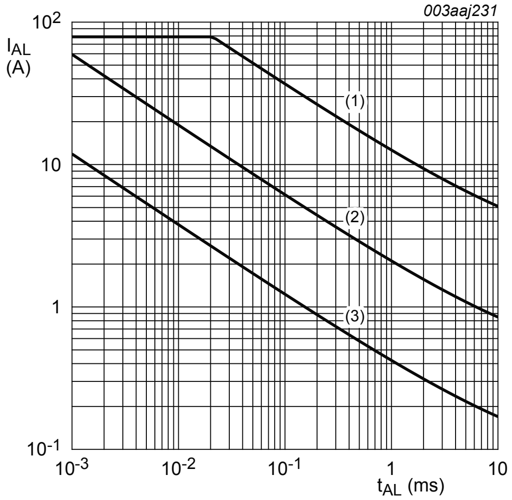


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 150°C$; (3) Repetitive Avalanche

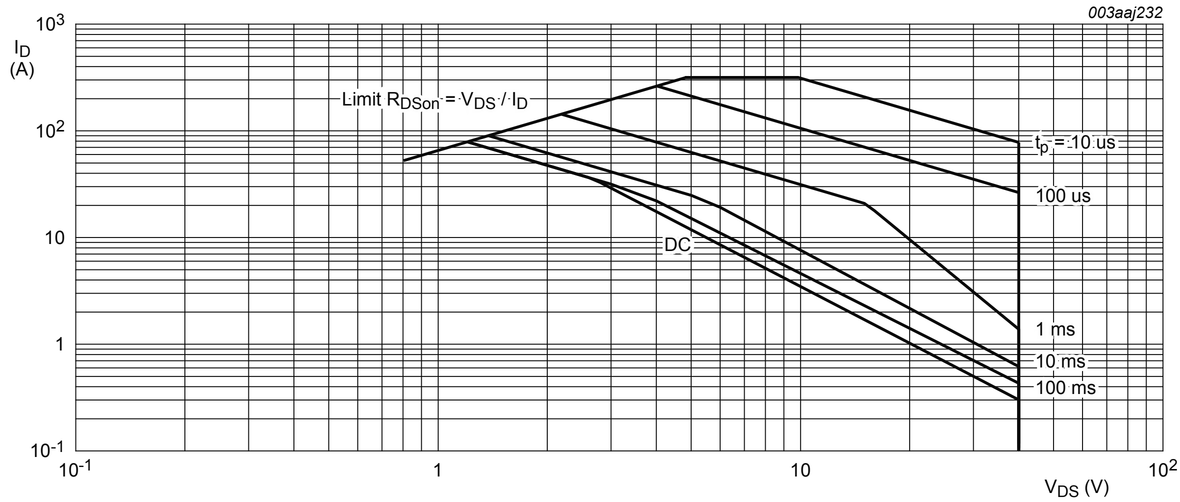


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C$; I_{DM} *is a single pulse*

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	1.58	K/W

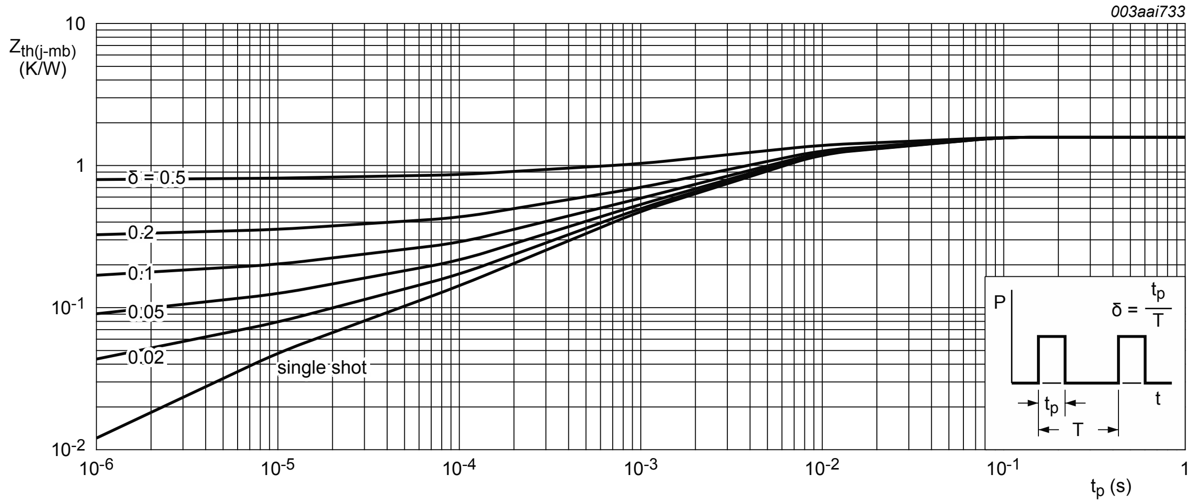


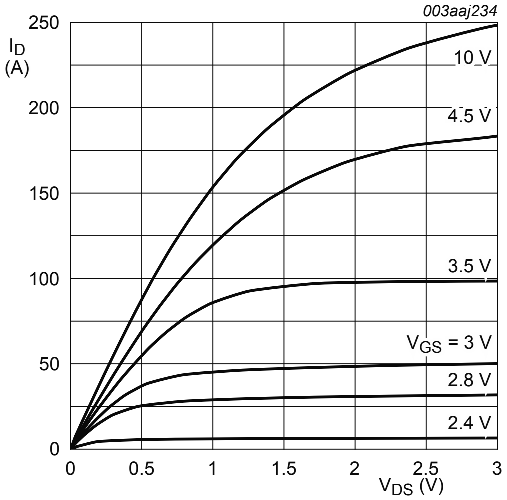
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 9		-	-	2.45	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 9		0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.04	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A; T_j = 25 °C; Fig. 11		-	6.4	7.6	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 11		-	5.3	6	mΩ
		V_{GS} = 5 V; I_D = 20 A; T_j = 175 °C; Fig. 11; Fig. 12		-	-	15.28	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 32 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 13; Fig. 14		-	16.4	-	nC
Q_{GS}	gate-source charge			-	5.1	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GD}	gate-drain charge			-	5.5	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	1807	2403	pF
C_{oss}	output capacitance			-	260	312	pF
C_{rss}	reverse transfer capacitance			-	126	173	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.5 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	11.3	-	ns
t_r	rise time			-	20.9	-	ns
$t_{d(off)}$	turn-off delay time			-	22.7	-	ns
t_f	fall time			-	16.6	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16		-	0.84	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C		-	17	-	ns
Q_r	recovered charge			-	8.1	-	nC



T_j = 25 °C; t_p = 300 µs

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

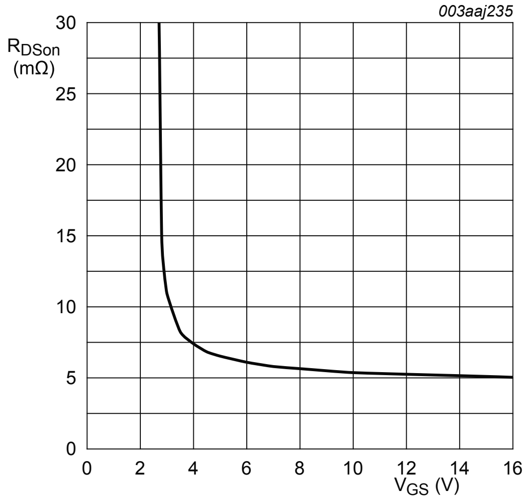


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C; I_D = 20A$

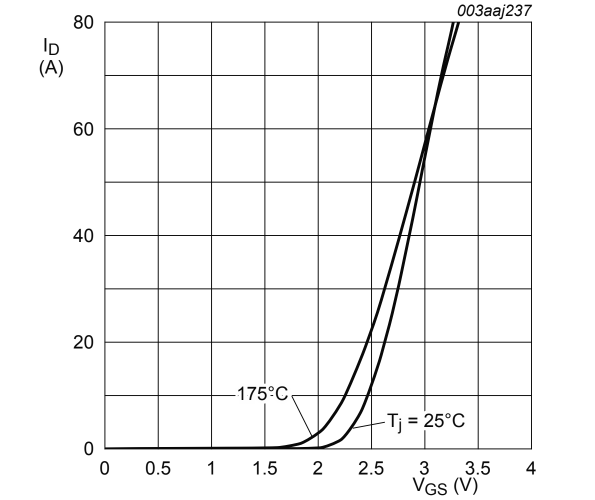


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10 V$

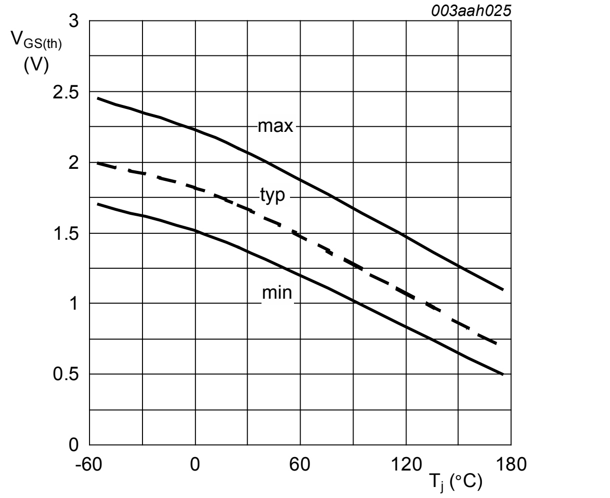


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1$ mA; $V_{DS} = V_{GS}$

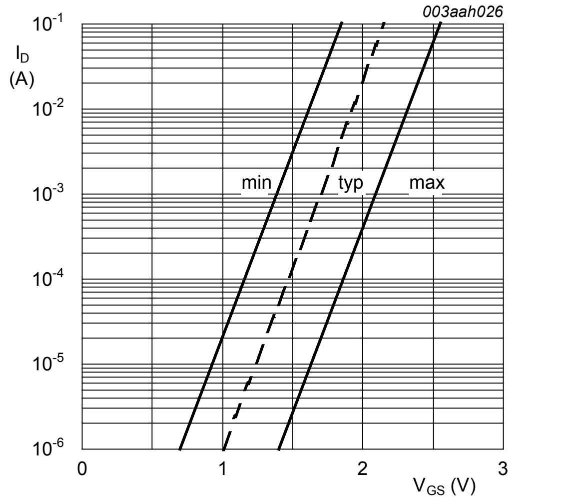
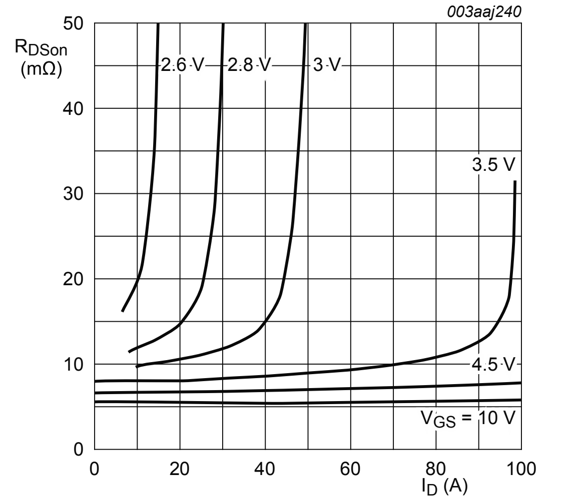


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25°C$; $V_{DS} = 5 V$



T_j = 25 °C; t_p = 300 μs

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

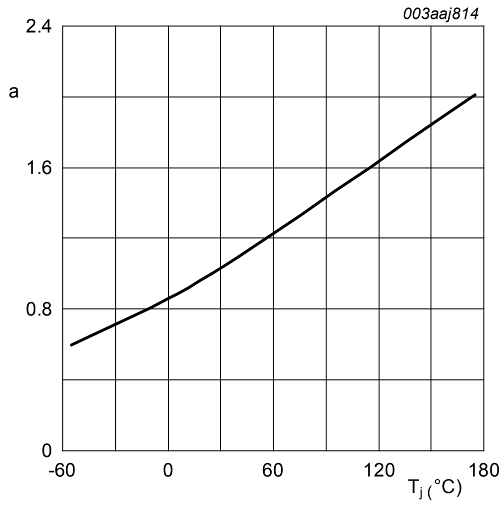


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

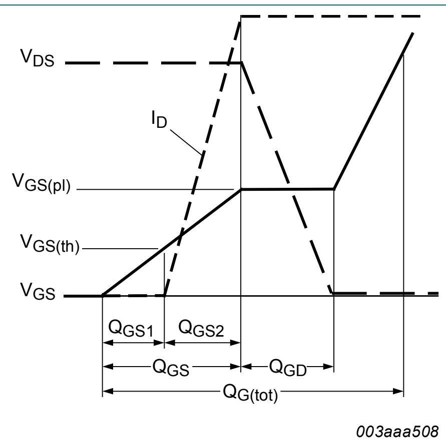


Fig. 13. Gate charge waveform definitions

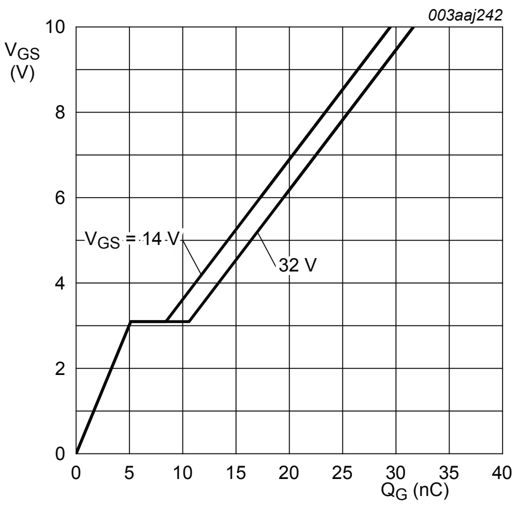


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25°C;\ I_D = 20A$$

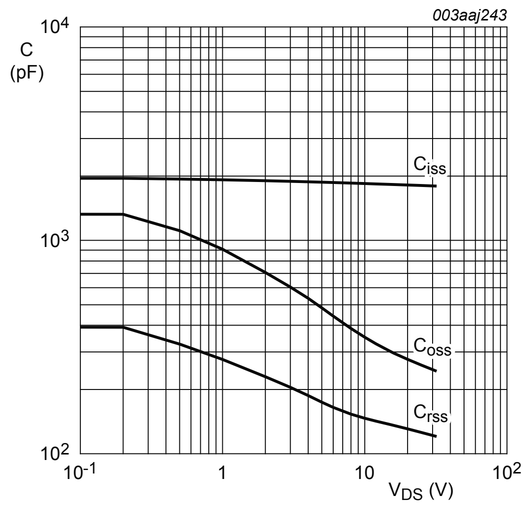


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V;\ f = 1MHz$$

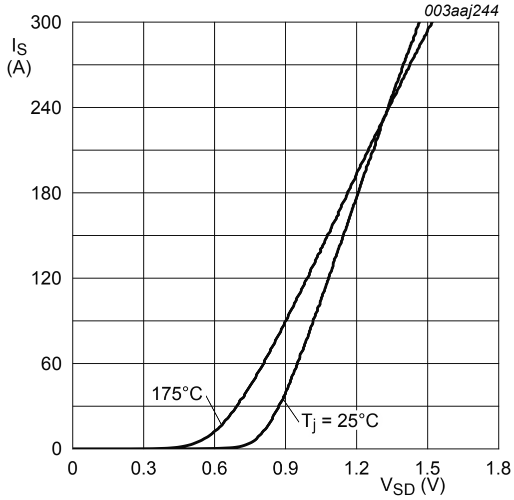
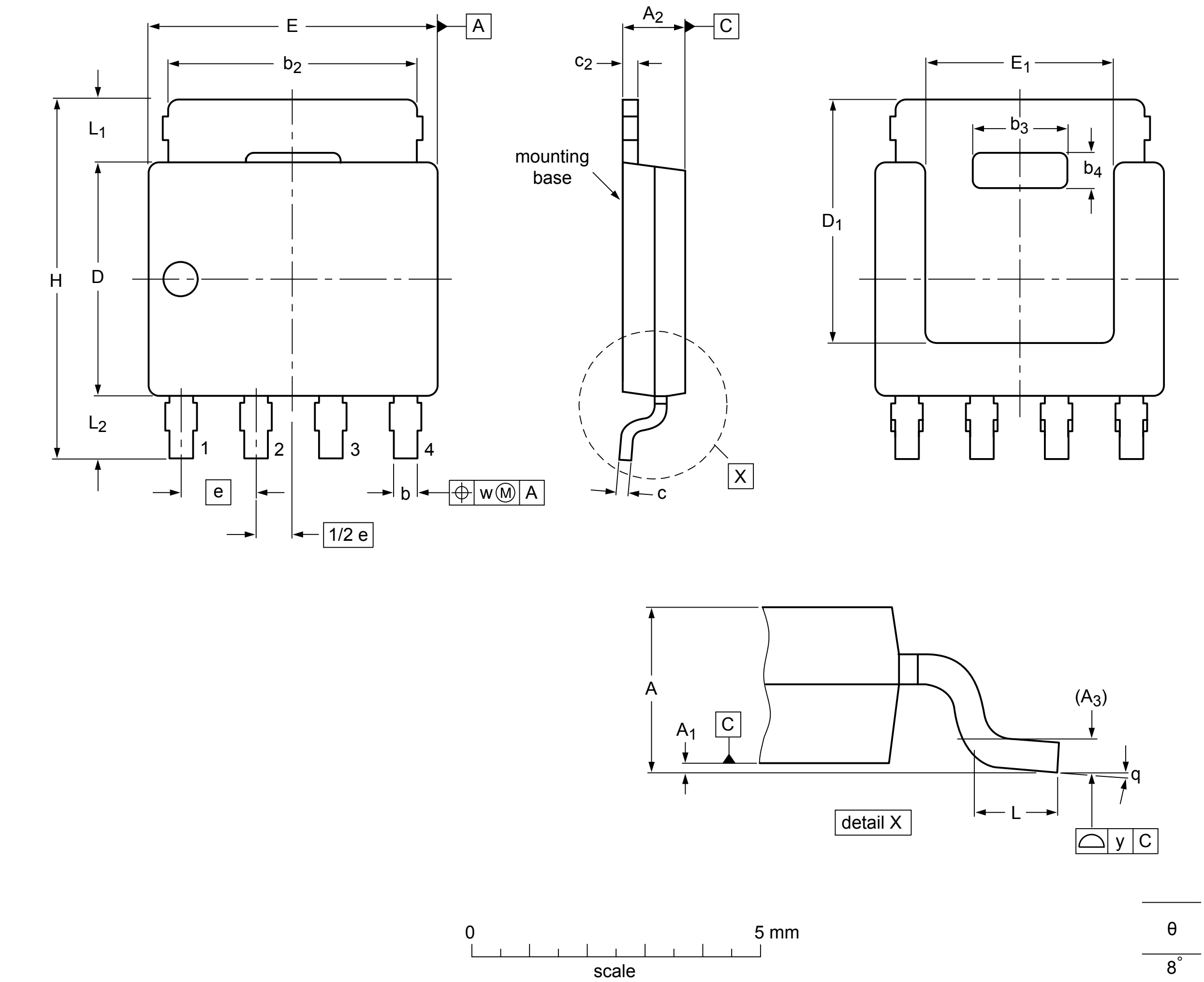


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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