

N-channel 80 V, 8.5 mΩ logic level MOSFET in LFPAK56 8 May 2013 Product data sheet

### 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

### 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V<sub>GS(th)</sub> rating of greater than 0.5 V at 175 °C

### 3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

### 4. Quick reference data

Table 1. Qui	ck reference data						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	80	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	[1]	-	-	100	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	238	W
Static characte	eristics	·			- 1		
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>		-	6.3	8.5	mΩ
Dynamic characteristics							
Q <sub>GD</sub>	gate-drain charge	$V_{GS} = 5 V; I_D = 25 A; V_{DS} = 64 V;$ T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>		-	17.1	-	nC

[1] Continuous current is limited by package.

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### 5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	q	G-UFT4
4	G	gate	មុប្បូប្	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

# 6. Ordering information

Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
BUK9Y8R5-80E	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669			

# 7. Marking

Table 4. Marking codes	
Type number	Marking code
BUK9Y8R5-80E	98E580

# 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	80	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ		-	80	V
V <sub>GS</sub>	gate-source voltage	T <sub>j</sub> ≤ 175 °C; DC		-10	10	V
		$T_j \le 175 \ ^{\circ}C; Pulsed$	[1][2]	-15	15	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; <u>Fig. 1</u>	<u>[3]</u>	-	100	А
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; <u>Fig. 1</u>	[3]	-	75	А
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \ \mu$ s; Fig. 4		-	423	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	238	W

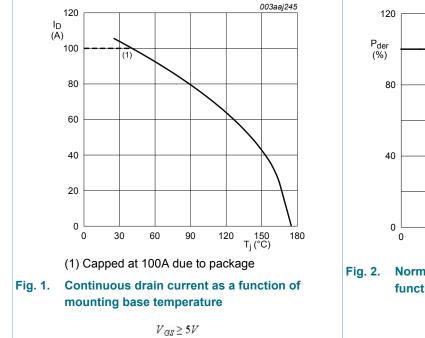
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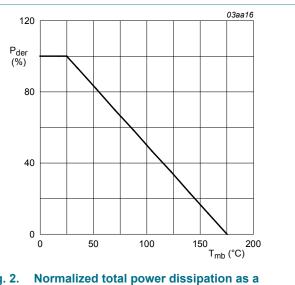
# **BUK9Y8R5-80E**

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Symbol	Parameter	Conditions		Min	Мах	Unit
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drai	n diode					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[3]	-	100	А
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^\circ C$		-	423	А
Avalanche r	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\begin{split} & {\sf I}_{\sf D} = 100 \; {\sf A};  {\sf V}_{\sf sup} \le 80 \; {\sf V};  {\sf R}_{\sf GS} = 50 \; \Omega; \\ & {\sf V}_{\sf GS} = 5 \; {\sf V}; \; {\sf T}_{\sf j(init)} = 25 \; {\rm ^{\circ}C}; \; {\sf unclamped}; \\ & {\sf Fig. \; 3} \end{split}$	[4][5]	-	148	mJ

- Accumulated pulse duration up to 50 hours delivers zero defect ppm Significantly longer life times are achieved by lowering  $\rm T_{j}$  and or  $\rm V_{GS}$ [1]
- [2]
- Continuous current is limited by package. [3]
- Single-pulse avalanche rating limited by maximum junction temperature of 175 °C. Refer to application note AN10273 for further information. [4]
- [5]



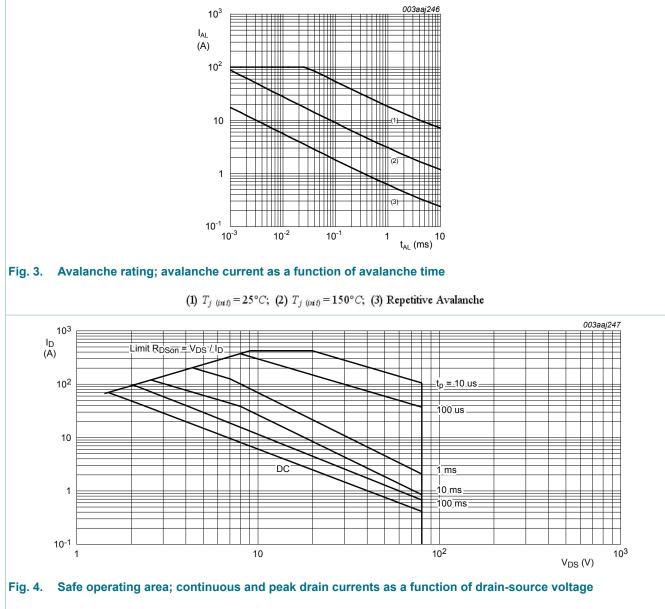


function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

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#### N-channel 80 V, 8.5 mΩ logic level MOSFET in LFPAK56

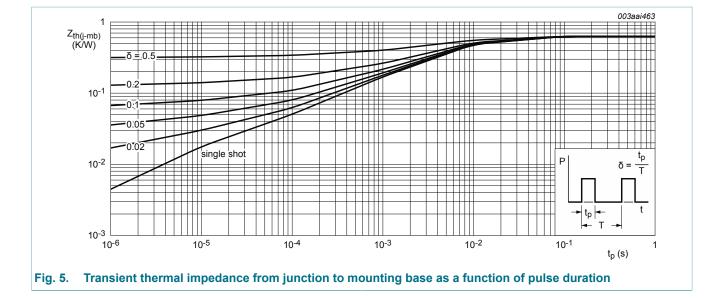


 $T_{mb} = 25^{\circ}C; \ I_{DM}$  is a single pulse

### 9. Thermal characteristics

Table 6. Th	ermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	-	0.63	K/W

#### N-channel 80 V, 8.5 mΩ logic level MOSFET in LFPAK56

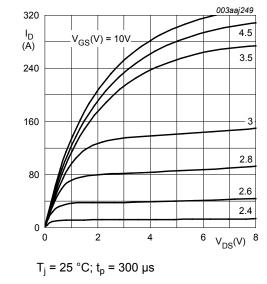


# **10. Characteristics**

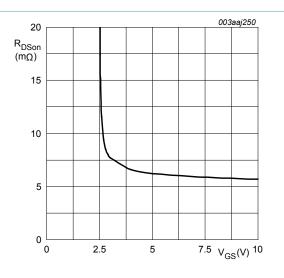
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics	· · · · ·	I			
V <sub>(BR)DSS</sub>	drain-source	$I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C	80	-	-	V
	breakdown voltage	$I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C	72	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	$V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C	-	0.07	10	μA
I <sub>DSS</sub>	drain leakage current	$V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	$V_{GS}$ = 10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
		$V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	6.3	8.5	mΩ
Doon	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; Fig. 11	-	5.8	8	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 11; Fig. 12	-	-	21.3	mΩ

#### N-channel 80 V, 8.5 mΩ logic level MOSFET in LFPAK56

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic cl	haracteristics	· · · · · ·				_
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 5 V;	-	54.7	-	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C; <u>Fig. 13; Fig. 14</u>	-	13.5	-	nC
Q <sub>GD</sub>	gate-drain charge		-	17.1	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz;	-	6125	8167	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	-	397	476	pF
C <sub>rss</sub>	reverse transfer capacitance		-	207	284	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 60 V; R <sub>L</sub> = 2.4 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C	-	28	-	ns
t <sub>r</sub>	rise time		-	50	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	82	-	ns
t <sub>f</sub>	fall time		-	45	-	ns
Source-dra	in diode		I			
V <sub>SD</sub>	source-drain voltage	$I_{S}$ = 25 A; $V_{GS}$ = 0 V; $T_{j}$ = 25 °C; <u>Fig. 16</u>	-	0.82	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_{\rm S}$ = 20 A; dI <sub>S</sub> /dt = -100 A/µs; V <sub>GS</sub> = 0 V;	-	30.9	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C	-	36.3	-	nC







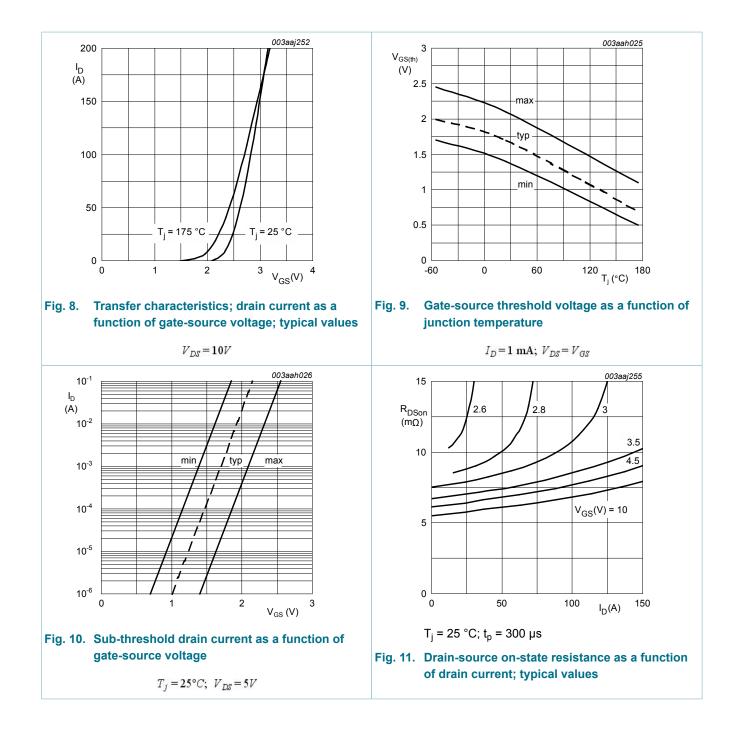


 $T_j = 25^{\circ}C; \ I_D = 25A$ 

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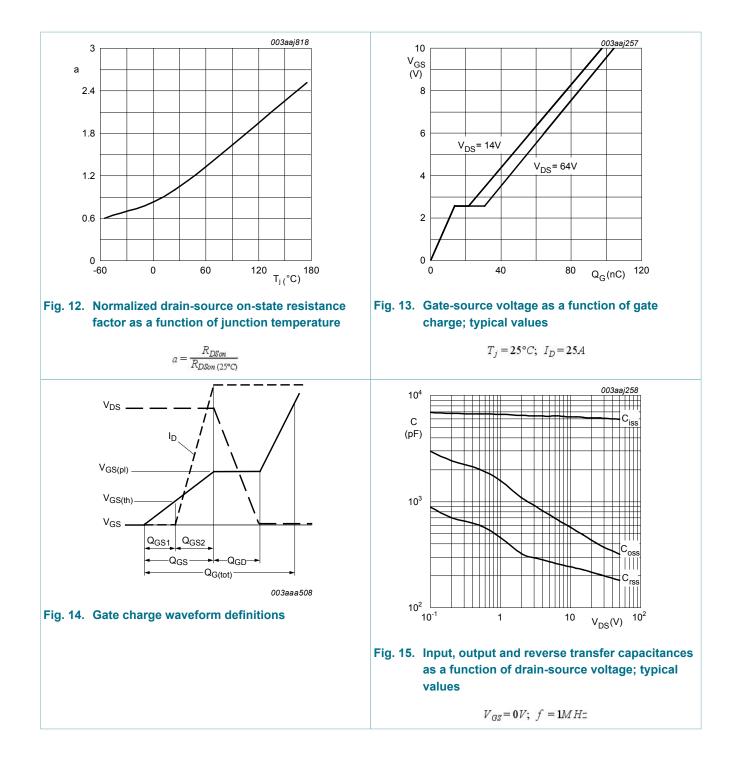


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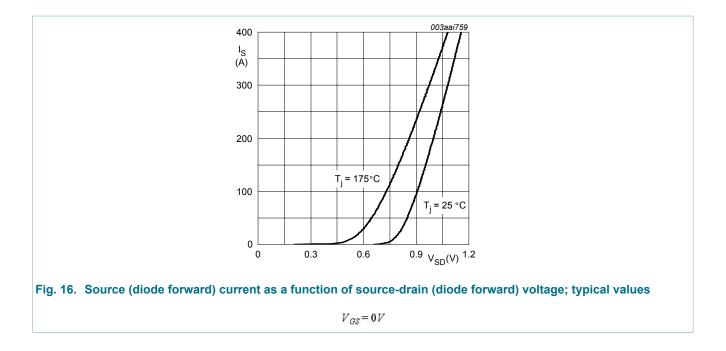
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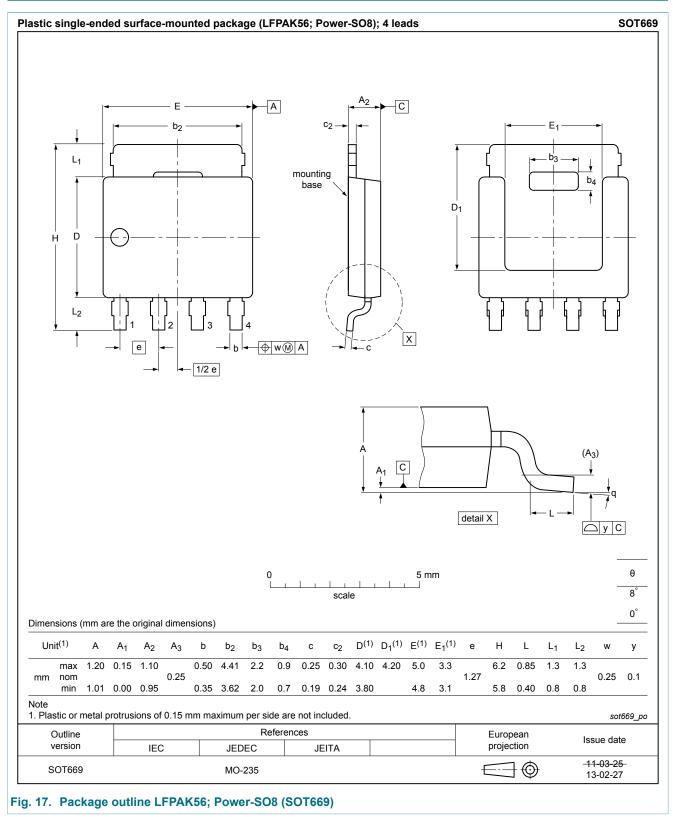
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#### N-channel 80 V, 8.5 mΩ logic level MOSFET in LFPAK56

### **11. Package outline**



#### N-channel 80 V, 8.5 m $\Omega$ logic level MOSFET in LFPAK56

### 12. Legal information

#### 12.1 Data sheet status

Document status [1][2]	Product status [ <u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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#### N-channel 80 V, 8.5 mΩ logic level MOSFET in LFPAK56

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	Features and benefits

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