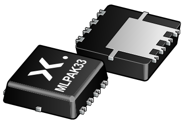


BXK9Q29-60E

60 V, N-channel Trench MOSFET

19 May 2024 Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT8002-3 (MLPAK33) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- Fully automotive qualified to AEC-Q101 at 175°C
- Side-wettable flanks for optical solder inspection

3. Applications

- LED Lighting
- Switching circuits
- DC-DC conversion

4. Quick reference data

Table 1. Quick reference data

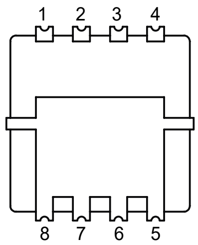
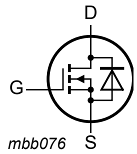
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	60	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	[1]	-	-	21	A
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	-	27	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.6 A; T_j = 25 °C		-	23.7	29	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{DS} = 30 V; I_D = 5.6 A; V_{GS} = 10 V; T_j = 25 °C		-	2.4	-	nC

[1] 21 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-3)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BXK9Q29-60E	MLPAK33	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BXK9Q29-60E	7AA

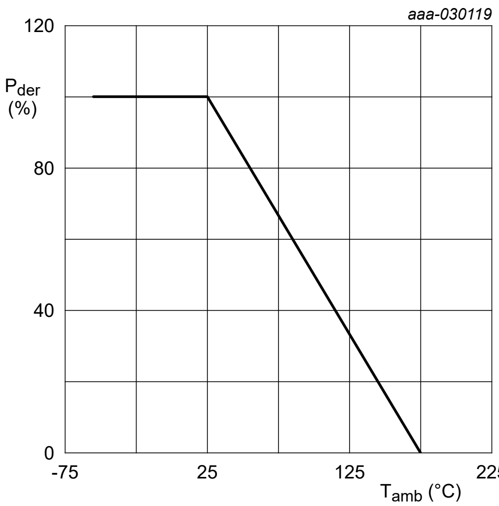
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

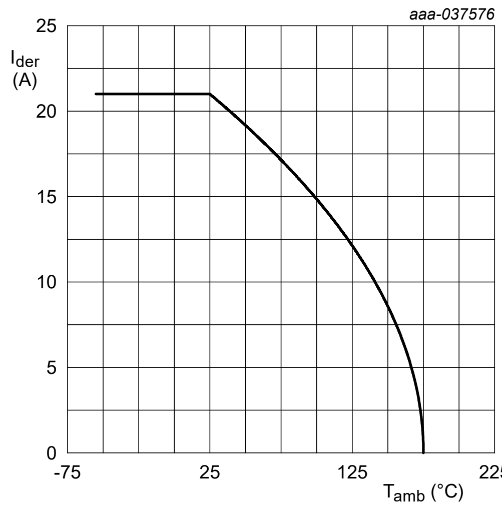
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	60	V
V_{GS}	gate-source voltage	DC; T_j ≤ 175 °C		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	[1]	-	21	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	14.5	A
I_{DM}	peak drain current	single pulse; t_p ≤ 10 µs; T_{mb} = 25 °C		-	84	A
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	27	W
T_j	junction temperature			-55	175	°C
T_{stg}	storage temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	21	A
I_{SM}	peak source current	single pulse; t_p ≤ 10 µs; T_{mb} = 25 °C	[1]	-	84	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{sup} < 60 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; I_D = 15.8 A; unclamped	[2] [3]	-	25	mJ
I_{AS}	non-repetitive avalanche current	$T_{j(init)}$ = 25 °C	[4]	-	15.8	A

[1] 21 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Protected by 100% test.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100 \ \%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100 \ \%$$

21 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of ambient temperature

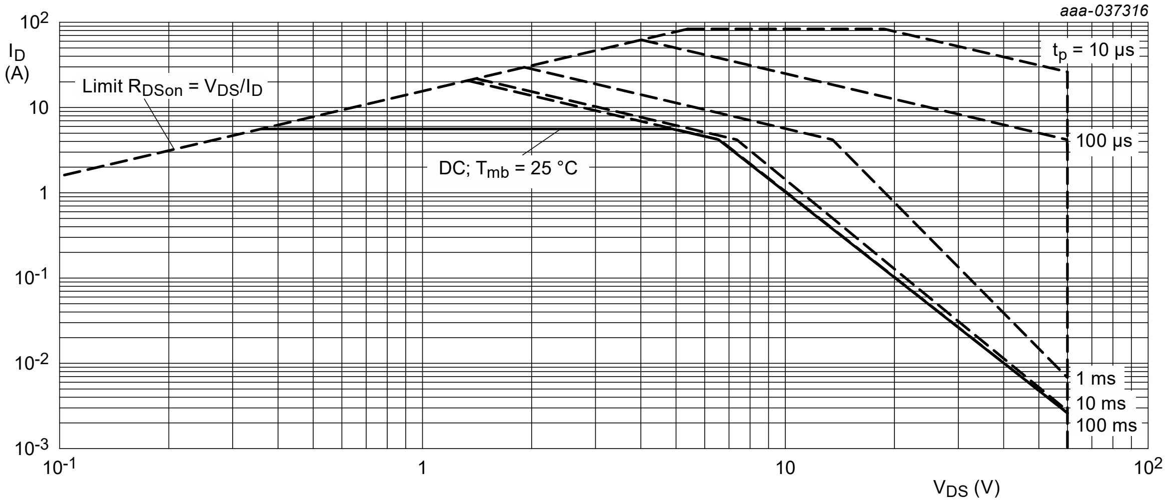
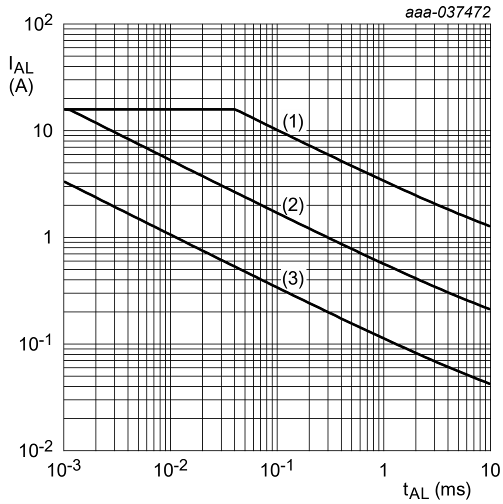


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage



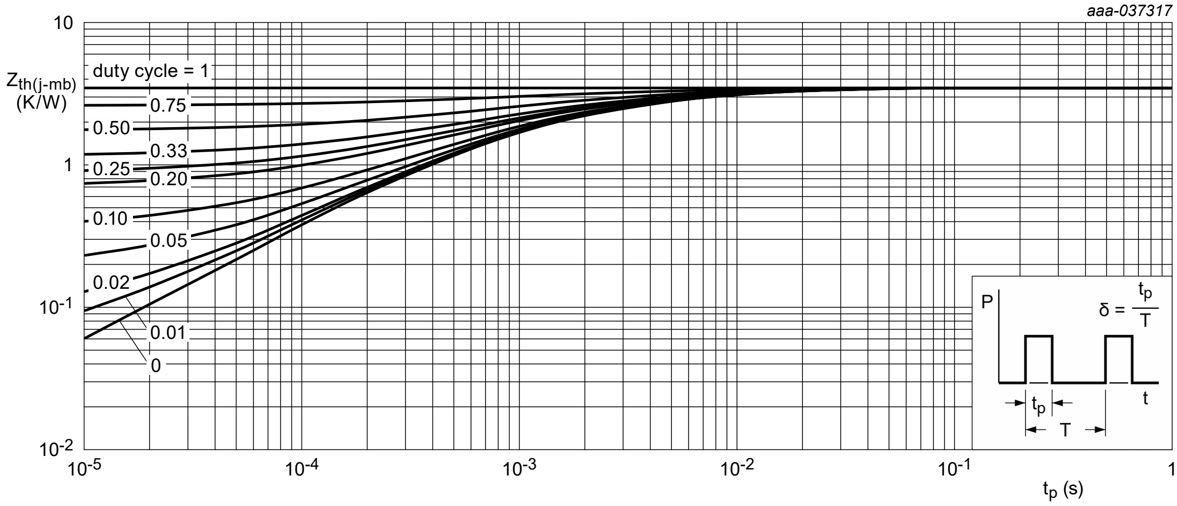
(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	3.5	5.5	K/W



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		60	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C		1.3	1.7	2.1	V
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C		-	-	20	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 °C		-	-	400	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	0.1	µA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-0.1	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.6 A; T_j = 25 °C		-	23.7	29	mΩ
		V_{GS} = 10 V; I_D = 5.6 A; T_j = 105 °C		-	39	51.4	mΩ
		V_{GS} = 10 V; I_D = 5.6 A; T_j = 125 °C		-	42.4	55.9	mΩ
		V_{GS} = 10 V; I_D = 5.6 A; T_j = 175 °C		-	52	64	mΩ
		V_{GS} = 4.5 V; I_D = 4.9 A; T_j = 25 °C		-	28	38	mΩ
		V_{GS} = 4.5 V; I_D = 4.9 A; T_j = 105 °C		-	45.3	63.9	mΩ
		V_{GS} = 4.5 V; I_D = 4.9 A; T_j = 125 °C		-	49.2	69.5	mΩ
		V_{GS} = 4.5 V; I_D = 4.9 A; T_j = 175 °C		-	60.9	83.6	mΩ
g_{fs}	forward transconductance	V_{DS} = 5 V; I_D = 5.6 A		-	18.6	-	S
R_G	gate resistance	f = 1 MHz		-	2	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = 30 V; I_D = 5.6 A; V_{GS} = 10 V; T_j = 25 °C		-	12	18	nC
Q_{GS}	gate-source charge			-	1.6	-	nC
Q_{GD}	gate-drain charge			-	2.4	-	nC
C_{iss}	input capacitance	V_{DS} = 30 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	660	-	pF
C_{oss}	output capacitance			-	67	-	pF
C_{rss}	reverse transfer capacitance			-	40	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; I_D = 5.6 A; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	3	-	ns
t_r	rise time			-	4	-	ns
$t_{d(off)}$	turn-off delay time			-	13	-	ns
t_f	fall time			-	5	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 2.5 A; V_{GS} = 0 V; T_j = 25 °C		-	0.8	1	V
t_{rr}	reverse recovery time	I_S = 2.5 A; dI_S/dt = -100 A/µs; V_{GS} = 10 V; V_{DS} = 30 V; T_j = 25 °C		-	13	-	ns
Q_r	recovered charge			-	7	-	nC

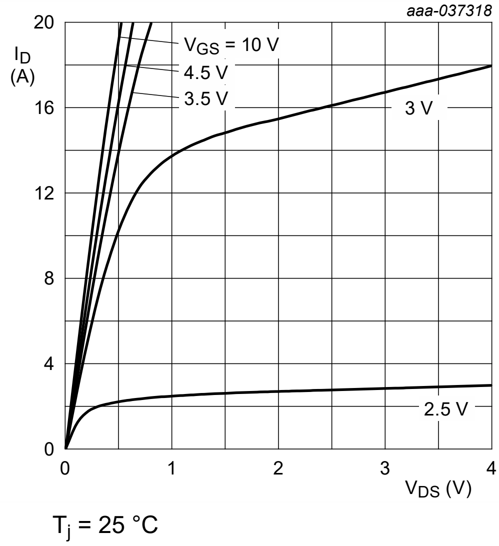


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

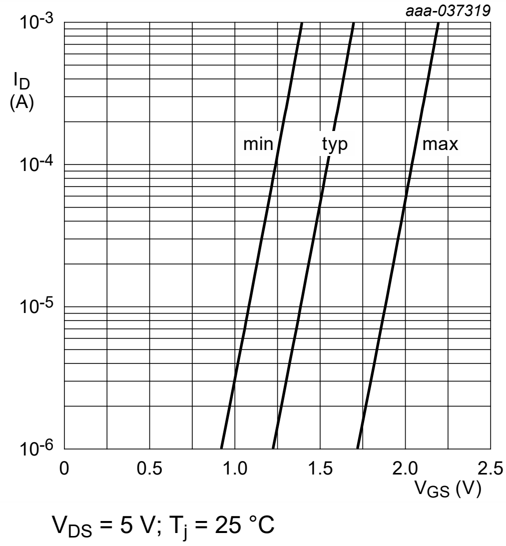


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

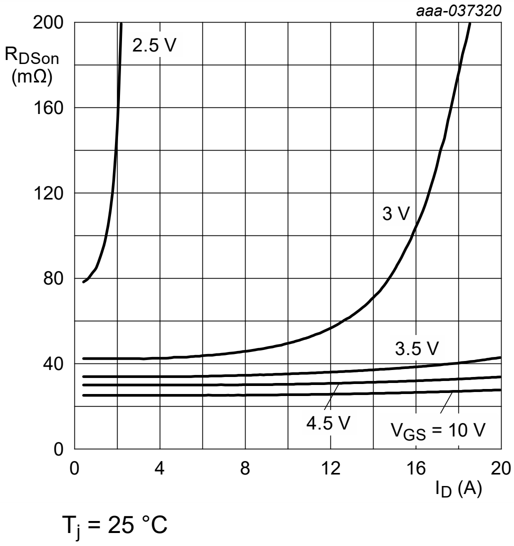


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

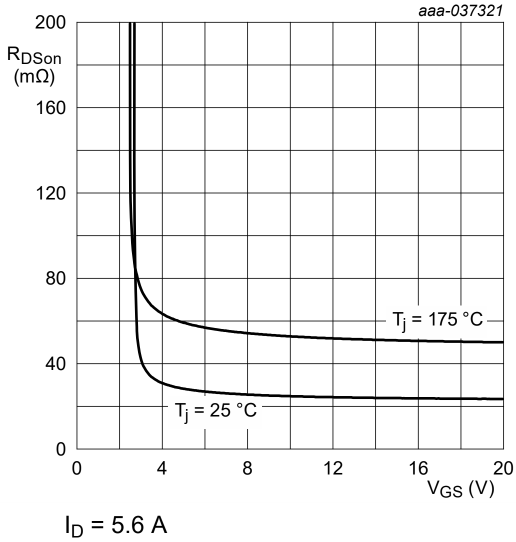
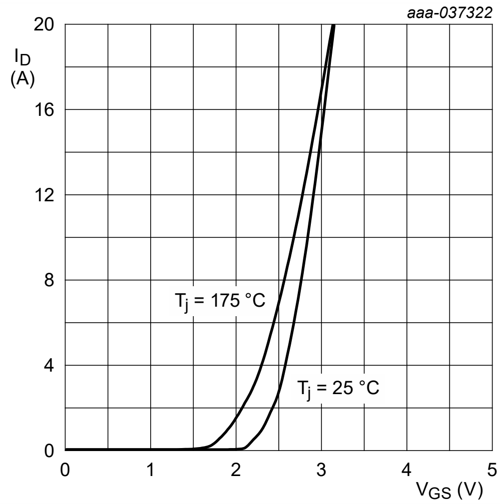
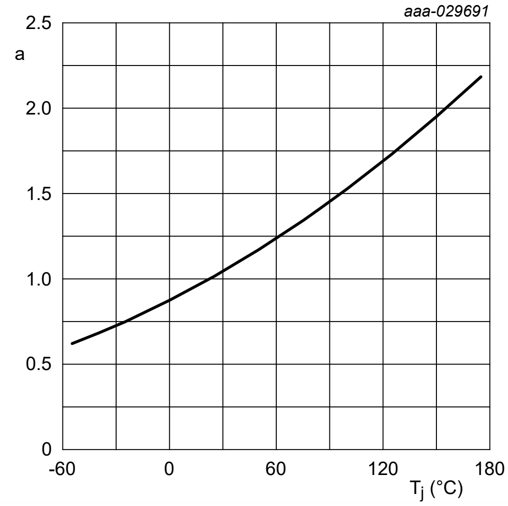


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



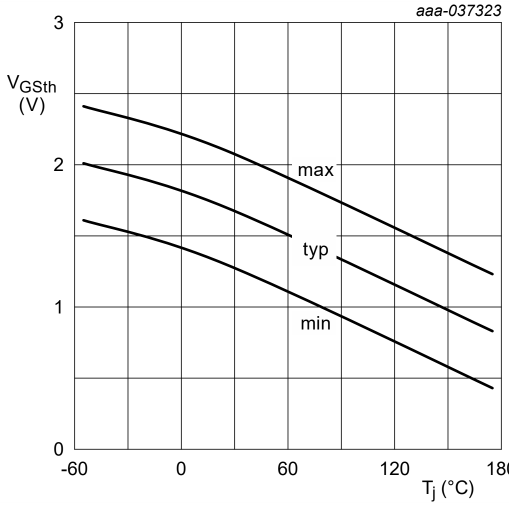
V_{DS} = 2 V

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



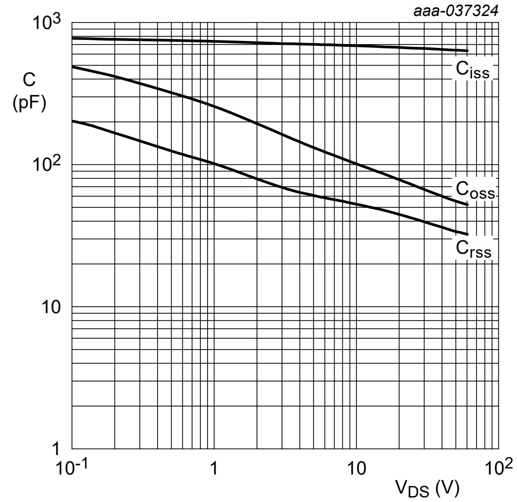
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



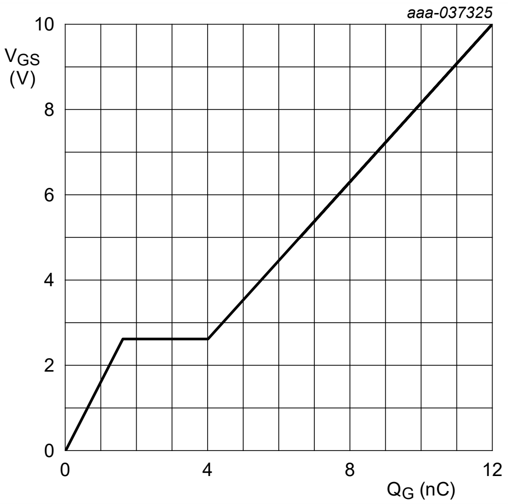
I_D = 250 µA; V_{DS} = V_{GS}

Fig. 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = 5.6 A; V_{DS} = 30 V; T_{amb} = 25 °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

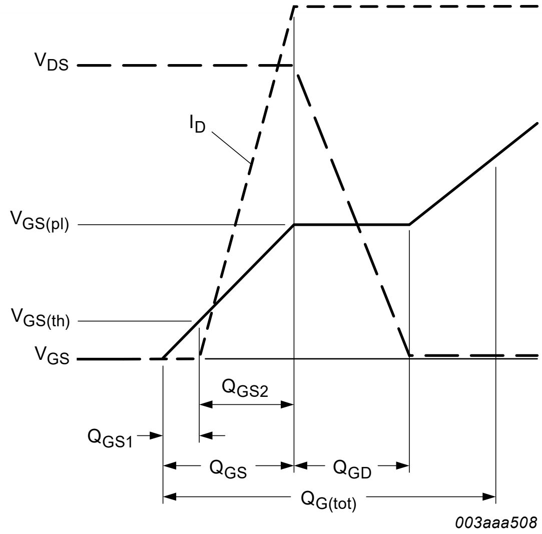
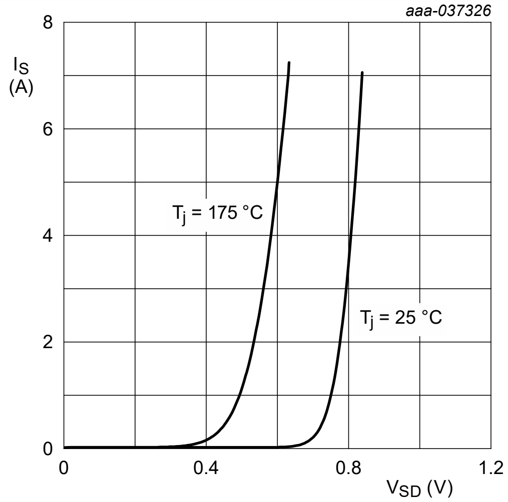


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

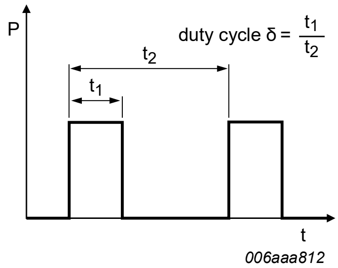


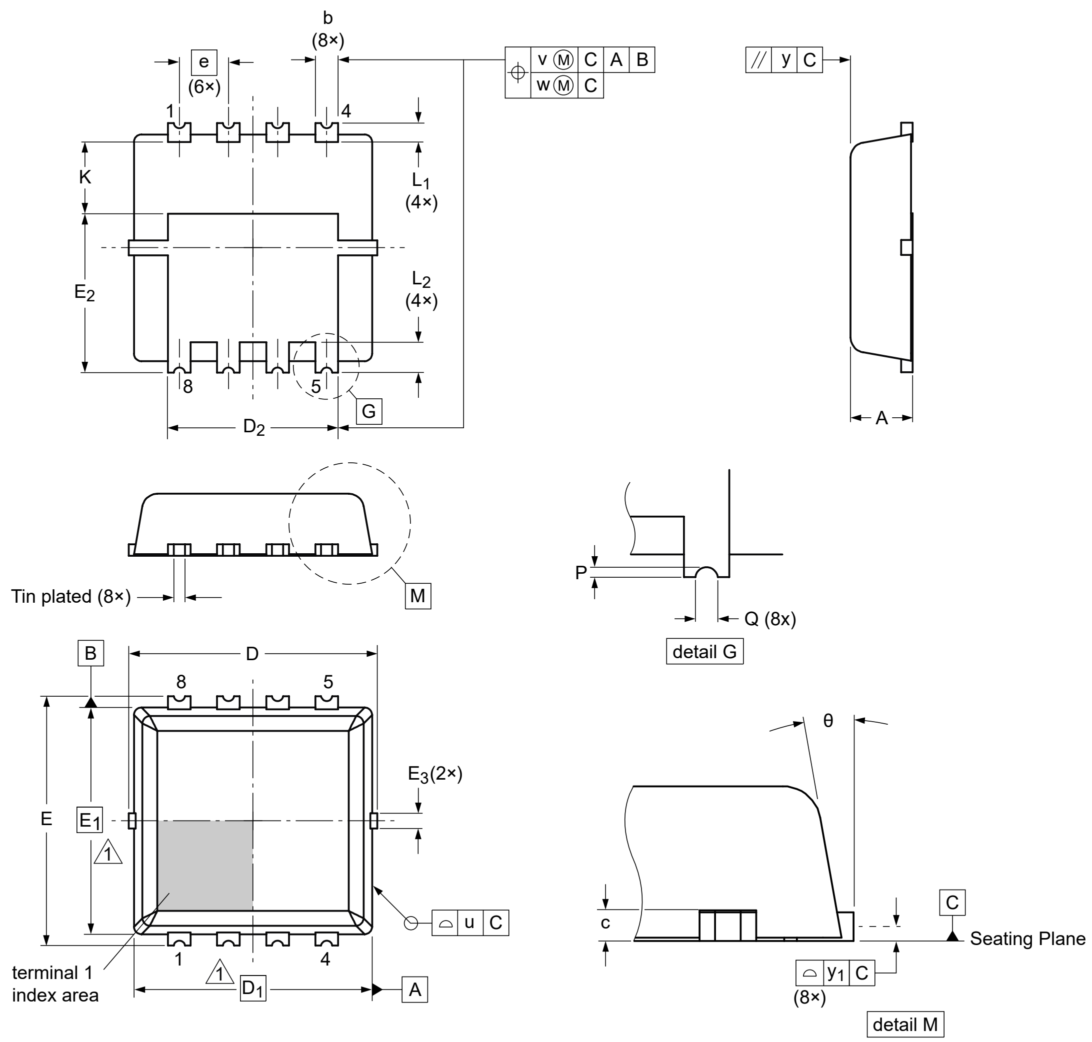
Fig. 17. Duty cycle definition

Quality information

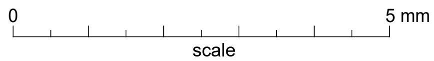
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

MLPAK33: plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body **SOT8002-3**



⚠1 Dimensions do not include mold flash, protrusions of gate burrs, mold flash, tie bar protrusion or tie bar flash. Mold flash shall not be greater than 0.05 mm



Dimensions (mm are the original dimensions)

Unit		A	b	c	D	D1	D2	e	E	E1	E2	E3	K	L1	L2	P	Q	θ	y	y1	u	v	w
mm	max	0.90	0.40	0.18	3.40	3.15 BSC	2.35	0.65 BSC	3.40	3.0 BSC	2.20	0.2 REF	0.95 REF	0.40	0.55	0.1 REF	0.15 REF	12°	0.05	0.05	0.1	0.1	0.05
	nom	0.80	0.32	0.15	3.30		2.25		3.30		2.10			0.25	0.40			10°					
	min	0.70	0.25	0.12	3.20		2.15		3.20		2.00			0.10	0.25			8°					

sot8002-3_po

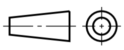
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8002-3						23-07-21

Fig. 18. Package outline MLPAK33 (SOT8002-3)

13. Soldering

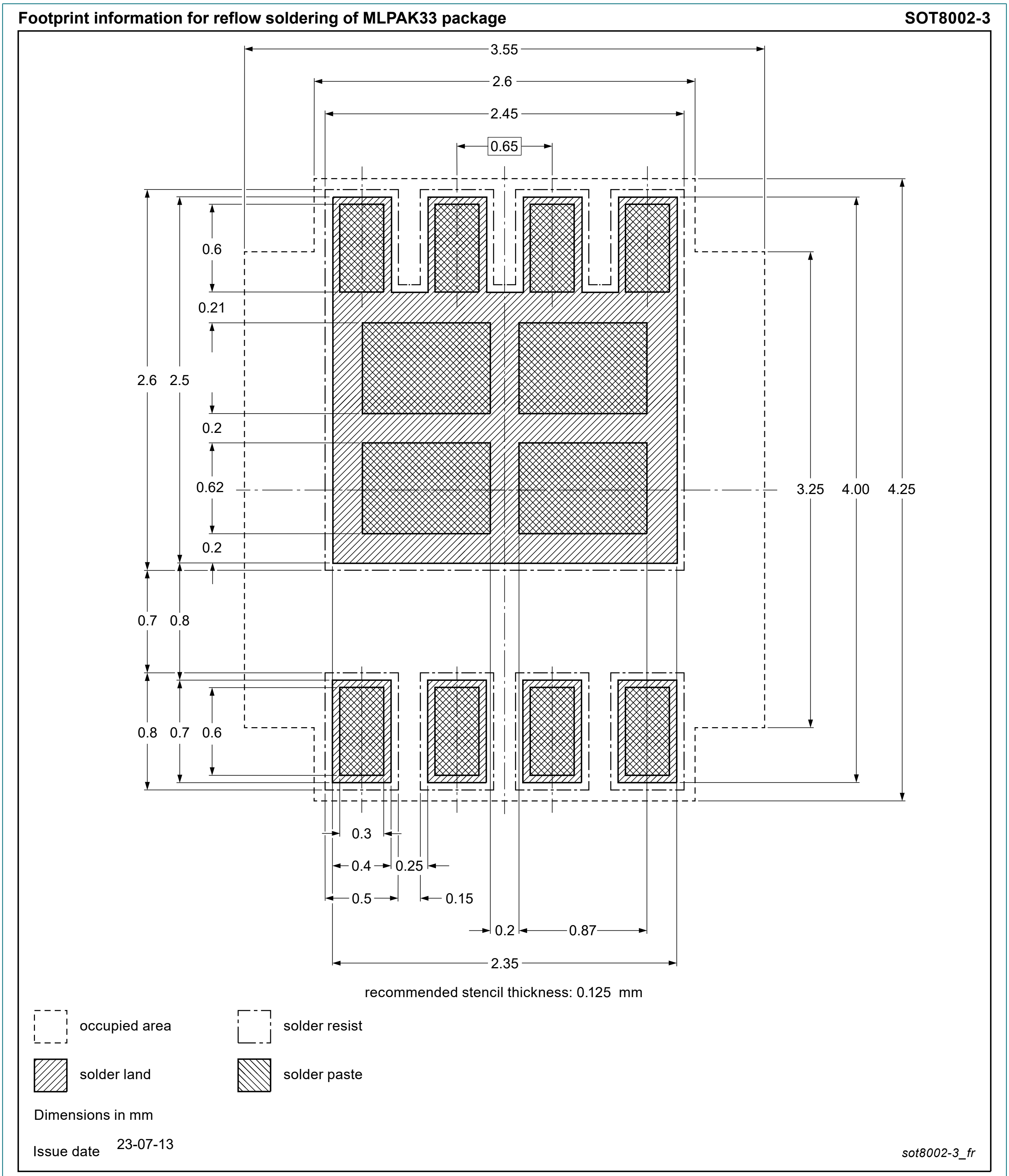


Fig. 19. Reflow soldering footprint for MLPAK33 (SOT8002-3)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BXK9Q29-60E v.1	20240519	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Contents

Date of release: 19 May 2024