HEF4053B-Q100

Triple single-pole double-throw analog switch

Rev. 3 — 21 December 2021 Product data sheet

1. General description

The HEF4053B-Q100 is a triple single-pole double-throw analog switch (3x SPDT) suitable for use in analog or digital 2:1 multiplexer/demultiplexer applications. Each switch features a digital select input (Sn), two independent inputs/outputs (Y0 and Y1) and a common input/output (Z). A digital enable input ($\overline{E}$) is common to all switches. When $\overline{E}$ is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Complies with JEDEC standard JESD 13-B

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4053BT-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4053BTT-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

nexperia

5. Functional diagram

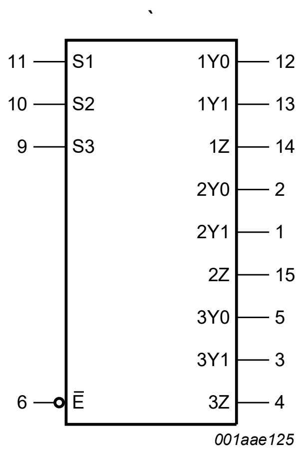


Fig. 1. Logic symbol

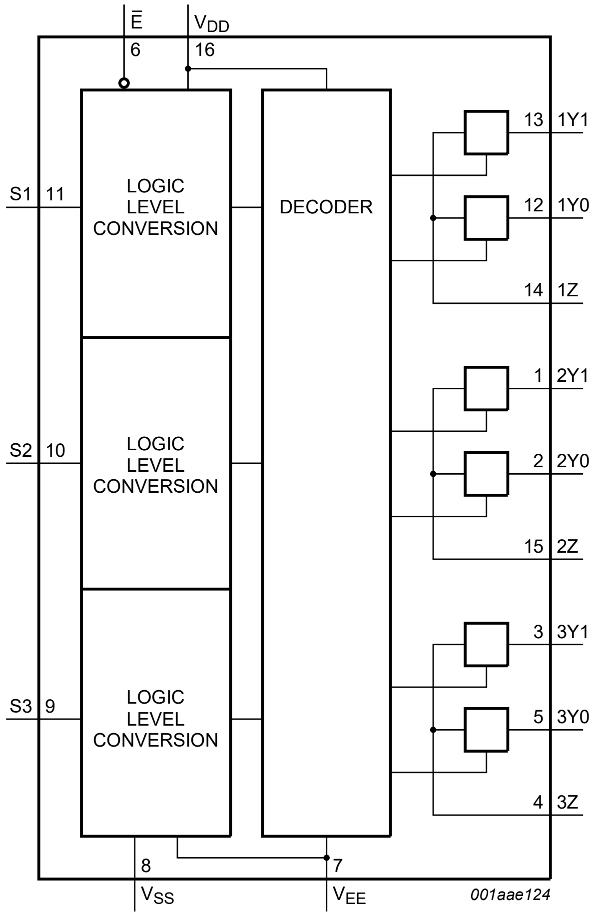


Fig. 2. Functional diagram

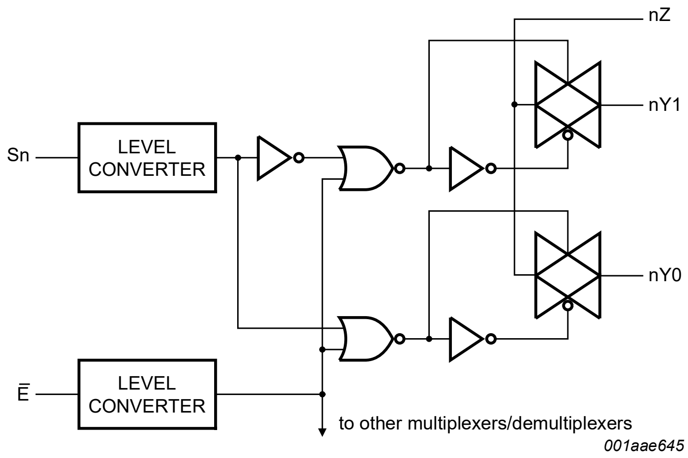


Fig. 3. Logic diagram (one multiplexer/demultiplexer)

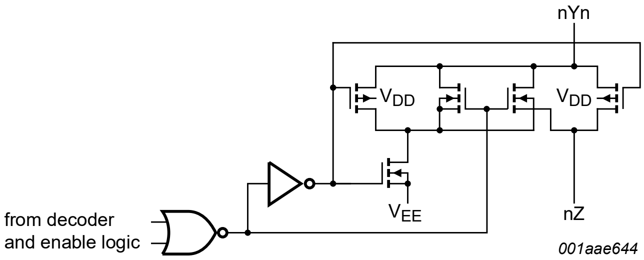


Fig. 4. Schematic diagram (one switch)

6. Pinning information

6.1. Pinning

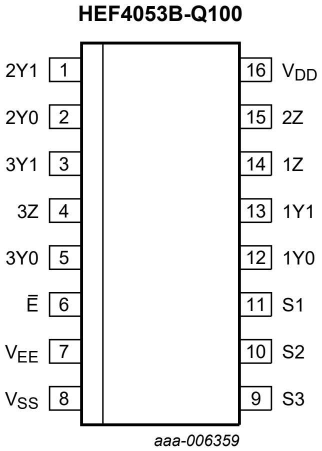


Fig. 5. Pin configuration for SOT109-1 (SO16)

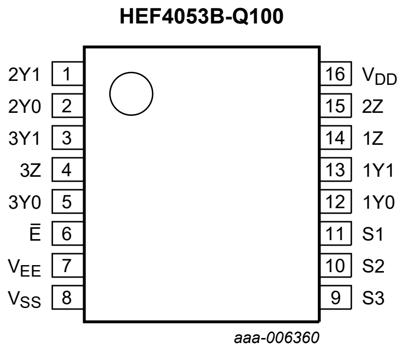


Fig. 6. Pin configuration for SOT403-1 (TSSOP16)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	supply voltage
V_{SS}	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
1Y0, 2Y0, 3Y0	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	13, 1, 3	independent input or output
1Z, 2Z, 3Z	14, 15, 4	independent output or input
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs		Channel on
$\overline{E}$	Sn	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches OFF

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+18	V
V_{EE}	supply voltage	referenced to V_{DD}	[1]	-18	+0.5	V
I_{IK}	input clamping current	pins Sn and $\overline{E}$; V_I < -0.5 V or V_I > V_{DD} + 0.5 V		-	±10	mA
V_I	input voltage			-0.5	V_{DD} + 0.5	V
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			-65	+150	°C
T_{amb}	ambient temperature			-40	+125	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	see Fig. 7	3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

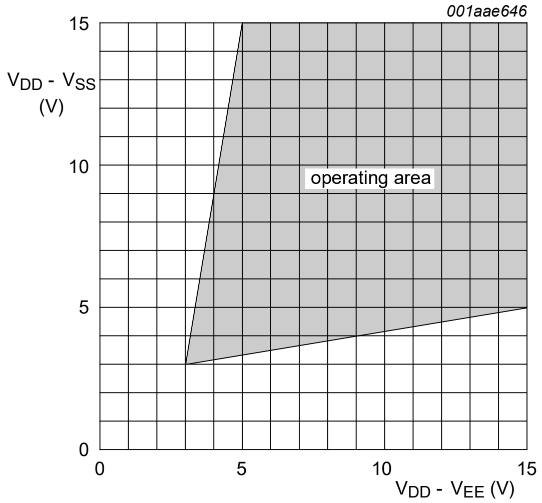


Fig. 7. Operating area as a function of the supply voltages

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = V_{EE} = 0$ V; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		T_{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\| < 1$ μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\| < 1$ μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	Z port; all channels OFF; see Fig. 8	15 V	-	-	-	1000	-	-	-	-	nA
		Y port; per channel; see Fig. 9	15 V	-	-	-	200	-	-	-	-	nA
I_{DD}	supply current	$I_O = 0$ A	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C_I	input capacitance	Sn, $\overline{E}$ inputs	-	-	-	-	7.5	-	-	-	-	pF

10.1. Test circuits

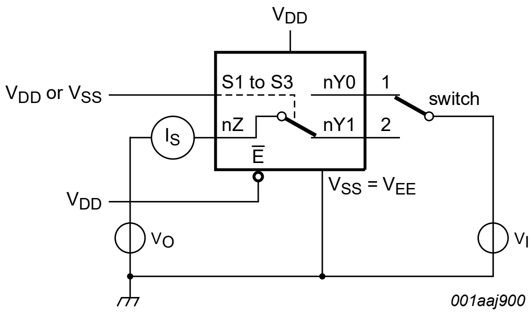


Fig. 8. Test circuit for measuring OFF-state leakage current Z port

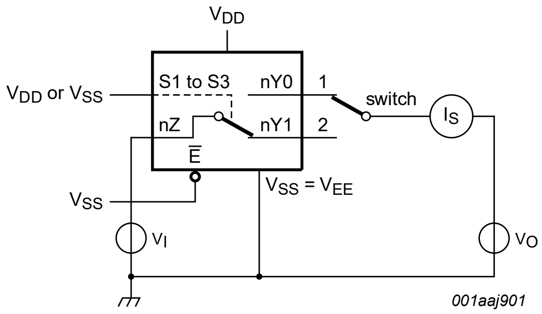


Fig. 9. Test circuit for measuring OFF-state leakage current nYn port

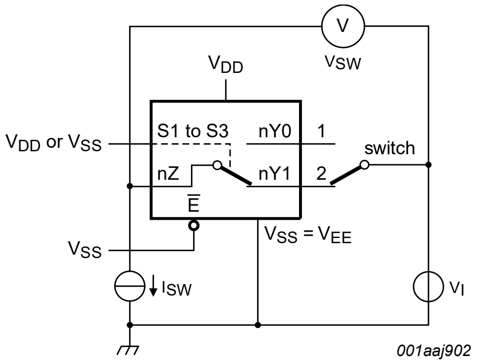
10.2. ON resistance

Table 7. ON resistance

T_{amb} = 25 °C; I_{SW} = 200 μA; V_{SS} = V_{EE} = 0 V.

Symbol	Parameter	Conditions	$V_{DD} - V_{EE}$	Typ	Max	Unit
$R_{ON(peak)}$	ON resistance (peak)	V_I = 0 V to V_{DD} - V_{EE}; see Fig. 10 and Fig. 11	5 V	350	2500	Ω
			10 V	80	245	Ω
			15 V	60	175	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = 0 V; see Fig. 10 and Fig. 11	5 V	115	340	Ω
			10 V	50	160	Ω
			15 V	40	115	Ω
		V_I = V_{DD} - V_{EE}; see Fig. 10 and Fig. 11	5 V	120	365	Ω
			10 V	65	200	Ω
			15 V	50	155	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0 V to V_{DD} - V_{EE}; see Fig. 10	5 V	25	-	Ω
			10 V	10	-	Ω
			15 V	5	-	Ω

10.2.1. ON resistance waveform and test circuit



$R_{ON} = V_{SW} / I_{SW}$.

Fig. 10. Test circuit for measuring R_{ON}

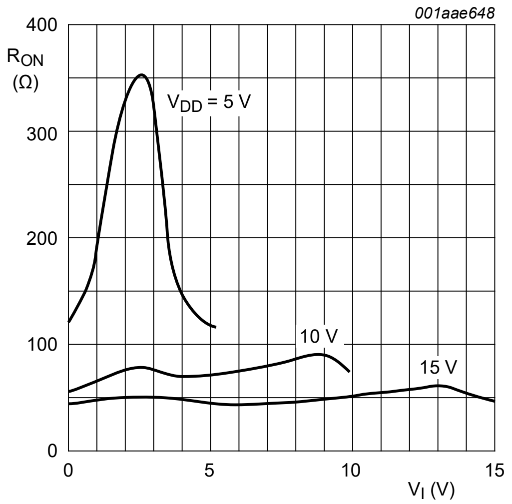


Fig. 11. Typical R_{ON} as a function of input voltage

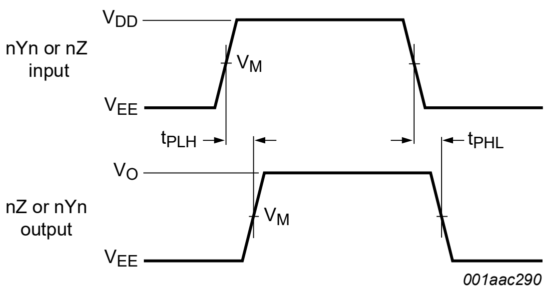
11. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = 25 °C; V_{SS} = V_{EE} = 0 V; for test circuit see Fig. 15.

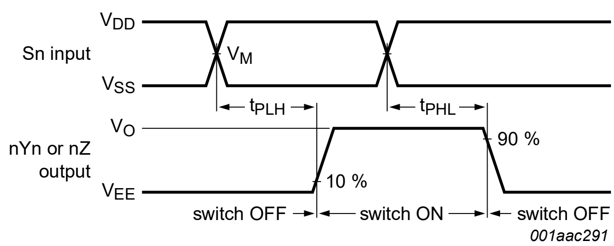
Symbol	Parameter	Conditions	V_{DD}	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nYn, nZ to nZ, nYn; see Fig. 12	5 V	10	20	ns
			10 V	5	10	ns
			15 V	5	10	ns
		Sn to nYn, nZ; see Fig. 13	5 V	200	400	ns
			10 V	85	170	ns
			15 V	65	130	ns
t_{PLH}	LOW to HIGH propagation delay	nYn, nZ to nZ, nYn; see Fig. 12	5 V	15	30	ns
			10 V	5	10	ns
			15 V	5	10	ns
		Sn to nYn, nZ; see Fig. 13	5 V	275	555	ns
			10 V	100	200	ns
			15 V	65	130	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{E}$ to nYn, nZ; see Fig. 14	5 V	200	400	ns
			10 V	115	230	ns
			15 V	110	220	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{E}$ to nYn, nZ; see Fig. 14	5 V	260	525	ns
			10 V	95	190	ns
			15 V	65	130	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{E}$ to nYn, nZ; see Fig. 14	5 V	200	400	ns
			10 V	120	245	ns
			15 V	110	215	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{E}$ to nYn, nZ; see Fig. 14	5 V	280	565	ns
			10 V	105	205	ns
			15 V	70	140	ns

11.1. Waveforms and test circuit



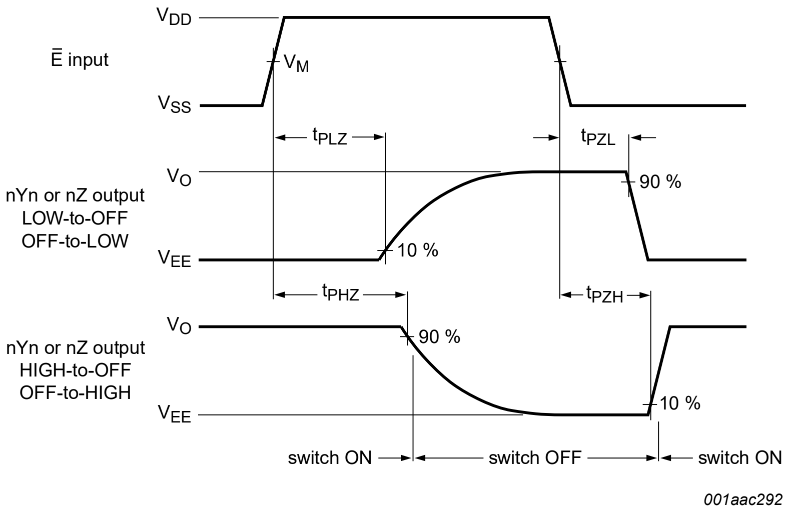
Measurement points are given in Table 9.

Fig. 12. nYn, nZ to nZ, nYn propagation delays



Measurement points are given in Table 9.

Fig. 13. Sn to nYn, nZ propagation delays

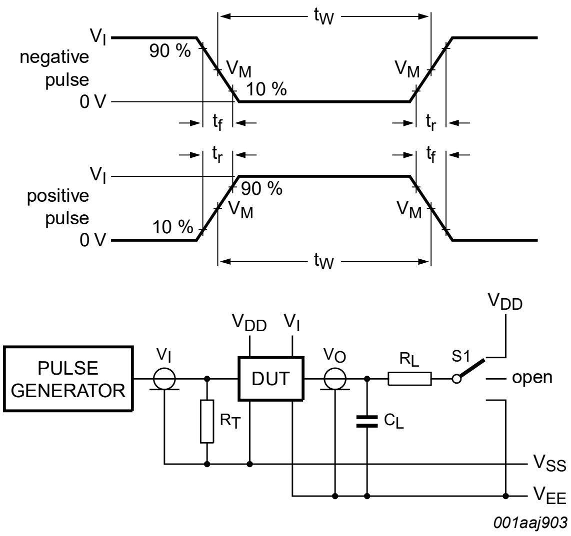


Measurement points are given in Table 9.

Fig. 14. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in Table 10.

Definitions:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including test jig and probe;

R_L = Load resistance.

Fig. 15. Test circuit for measuring switching times

Table 10. Test data

Input				Load		S1 position				
nYn, nZ	Sn and Ē	t_r, t_f	V_M	C_L	R_L	t_{PHL} [1]	t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	other
V_{DD} or V_{EE}	V_{DD} or V_{SS}	≤ 20 ns	$0.5V_{DD}$	50 pF	10 kΩ	V_{DD} or V_{EE}	V_{EE}	V_{EE}	V_{DD}	V_{EE}

[1] For nYn to nZ or nZ to nYn propagation delays use V_{EE}. For Sn to nYn or nZ propagation delays use V_{DD}.

11.2. Additional dynamic parameters

Table 11. Additional dynamic characteristics

$V_{SS} = V_{EE} = 0$ V; $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions		V_{DD}	Typ	Max	Unit
THD	total harmonic distortion	see Fig. 16; $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_I = 0.5V_{DD}$ (p-p); $f_i = 1$ kHz	[1]	5 V	0.25	-	%
				10 V	0.04	-	%
				15 V	0.04	-	%
$f_{(-3dB)}$	-3 dB frequency response	see Fig. 17; $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_I = 0.5V_{DD}$ (p-p)	[1]	5 V	13	-	MHz
				10 V	40	-	MHz
				15 V	70	-	MHz
α_{iso}	isolation (OFF-state)	see Fig. 18; $f_i = 1$ MHz; $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_I = 0.5V_{DD}$ (p-p)	[1]	10 V	-50	-	dB
V_{ct}	crosstalk voltage	digital inputs to switch; see Fig. 19; $R_L = 10$ kΩ; $C_L = 15$ pF; $\overline{E}$ or Sn = V_{DD} (square-wave)		10 V	50	-	mV
Xtalk	crosstalk	between switches; see Fig. 20; $f_i = 1$ MHz; $R_L = 1$ kΩ;$V_I = 0.5V_{DD}$ (p-p)	[1]	10 V	-50	-	dB

[1] f_i is biased at 0.5 V_{DD}; $V_I = 0.5V_{DD}$ (p-p).

Table 12. Dynamic power dissipation

P_D can be calculated from the formulas shown; $V_{EE} = V_{SS} = 0$ V; $t_r = t_f \leq 20$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 2500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 11500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	
		15 V	$P_D = 29000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	

11.2.1. Test circuits

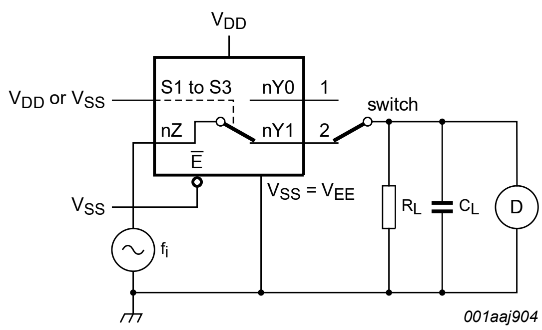


Fig. 16. Test circuit for measuring total harmonic distortion

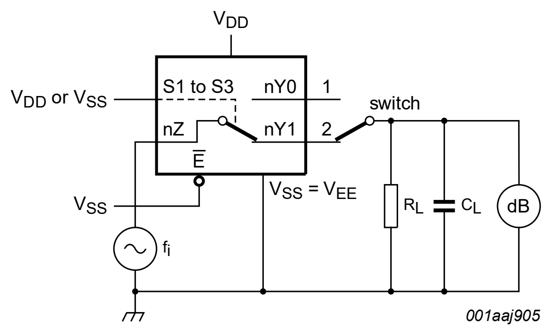


Fig. 17. Test circuit for measuring frequency response

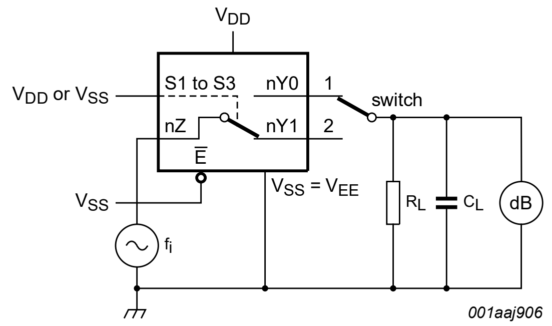
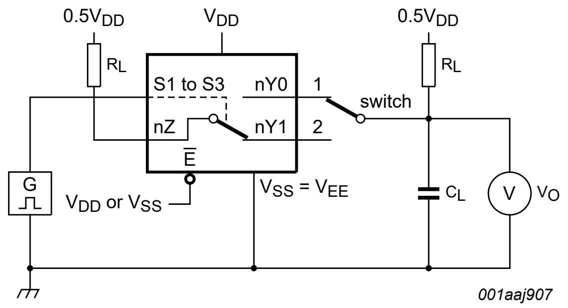
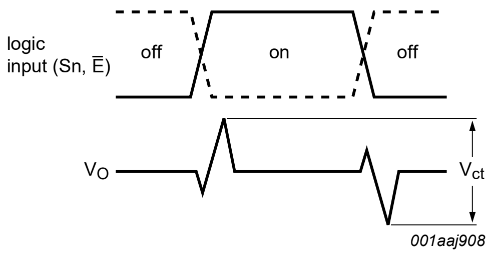


Fig. 18. Test circuit for measuring isolation (OFF-state)

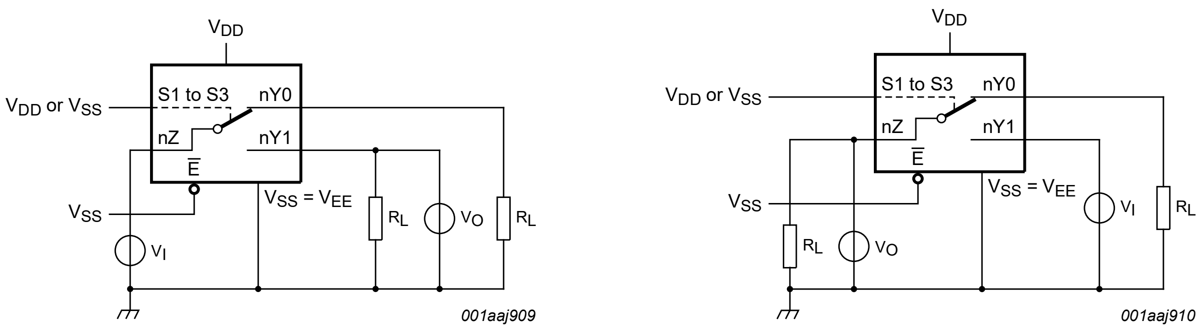


a. Test circuit



b. Input and output pulse definitions

Fig. 19. Test circuit for measuring crosstalk voltage between digital inputs and switch



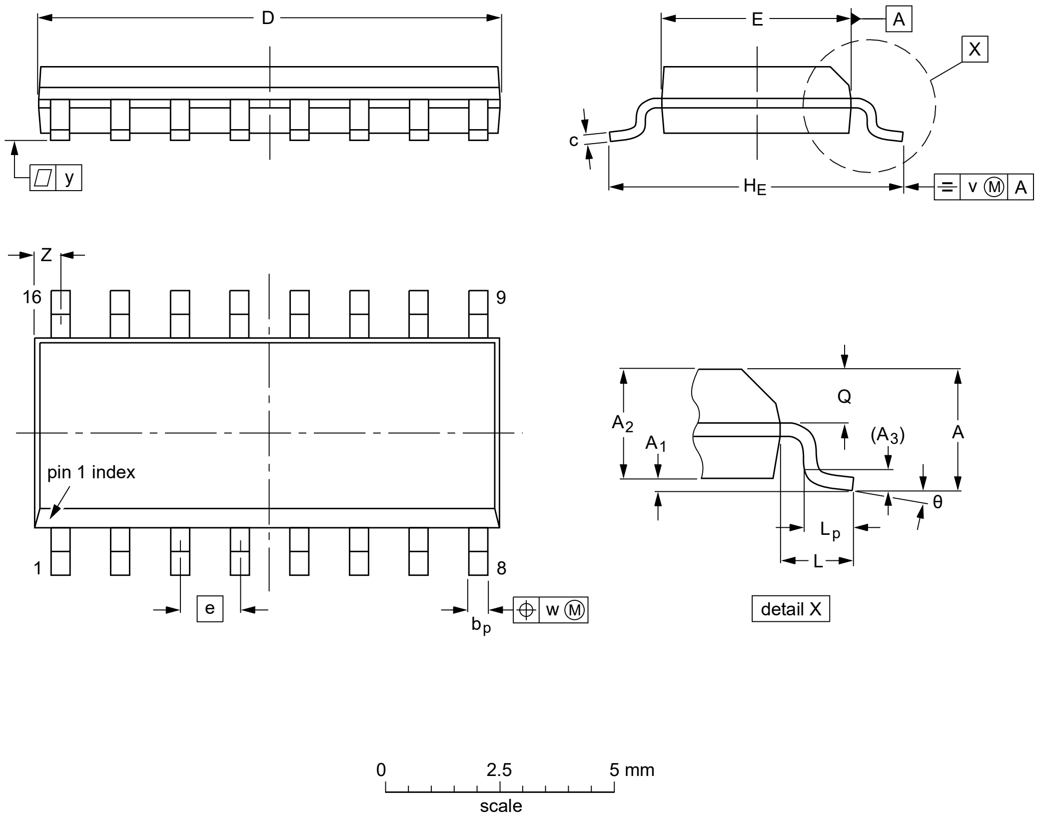
a. Switch closed condition

b. Switch open condition

Fig. 20. Test circuit for measuring crosstalk between switches

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D[(1)]	E[(1)]	e	H_E	L	L_p	Q	v	w	y	Z[(1)]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

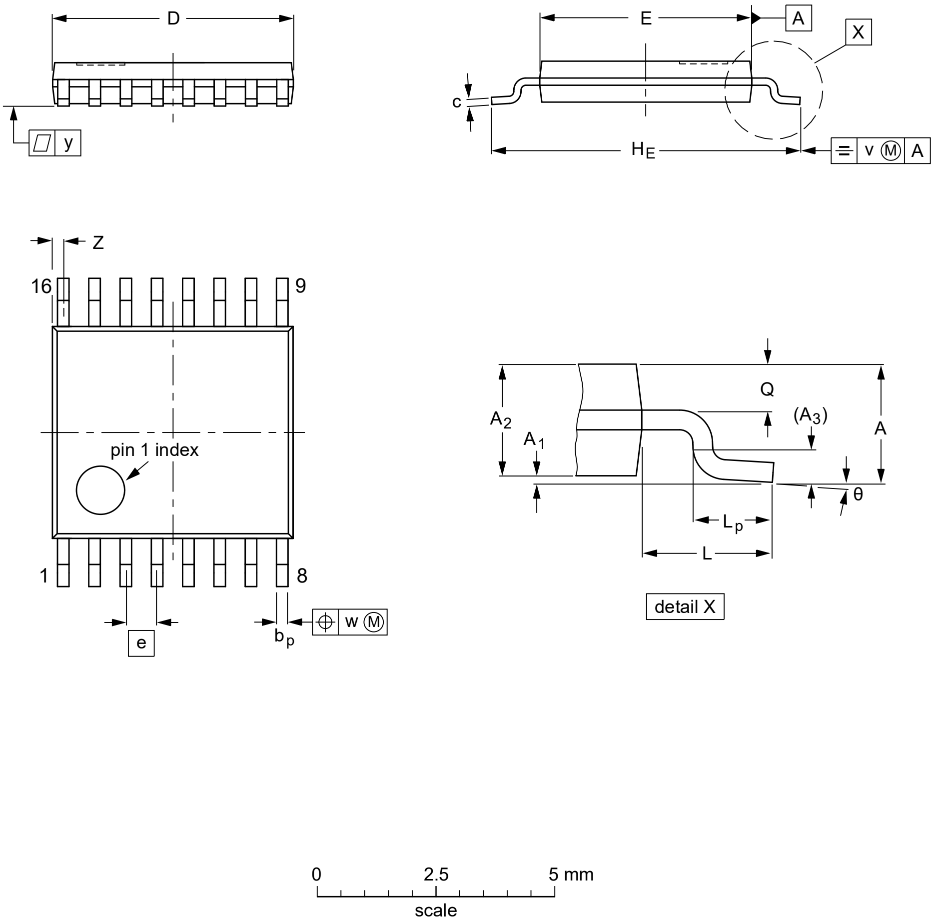
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 21. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 22. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4053B_Q100 v.3	20211221	Product data sheet	-	HEF4053B_Q100 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation updated. • Table 13 updated.			
HEF4053B_Q100 v.2	20140911	Product data sheet	-	HEF4053B_Q100 v.1
Modifications:	• Fig. 19: Test circuit modified			
HEF4053B_Q100 v.1	20130222	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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